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# HCPL-540x, 5962-89570, HCPL-543x, HCPL-643x, 5962-89571 <sup>1</sup>



## Hermetically Sealed, Very High Speed, Logic Gate Optocouplers

### Data Sheet

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#### Description

These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either commercial product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DLA Standard Microcircuit Drawing (SMD). All devices are manufactured and tested on a MIL-PRF-38534 certified line, and Class H and K devices are included in the DLA Qualified Manufacturers List, QML-38534 for Hybrid Microcircuits.

**CAUTION** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

1. See [Selection Guide – Lead Configuration Options](#) for available extensions.

#### Features

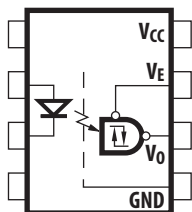
- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 certified line
- QML-38534, Class H and K
- Two hermetically sealed package configurations
- Performance guaranteed over full military temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- High speed: 40 M bit/s
- High common mode rejection 500 V/ $\mu\text{s}$  guaranteed
- 1500 Vdc withstand test voltage
- Active (totem pole) outputs
- Three stage output available
- High radiation immunity
- HCPL-2400/30 function compatibility
- Reliability data
- Compatible with TTL, STTL, LSTTL, and HCMOS logic families

#### Applications

- Military and space
- High reliability systems
- Transportation, medical, and life critical systems
- Isolation of high-speed logic systems
- Computer-peripheral interfaces
- Switching power supplies
- Isolated bus driver (networking applications) – (5400/1/K only)
- Pulse transformer replacement
- Ground loop elimination
- Harsh industrial environments
- High-speed disk drive I/O
- Digital isolation for A/D, D/A conversion

## Functional Diagram

Multiple-channel devices available.



## Truth Tables

(Positive Logic)

### Multichannel Devices

Input	Output
On (H)	L
Off (L)	H

### Single-Channel DIP

Input	Enable	Output
On (H)	L	L
Off (L)	L	H
On (H)	H	Z
Off (L)	H	Z

**NOTE** The connection of a 0.1- $\mu$ F bypass capacitor between  $V_{CC}$  and GND is recommended.

Each channel contains an AlGaAs light emitting diode, which is optically coupled to an integrated high gain photon detector. This combination results in very high data rate capability. The detector has a threshold with hysteresis, which typically provides 0.25 mA of differential mode noise immunity and minimizes the potential for output signal chatter. The detector in the single-channel units has a three-state output stage that eliminates the need for a pull-up resistor and allows for direct drive of a data bus.

All units are compatible with TTL, STTL, LSTTL, and HCMOS logic families. The 35-ns pulse width distortion specification guarantees a 10 MBd signaling rate at +125°C with 35% pulse width distortion. [Figure 13](#) through [Figure 16](#) show recommended circuits for reducing pulse width distortion and optimizing the signal rate of the product. Package styles for these parts are 8-pin DIP through hole (case outlines P) and leadless ceramic chip carrier (case outline 2). Devices can be purchased with a variety of lead bend and plating options. See [Selection Guide – Lead Configuration Options](#) for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are similar for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.



## Selection Guide – Lead Configuration Options

Package	8-Pin DIP	8-Pin DIP	20-Pad LCCC
Lead Style	Through Hole	Through Hole	Surface Mount
Channels	1	2	2
Common Channel Wiring	None	V <sub>CC</sub> , GND	None
<b>Part Number and Options</b>			
Commercial	HCPL-5400	HCPL-5430	HCPL-6430
MIL-PRF-38534, Class H	HCPL-5401	HCPL-5431	HCPL-6431
MIL-PRF-38534, Class K	HCPL-540K	HCPL-543K	HCPL-643K
Standard Lead Finish	Gold Plate <sup>a</sup>	Gold Plate <sup>a</sup>	Solder Pads <sup>b</sup>
Solder Dipped <sup>b</sup>	Option 200	Option 200	
Butt Cut/Gold Plate <sup>a</sup>	Option 100	Option 100	
Gull Wing/Soldered <sup>b</sup>	Option 300	Option 300	
<b>Class H SMD Part Number</b>			
Prescript for all below	5962-	5962-	5962-
Gold Plate <sup>a</sup>	8957001PC	8957101PC	
Solder Dipped <sup>b</sup>	8957001PA	8957101PA	89571022A
Butt Cut/Gold Plate <sup>a</sup>	8957001YC	8957101YC	
Butt Cut/Soldered <sup>b</sup>	8957001YA	8957101YA	
Gull Wing/Soldered <sup>b</sup>	8957001XA	8957101XA	
<b>Class K SMD Part Number</b>			
Prescript for all below	5962-	5962-	5962-
Gold Plate <sup>a</sup>	8957002KPC	8957103KPC	
Solder Dipped <sup>b</sup>	8957002KPA	8957103KPA	8957104K2A
Butt Cut/Gold Plate <sup>a</sup>	8957002KYC	8957103KYC	
Butt Cut/Soldered <sup>b</sup>	8957002KYA	8957103KYA	
Gull Wing/Soldered <sup>b</sup>	8957002KXA	8957103KXA	

a. Gold plate lead finish: Maximum gold thickness of leads is <100 micro-inches. Typical is 60 to 90 micro-inches.

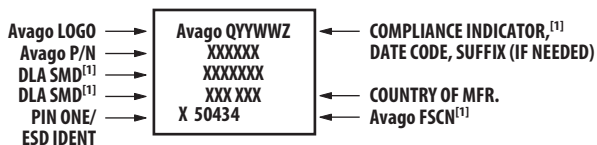
b. Solder lead finish: Sn63/Pb37.

## Functional Diagrams

8-Pin DIP	8-Pin DIP	20-Pad LCCC
Through Hole	Through Hole	Surface Mount
1 Channel	2 Channels	2 Channels

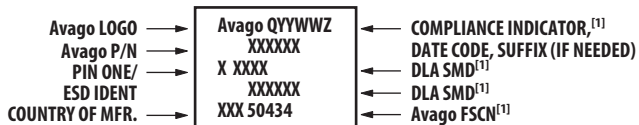
**NOTE** All DIP devices have common  $V_{CC}$  and ground. LCCC (leadless ceramic chip carrier) package has isolated channels with separate  $V_{CC}$  and ground connections. All diagrams are top view.

## Leaded Device Marking



[1] QML PARTS ONLY

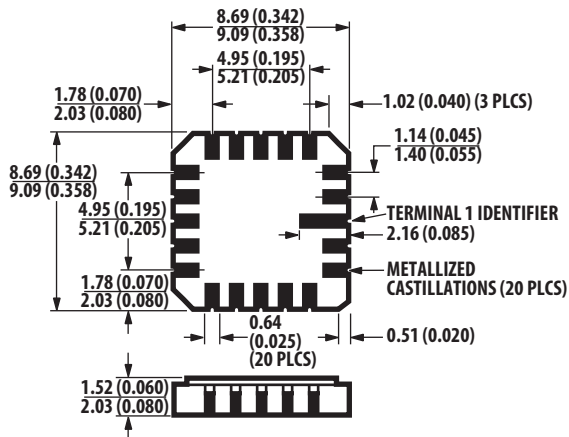
## Leadless Device Marking



[1] QML PARTS ONLY

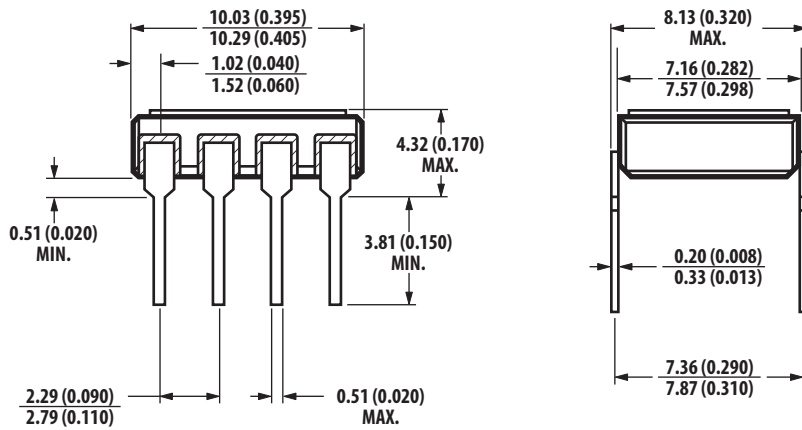
## Outline Drawings

### 20-Terminal LCCC Surface Mount, 2 Channels



Note: Dimensions in millimeters (inches).  
Solder thickness 0.127 (0.005) max.

### 8-Pin DIP Through Hole, 1 and 2 Channel



Note: Dimensions in millimeters (inches).

## Hermetic Optocoupler Options

Option	Description
100	<p>Surface-mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H, and Class K product in 8-pin DIP.</p> <p>Note: Dimensions in millimeters (inches).</p>
200	<p>Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H, and Class K product in 8-pin DIP. DLA Drawing (SMD) part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder-dipped terminals as a standard feature.</p>
300	<p>Surface-mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on Commercial, Class H, and Class K in 8-pin DIP. This option has solder-dipped leads.</p> <p>Note: Dimensions in millimeters (inches).</p>

## Absolute Maximum Ratings

No derating required up to +125°C.

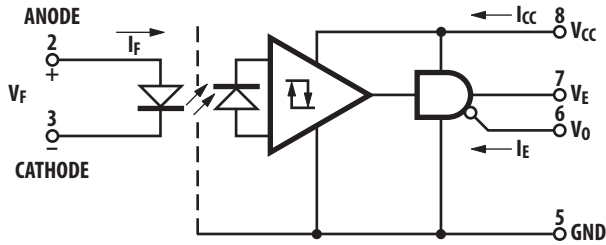
Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	$T_S$	-65	+150	°C	
Operating Temperature	$T_A$	-55	+125	°C	
Case Temperature	$T_C$	—	+170	°C	
Junction Temperature	$T_J$	—	+175	°C	
Lead Solder Temperature		—	260 for 10 sec	°C	
Average Forward Current (each channel)	$I_{F(AVG)}$	—	10	mA	
Peak Input Current (each channel)	$I_{F(PEAK)}$	—	20	mA	a
Reverse Input Voltage (each channel)	$V_R$	—	3	V	
Supply Voltage	$V_{CC}$	0.0	7.0	V	
Average Output Current (each channel)	$I_{O(AVG)}$	-25	25	mA	
Output Voltage (each channel)	$V_O$	-0.5	10	V	
Output Power Dissipation (each channel)	$P_O$	—	130	mW	
Package Power Dissipation (each channel)	$P_D$	—	200	mW	

a. Not to exceed 5% duty factor, not to exceed 50  $\mu$ s pulse width.

## Single-Channel Product Only

Parameter	Symbol	Min	Max	Unit	Note
Three State Enable Voltage	$V_E$	-0.5	10	V	

## 8-Pin Ceramic DIP Single-Channel Schematic



Note: Enable pin 7. An external 0.01- $\mu$ F to 0.1- $\mu$ F bypass capacitor must be connected between  $V_{CC}$  and ground for each package type.

## ESD Classification

(MIL-STD-883, Method 3015)	
HCPL-5400/01/0K	▲▲, Class 2
HCPL-5430/31/3K and HCPL-6430/31/3K	●, Class 3

## Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Current (High)	$I_{F(ON)}$	6	10	mA
Supply Voltage, Output	$V_{CC}$	4.75	5.25	V
Input Voltage (Low)	$V_{F(OFF)}$	—	0.7	V
Fan Out (Each Channel)	N	—	5	TTL Loads

## Single-Channel Product Only

Parameter	Symbol	Min	Max	Unit
High Level Enable Voltage	$V_{EH}$	2.0	$V_{CC}$	V
Low Level Enable Voltage	$V_{EL}$	0	0.8	V



## Electrical Characteristics

$T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ ,  $6\text{ mA} \leq I_{F(\text{ON})} \leq 10\text{ mA}$ ,  $0\text{V} \leq V_{F(\text{OFF})} \leq 0.7\text{V}$ , unless otherwise specified.

Parameter	Sym	Test Conditions	Group A Subgroups <sup>a</sup>	Limits			Unit	Fig	Notes
				Min	Typ <sup>b</sup>	Max			
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 8.0\text{ mA}$ (5 TTL Loads)	1, 2, 3	—	0.3	0.5	V	1	c
High Level Output Voltage	$V_{OH}$	$I_{OH} = -4.0\text{ mA}$	1, 2, 3	2.4	—	—	V	2	c
Output Leakage Current	$I_{OHH}$	$V_O = 5.25\text{V}$ , $V_F = 0.7\text{V}$	1, 2, 3	—	—	100	$\mu\text{A}$		c
Logic High Supply Current	Single Channel	$V_{CC} = 5.25\text{V}$ , $V_E = 0\text{V}$	1, 2, 3	—	17	26	mA		
	Dual Channel			—	34	52			
Logic Low Supply Current	Single Channel		1, 2, 3	—	19	26	mA		
	Dual Channel			—	38	52			
Input Forward Voltage	$V_F$	$I_F = 10\text{ mA}$	1, 2, 3	1.0	1.35	1.85	V	4	c
Input Reverse Breakdown Voltage	$V_R$	$I_R = 10\text{ }\mu\text{A}$	1, 2, 3	3.0	4.8	—	V		c
Input-Output Insulation Leakage Current	$I_{I-O}$	$V_{I-O} = 1500\text{ Vdc}$ , $RH \leq 65\%$ , $t = 5\text{ s}$	1	—	—	1.0	$\mu\text{A}$		e, f
Propagation Delay Time Logic Low Output	$t_{PHL}$		9, 10, 11	—	33	60	ns	5, 6, 7	g, c
Propagation Delay Time Logic High Output	$t_{PLH}$		9, 10, 11	—	30	60	ns	5, 6, 7	g, c
Pulse Width Distortion	PWD		9, 10, 11	—	3	35	ns	5, 6, 7	g, c
Logic High Common-Mode Transient Immunity	$ CM_H $	$V_{CM} = 50\text{ V}_{P-P}$ , $I_F = 0\text{ mA}$	9, 10, 11	500	3000	—	$\text{V}/\mu\text{s}$	11	h, c, i
Logic Low Common-Mode Transient Immunity	$ CM_L $	$V_{CM} = 50\text{ V}_{P-P}$ , $I_F = 6\text{ mA}$	9, 10, 11	500	3000	—	$\text{V}/\mu\text{s}$	11	h, c, i

- Commercial parts receive 100% testing at  $25^\circ\text{C}$  (Subgroups 1 and 9). SMD, Class H and Class K parts receive 100% testing at  $25^\circ\text{C}$ ,  $125^\circ\text{C}$ , and  $-55^\circ\text{C}$  (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $I_F = 8\text{ mA}$  unless otherwise specified.
- Each channel.
- The HCPL-6430, HCPL-6431, and HCPL-643K dual-channel parts function as two independent single-channel units. Use the single-channel parameter limits.
- All devices are considered two-terminal devices: measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
- This is a momentary withstand test, not an operating condition.
- $t_{PHL}$  propagation delay is measured from the 50% point on the rising edge of the input current pulse to the 1.5V point on the falling edge of the output pulse. The  $t_{PLH}$  propagation delay is measured from the 50% point on the falling edge of the input current pulse to the 1.5V point on the rising edge of the output pulse. Pulse Width Distortion,  $PWD = |t_{PHL} - t_{PLH}|$ .
- $CM_L$  is the maximum slew rate of the common-mode voltage that can be sustained with the output voltage in the logic low state ( $V_{O(\text{MAX})} < 0.8\text{V}$ ).  $CM_H$  is the maximum slew rate of the common-mode voltage that can be sustained with the output voltage in the logic high state ( $V_{O(\text{MIN})} > 2.0\text{V}$ ).
- Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

## Single-Channel Product Only

Parameter	Sym	Test Conditions	Group A Subgroups <sup>a</sup>	Limits			Unit	Fig	Notes
				Min	Typ <sup>b</sup>	Max			
Logic High Enable Voltage	V <sub>EH</sub>		1, 2, 3	2.0	—	—	V		
Logic Low Enable Voltage	V <sub>EL</sub>		1, 2, 3	—	—	0.8	V		
Logic High Enable Current	I <sub>EH</sub>	V <sub>E</sub> = 2.4V	1, 2, 3	—	—	20	μA		
		V <sub>E</sub> = 5.25V	1, 2, 3	—	—	100			
Logic Low Enable Current	I <sub>EL</sub>	V <sub>E</sub> = 0.4V	1, 2, 3	—	-0.28	-0.4	mA		
High Impedance State Supply Current	I <sub>CCZ</sub>	V <sub>CC</sub> = 5.25V, V <sub>E</sub> = 5.25V	1, 2, 3	—	22	28	mA		
High Impedance State Output Current	I <sub>OZL</sub>	V <sub>O</sub> = 0.4V, V <sub>E</sub> = 2V	1, 2, 3	—	—	-20	μA		
		V <sub>O</sub> = 2.4V, V <sub>E</sub> = 2V		—	—	20			
		V <sub>O</sub> = 5.25V, V <sub>E</sub> = 2V		—	—	100			

- a. Commercial parts receive 100% testing at 25°C (Subgroup 1). SMD, Class H and Class K parts receive 100% testing at 25°C, 125°C, and -55°C (Subgroups 1, 2, and 3, respectively).
- b. All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, I<sub>F</sub> = 8 mA unless otherwise specified.

## Typical Characteristics

All typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V, I<sub>F</sub> = 8 mA, unless otherwise specified.

Parameter	Symbol	Typ	Unit	Test Conditions	Fig	Notes
Input Current Hysteresis	I <sub>HYS</sub>	0.25	mA	V <sub>CC</sub> = 5V	3	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.11	mV/°C	I <sub>F</sub> = 10 mA	4	
Resistance (Input-Output)	R <sub>I-O</sub>	10 <sup>12</sup>	Ω	V <sub>I-O</sub> = 500V		a
Capacitance (Input-Output)	C <sub>I-O</sub>	0.6	pF	f = 1 MHz, V <sub>I-O</sub> = 0V		a
Logic Low Short Circuit Output Current	I <sub>OSL</sub>	65	mA	V <sub>O</sub> = V <sub>CC</sub> = 5.25V, I <sub>F</sub> = 10 mA		b, c
Logic High Short Circuit Output Current	I <sub>OSH</sub>	-50	mA	V <sub>CC</sub> = 5.25V, I <sub>F</sub> = 0 mA, V <sub>O</sub> = GND		b, c
Output Rise Time (10% to 90%)	t <sub>r</sub>	15	ns		5	
Output Fall Time (90% to 10%)	t <sub>f</sub>	10	ns		5	
Propagation Delay Skew	t <sub>PSK</sub>	30	ns		10	d
Power Supply Noise Immunity	PSNI	0.5	V <sub>p-p</sub>	48 Hz ≤ f <sub>ac</sub> ≤ 50 MHz		e

- a. All devices are considered two-terminal devices: measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
- b. Duration of output short circuit time not to exceed 10 ms.
- c. Each channel.
- d. Propagation delay skew is defined as the difference between the minimum and maximum propagation delays for any given group of optocouplers with the same part number that are all switching at the same time under the same operating conditions.
- e. Power Supply Noise Immunity is the peak-to-peak amplitude of the ac ripple voltage on the V<sub>CC</sub> line that the device will withstand and still remain in the desired logic state. For desired logic high state, V<sub>OH(MIN)</sub> > 2.0V, and for desired logic low state, V<sub>OL(MAX)</sub> < 0.8V.

## Single-Channel Product Only

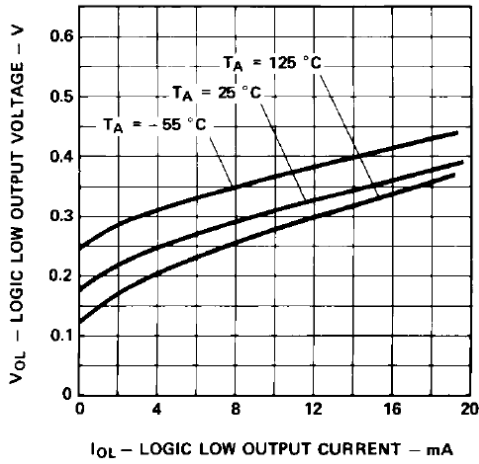
Parameter	Symbol	Typ	Unit	Test Conditions	Fig	Notes
Input Capacitance	$C_{IN}$	15	pF	$f = 1 \text{ MHz}, V_F = 0V,$ Pins 2 and 3		
Output Enable Time to Logic High	$t_{PZH}$	15	ns		8, 9	
Output Enable Time to Logic Low	$t_{PZL}$	30	ns		8, 9	
Output Disable Time from Logic High	$t_{PHZ}$	20	ns		8, 9	
Output Disable Time from Logic Low	$t_{PLZ}$	15	ns		8, 9	

## Dual-Channel Product Only

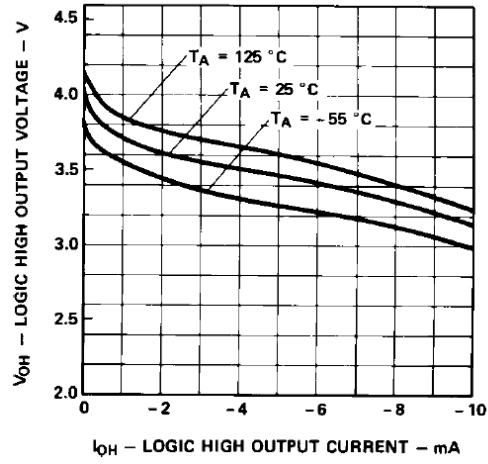
Parameter	Symbol	Typ	Unit	Test Conditions	Fig	Notes
Input Capacitance	$C_{IN}$	15	pF	$f = 1 \text{ MHz}, V_O = 0V$		
Input-Input Leakage Current	$I_{I-I}$	0.5	nA	$RH \leq 65\%, V_{I-I} = 500 \text{ Vdc}$		a
Input-Input Resistance	$R_{I-I}$	$10^{12}$	$\Omega$	$V_{I-I} = 500V$		a
Input-Input Capacitance	$C_{I-I}$	1.3	pF	$f = 1 \text{ MHz}, V_F = 0V$		a

a. Measured between adjacent input pairs shorted together for each multichannel device.

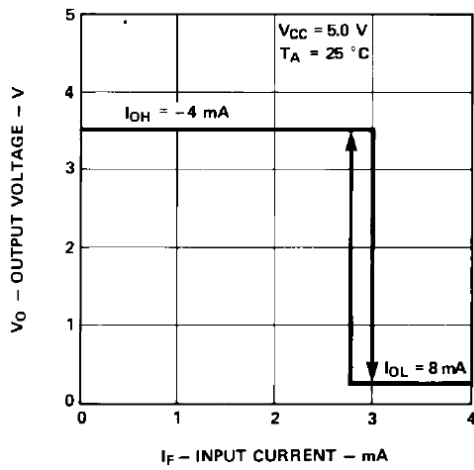
**Figure 1 Typical Logic Low Output Voltage vs. Logic Low Output Current**



**Figure 2 Typical Logic High Output Voltage vs. Logic High Output Current**



**Figure 3 Typical Output Voltage vs. Input Forward Current**



**Figure 4 Typical Diode Input Forward Current Characteristic**

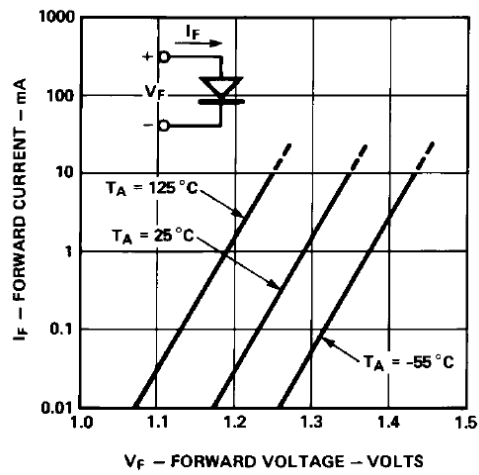


Figure 5 Test Circuit for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ , and  $t_f$

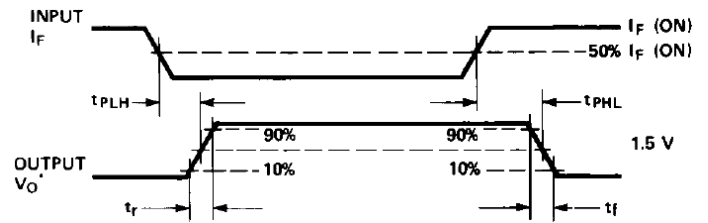
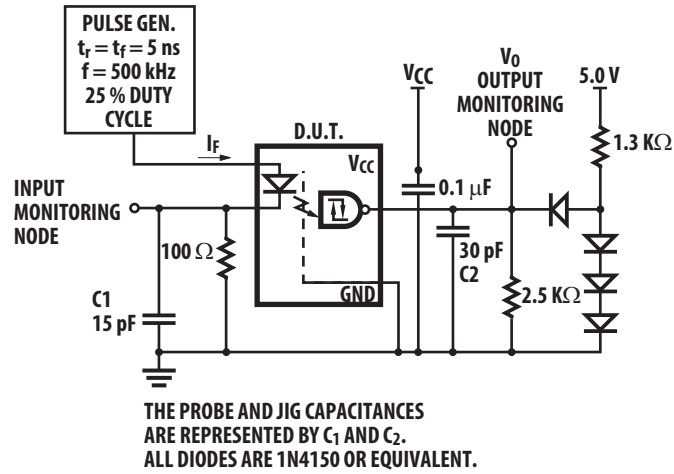


Figure 6 Typical Propagation Delay vs. Ambient Temperature

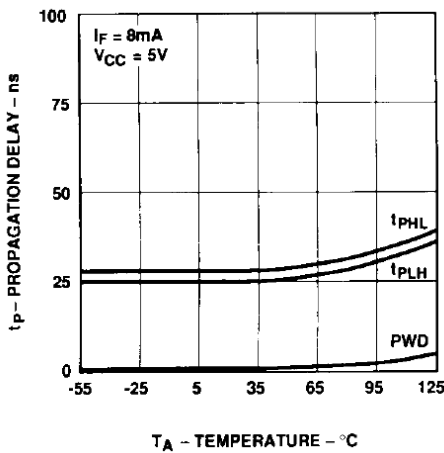


Figure 7 Typical Propagation Delay vs. Input Forward Current

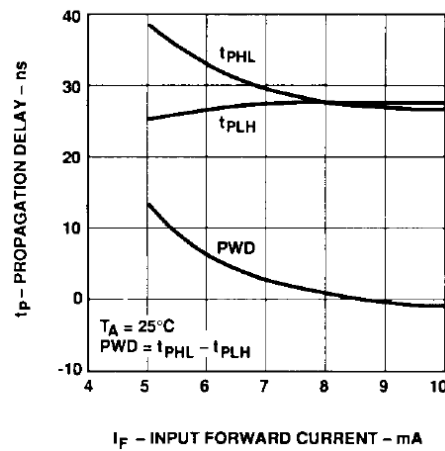
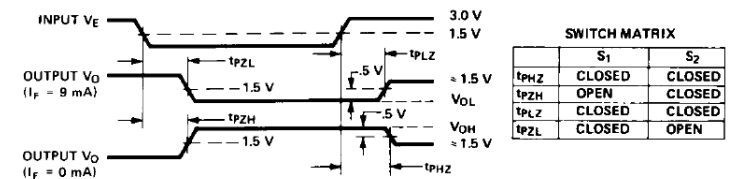
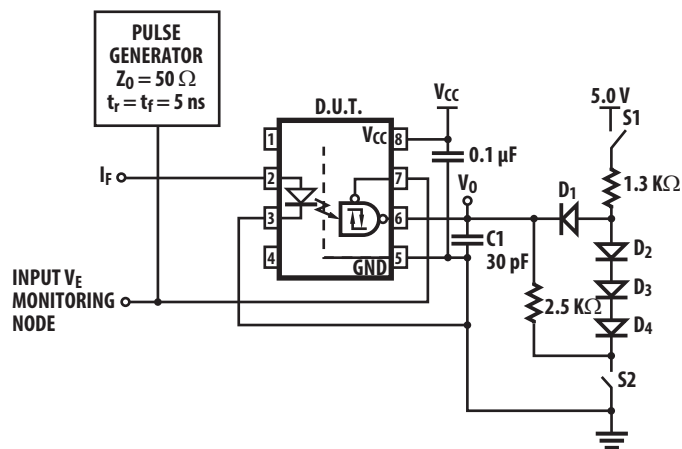


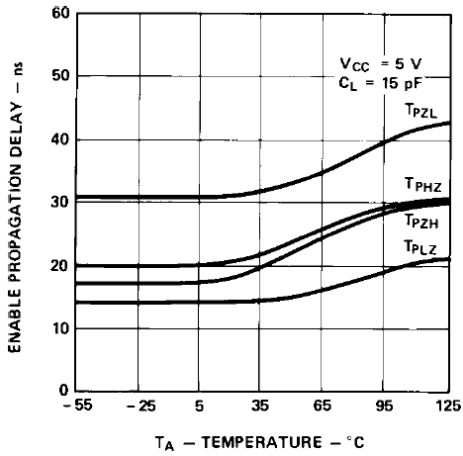
Figure 8 Test Circuit for  $t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PLZ}$ , and  $t_{PZL}$  (Single-Channel Product Only)



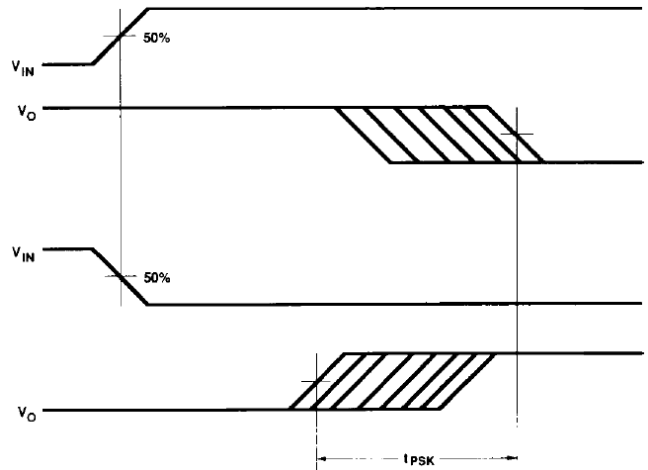
	S <sub>1</sub>	S <sub>2</sub>
$t_{PHZ}$	CLOSED	CLOSED
$t_{PZH}$	OPEN	CLOSED
$t_{PLZ}$	CLOSED	CLOSED
$t_{PZL}$	CLOSED	OPEN

ALL DIODES ARE 1N4150 OR EQUIVALENT  
C<sub>1</sub> = 30 pF INCLUDING PROBE AND JIG CAPACITANCE.

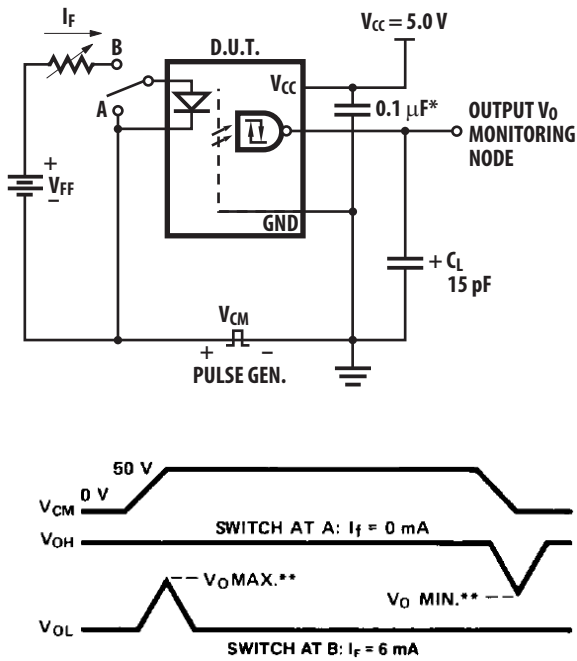
**Figure 9 Typical Enable Propagation Delay vs. Ambient Temperature (Single-Channel Product Only)**



**Figure 10 Propagation Delay Skew,  $t_{PSK}$ , Waveform**

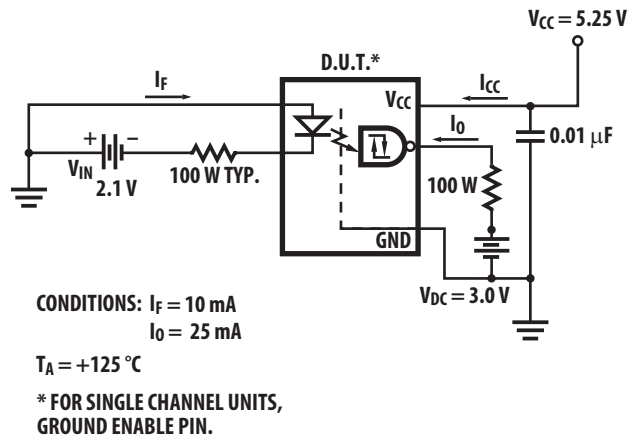


**Figure 11 Test Diagram for Common-Mode Transient Immunity and Typical Waveforms**



\*TOTAL LEAD LENGTH < 10 mm FROM DEVICE UNDER TEST.  
\*\*SEE NOTE 5.  
† $C_L$  IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

**Figure 12 Operating Circuit for Burn-in and Steady State Life Tests**





## Data Rate and Pulse-Width Distortion Definitions

Propagation delay is a figure of merit that describes the finite amount of time required for a system to translate information from input to output when shifting logic levels. Propagation delay from low to high ( $t_{PLH}$ ) specifies the amount of time required for a system's output to change from a Logic 0 to a Logic 1, when given a stimulus at the input. Propagation delay from high to low ( $t_{PHL}$ ) specifies the amount of time required for a system's output to change from a Logic 1 to a Logic 0, when given a stimulus at the input (see Figure 5).

When  $t_{PLH}$  and  $t_{PHL}$  differ in value, pulse width distortion results. Pulse width distortion is defined as  $|t_{PHL} - t_{PLH}|$  and determines the maximum data rate capability of a distortion-limited system. Maximum pulse width distortion on the order of 25% to 35% is typically used when specifying the maximum data rate capabilities of systems. The exact figure depends on the particular application (RS-232, PCM, T-1, etc.).

These high-performance optocouplers offer the advantages of specified propagation delay ( $t_{PLH}$ ,  $t_{PHL}$ ), and pulse width distortion ( $|t_{PLH} - t_{PHL}|$ ) over temperature and power supply voltage ranges.

## Applications

Figure 13 Recommended HCPL-540x Interface Circuit

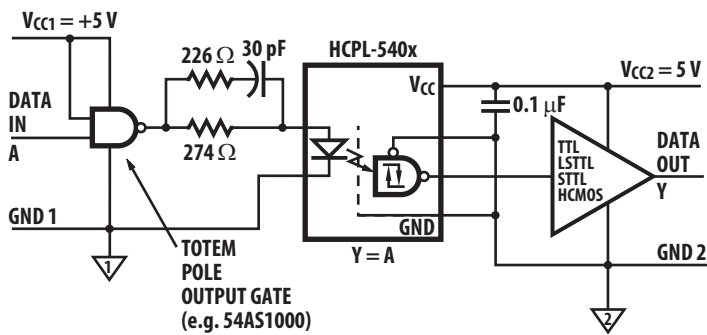
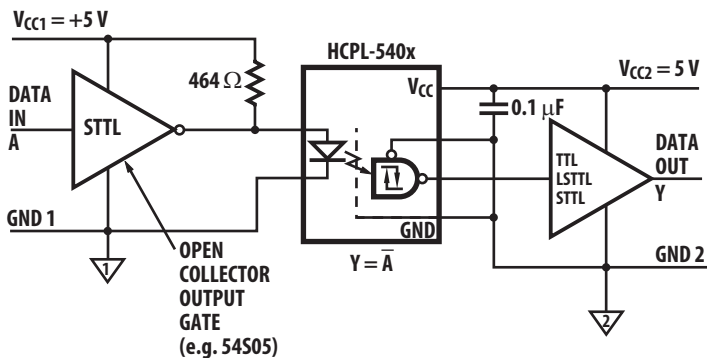
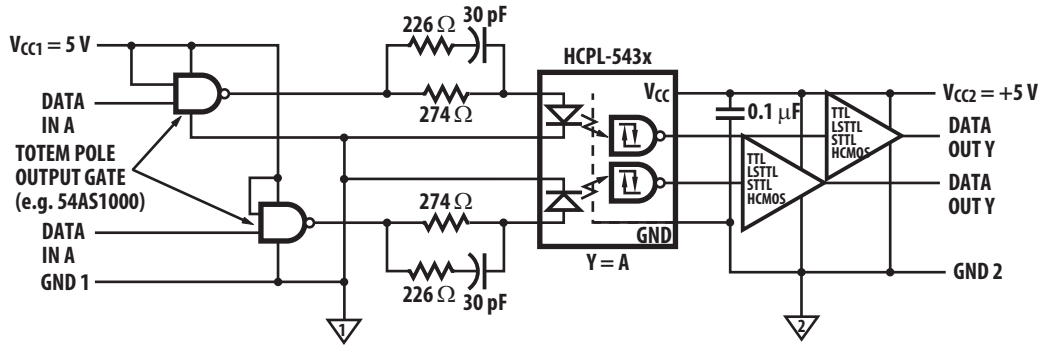


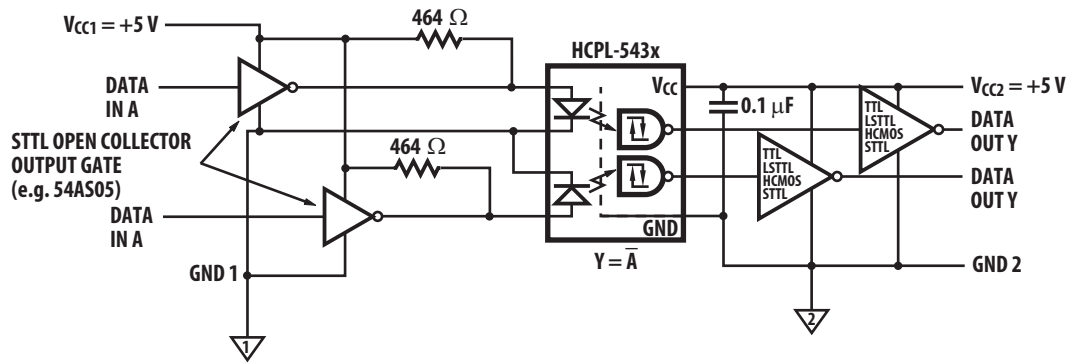
Figure 14 Alternative HCPL-540x Interface Circuit



**Figure 15 Recommended HCPL-543x and HCPL-643x Interface Circuit**



**Figure 16 Alternative HCPL-543x and HCPL-643x Interface Circuit**



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