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April 1st, 2010
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User's Manual

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SH7020 and SH7021

Hardware Manual

SuperH™ RISC engine

HD6437020, HD6477021,
HD6437021, HD6417021

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Introduction

The SH7020 and SH7021 are part of a new generation of reduced instruction-set computer-type (RISC) microcomputers that integrate RISC-type CPUs and the peripheral functions required for system configuration onto a single chip to achieve high-performance operations processing. They can operate in a power-down state, which is an essential feature for portable equipment.

The SH7020 and SH7021 CPUs have RISC-type instruction sets. Basic instructions can be executed in a single clock cycle, which strikingly improves instruction execution speed. The SH7020 and SH7021 include peripheral functions such as large-capacity ROM (PROM or masked ROM), RAM, a direct memory access controller (DMAC), timers, a serial communication interface (SCI), an interrupt controller (INTC), and I/O ports. These on-chip elements enable users to construct systems with the fewest possible components. External memory access support functions enable direct connection to SRAM and DRAM. without the use of glue logics.

This Hardware Manual describes in detail the hardware functions of the SH7020 and SH7021. For information on the instructions, please refer to the Programming Manual.

Related Manuals

SH7000 Series Instructions

"SH-1/SH-2/SH-DSP Programming Manual"

For development support tools, contact your Hitachi sales office.

Organization of This Manual

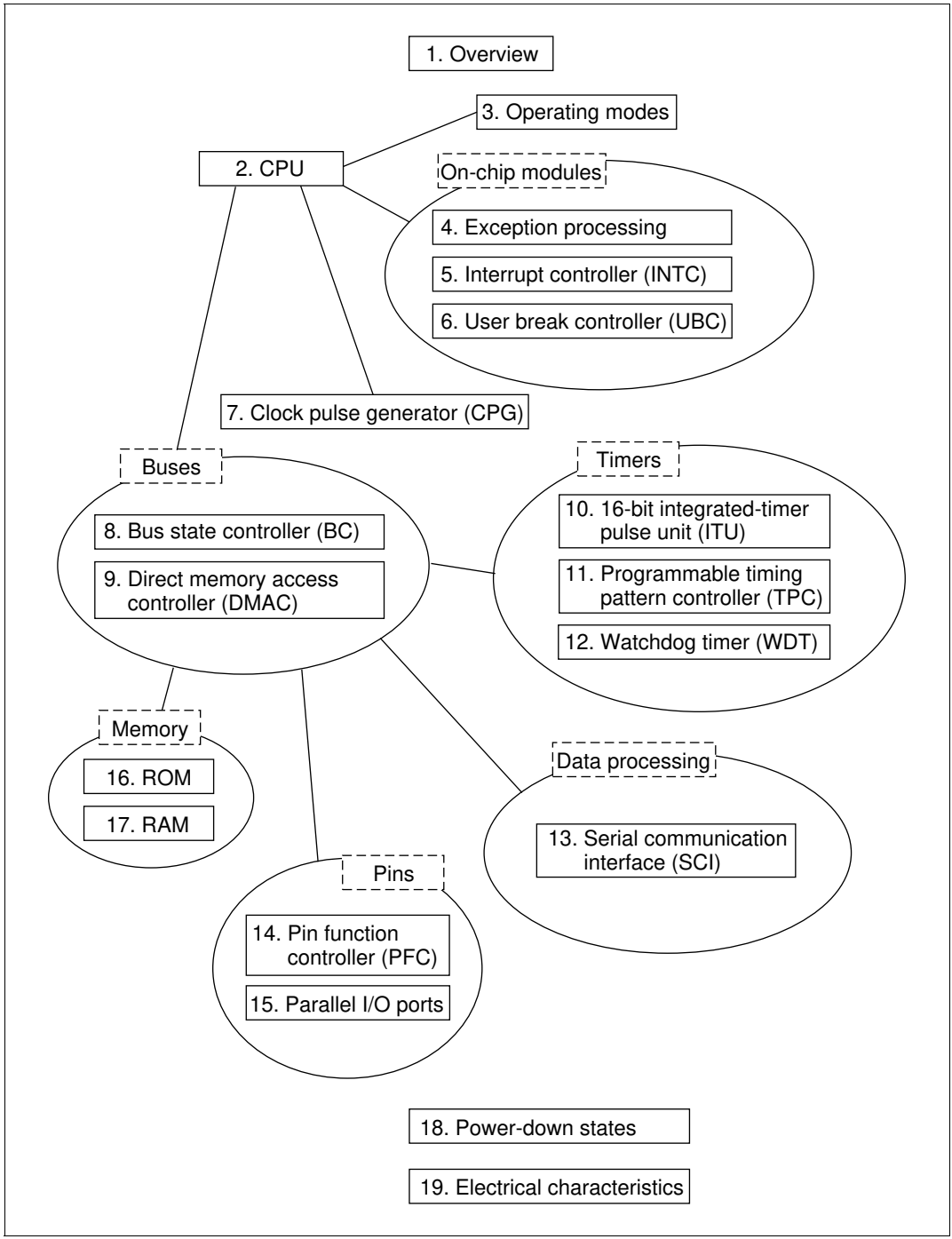
Table 1 describes how this manual is organized. Figure 1 shows the relationships between the Sections within this manual.

Table 1 Manual Organization

Category	Section Title	Abbreviation	Contents
Overview	1. Overview	—	Features, internal block diagram, pin layout, pin functions
CPU	2. CPU	CPU	Register configuration, data structure. instruction features, instruction types, instruction lists
Operating Modes	3. Operating Modes	—	MCU mode, PROM mode
Internal Modules	4. Exception Processing	—	Resets, address errors, interrupts, trap instructions, illegal instructions
	5. Interrupt Controller	INTC	NMI interrupts, user break interrupts, IRQ interrupts, on-chip module interrupts
	6. User Break Controller	UBC	Break address and break bus cycles selection
Clock	7. Clock Pulse Generator	CPG	Crystal pulse generator, duty correction circuit
Buses	8. Bus State Controller	BSC	Division of memory space, DRAM interface, refresh, wait state control, parity control
	9. Direct Memory Access Controller	DMAC	Auto request, external request, on-chip peripheral module request, cycle steal mode, burst mode
Timers	10. 16-Bit Integrated-Timer Pulse Unit	ITU	Waveform output mode, input capture function, counter clear function, buffer operation, PWM mode, complementary PWM mode, reset synchronized mode, synchronized operation, phase counting mode, compare match output mode
	11. Programmable Timing Pattern Controller	TPC	Compare match output triggers, non-overlap operation
	12. Watchdog Timer	WDT	Watchdog timer mode, interval timer mode
Data Processing	13. Serial Communication Interface	SCI	Asynchronous mode, clock synchronous mode, multiprocessor communication function

Table 1 Manual Organization (cont)

Category	Section Title	Abbreviation	Contents
Pins	14. Pin Function Controller	PFC	Pin function selection
	15. Parallel I/O Ports	I/O	I/O port
Memory	16. ROM	ROM	On-chip ROM
	17. RAM	RAM	On-chip RAM
Power-Down States	18. Power-Down States	—	Sleep mode, standby mode
Electrical Characteristics	19. Electrical Characteristics	—	Absolute maximum ratings, AC characteristics, DC characteristics, operation timing



Manual Organization Scheme

Addresses of On-Chip Peripheral Module Registers

The on-chip peripheral module registers are located in the on-chip peripheral module space (area 5: H'5000000–H'5FFFFFF), but since the actual register space is only 512 bytes, address bits A23–A9 are ignored. 32k shadow areas in 512 byte units that contain exactly the same contents as the actual registers are thus provided in the on-chip peripheral module space.

In this manual, register addresses are specified as though the on-chip peripheral module registers were in the 512 bytes H'5FFFE00–H'5FFFFFF. Only the values of the A27–A24 and A8–A0 bits are valid; the A23–A9 bits are ignored. When H'5000000–H'50001FF is accessed, for example, the result will be the same as when H'5FFFE00–H'5FFFFFF is accessed. For more details, see Section 8.3.5, Area Description: Area 5.

Free Addresses in the On-chip Peripheral Module Space (Area 5)

Avoid reading/writing from/to the free addresses without registers in the on-chip peripheral module space (area 5: H'5000000-H'5FFFFFF).

Contents

Section 1 Overview

1.1 SuperH Microcomputer Features

The SuperH microcomputer (SH7000 series) is a new generation reduced instruction set computer (RISC) in which a Hitachi-original CPU and the peripheral functions required for system configuration are integrated onto a single chip.

The CPU has a RISC-type instruction set. Most instructions can be executed in one clock cycle, which strikingly improves instruction execution speed. In addition, the CPU has a 32-bit internal architecture for enhanced data-processing ability. As a result, the CPU enables high-performance systems to be constructed with advanced functionality at low cost, even in applications such as realtime control that require very high speeds, an impossibility with conventional microcomputers.

The SH microcomputer includes peripheral functions such as large-capacity ROM, RAM, a direct memory access controller (DMAC), timers, a serial communication interface (SCI), an interrupt controller (INTC), and I/O ports. External memory access support functions enable direct connection to SRAM and DRAM. These features can drastically reduce system cost.

For on-chip ROM, masked ROM or electrically programmable ROM (PROM) can be selected. The PROM version can be programmed by users with a general-purpose EPROM programmer.

Table 1.1 lists the features of the SH microcomputers (SH7020 and SH7021).

Table 1.1 Features of the SH7020 and SH7021 Microcomputers

Feature	Description
CPU	Original Hitachi architecture
	32-bit internal data paths
	General-register machine: • Sixteen 32-bit general registers • Three 32-bit control registers • Four 32-bit system registers
	RISC-type instruction set: • Instruction length: 16-bit fixed length for improved code efficiency • Load-store architecture (basic arithmetic and logic operations are executed between registers) • Delayed unconditional branch instructions reduce pipeline disruption • Instruction set optimized for C language
	Instruction execution time: one instruction/cycle (50 ns/instruction at 20-MHz operation)
	Address space: 4 Gbytes available on the architecture
	On-chip multiplier: multiplication operations (16 bits × 16 bits → 32 bits) executed in 1–3 cycles, and multiplication/accumulation operations (16 bits × 16 bits + 42 bits → 42 bits) executed in 2–3 cycles
	Five-stage pipeline
Operating modes	Operating modes: • On-chip ROMless mode • On-chip ROM mode
	Processing states: • Power-on reset state • Manual reset state • Exception processing state • Program execution state • Power-down state • Bus-released state
	Power-down states: • Sleep mode • Software standby mode