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DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4000B gates

Dual 3-input NOR gate and inverter

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

The HEF4000B provides the positive dual 3-input NOR function. A single stage inverting function with standard output performance is also accomplished. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

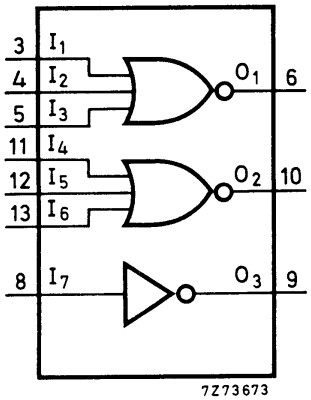


Fig.1 Functional diagram.

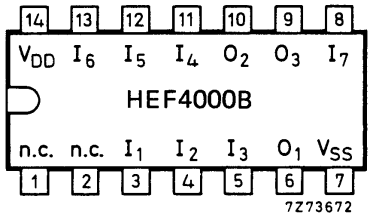


Fig.2 Pinning diagram.

HEF4000BP(N): 14-lead DIL; plastic (SOT27-1)

HEF4000BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4000BT(D): 14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

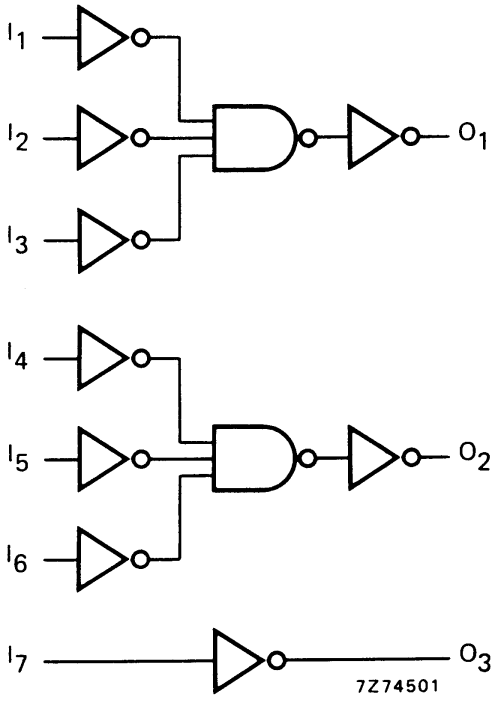


Fig.3 Logic diagram.

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

DC CHARACTERISTICS

For the single inverter stage (I_7/O_3):

see Family Specifications for input voltages HIGH and LOW (unbuffered stages only).

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays	5		70	140	ns	43 ns + (0,55 ns/pF) C_L
I_1 to $I_6 \rightarrow O_1, O_2$	10	t_{PHL}; t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
$I_7 \rightarrow O_3$	10	t_{PHL}; t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
(unbuffered output)	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$7\,700\ f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$28\,700\ f_i + \sum (f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

The following information (Figs 4 to 7) is only for the single inverter stage (I_7/O_3).

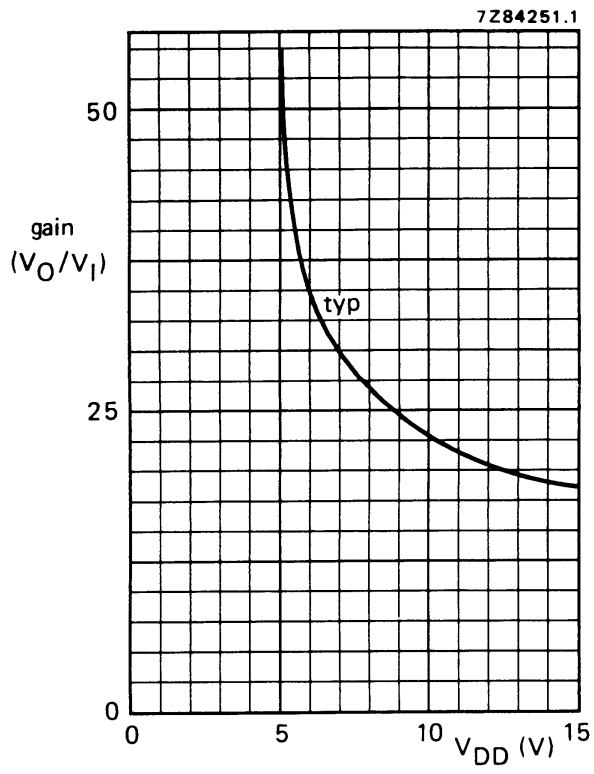


Fig.4 Voltage gain (V_O/V_I) as a function of supply voltage.

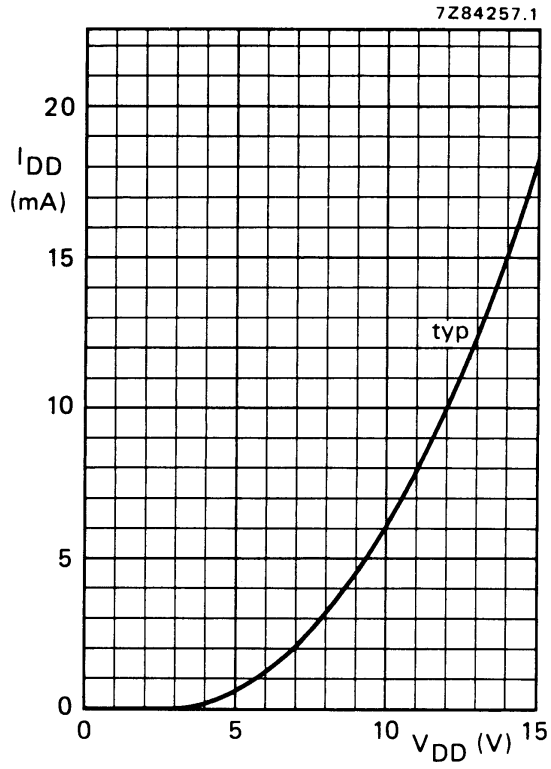


Fig.5 Supply current as a function of supply voltage.

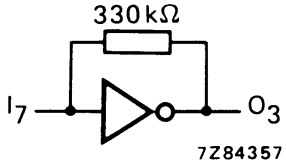


Fig.6 Test set-up for measuring graphs of Figs 4 and 5.

This is also an example of an analogue amplifier using the single inverter stage (I_7/O_3) of the HEF4000B.

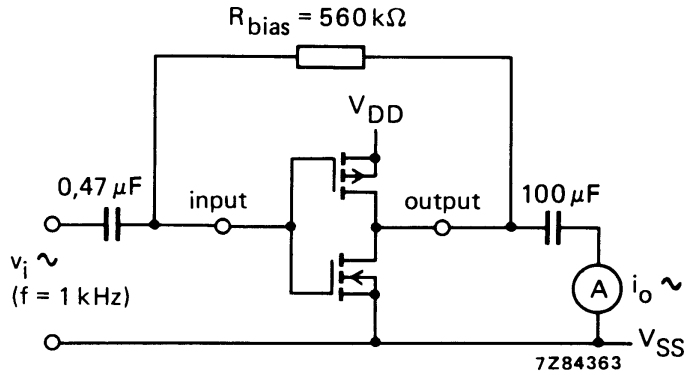
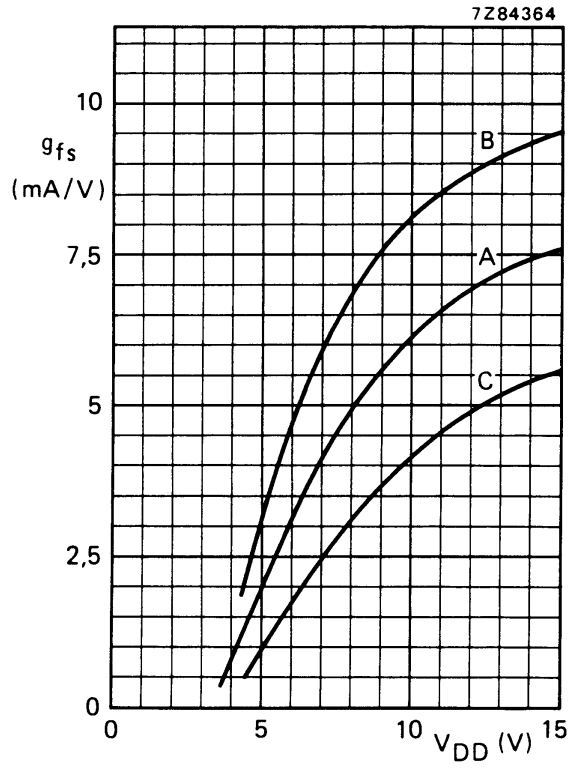


Fig.7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.8).



A: average
B: average + 2 s,
C: average − 2 s, in where 's' is the observed standard deviation.

Fig.8 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.