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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4025B

gates

Triple 3-input NOR gate

Product specification
File under Integrated Circuits, IC04

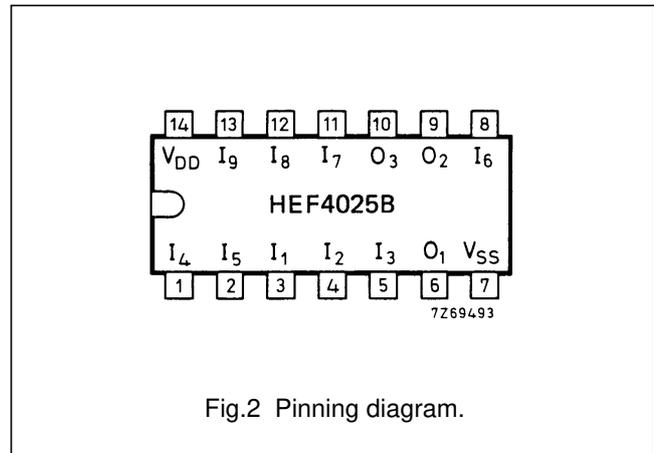
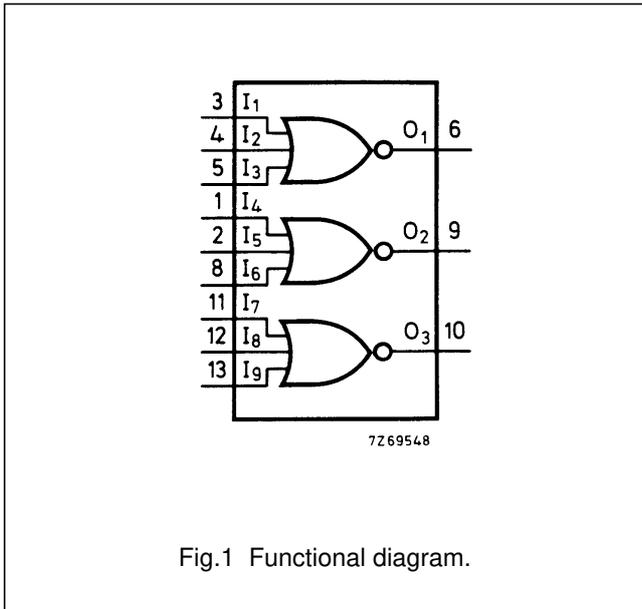
January 1995

Triple 3-input NOR gate

HEF4025B gates

DESCRIPTION

The HEF4025B provides the positive triple 3-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

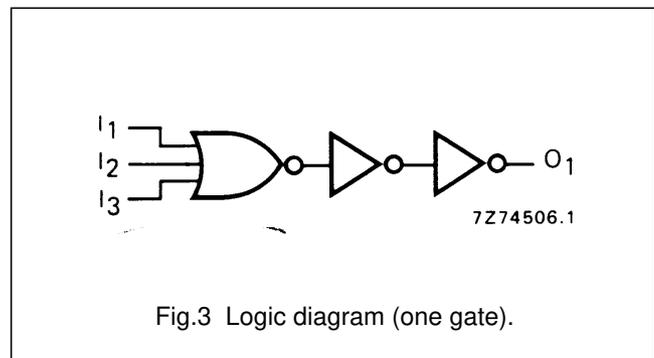


HEF4025BP(N): 14-lead DIL; plastic (SOT27-1)

HEF4025BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4025BT(D): 14-lead SO; plastic (SOT108-1)

(): Package Designator North America



FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

Triple 3-input NOR gate

HEF4025B
gates

AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	70	135	ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		25	55	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	60	120	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		15	35	ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$900 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$10\,900 f_i + \sum (f_o C_L) \times V_{DD}^2$	