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HEF4094B-Q100

8-stage shift-and-store register

Rev. 3 — 4 July 2013 | Product data sheet

1. General description

The HEF4094B-Q100 is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs QP0 to QP7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (OE) signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of HEF4094B-Q100 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading HEF4094B-Q100 devices when the clock has a slow rise time.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Connect unused inputs to V_{DD}, V_{SS}, or another input.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
  - MIL-STD-833, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +125 °C.

Type number	Package		
	Name	Description	Version
HEF4094BT-Q100	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4094BTT-Q100	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

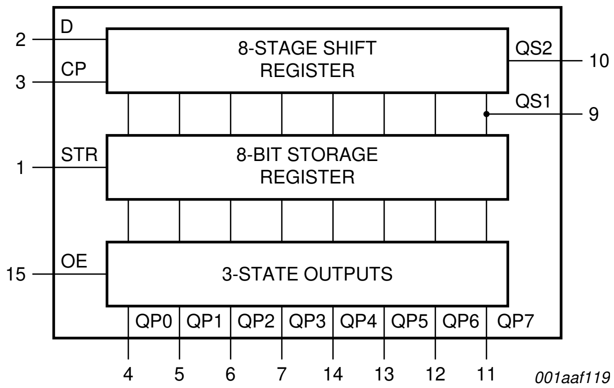


Fig 1. Functional diagram

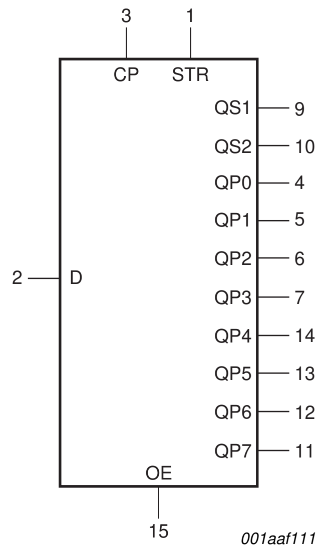


Fig 2. Logic symbol

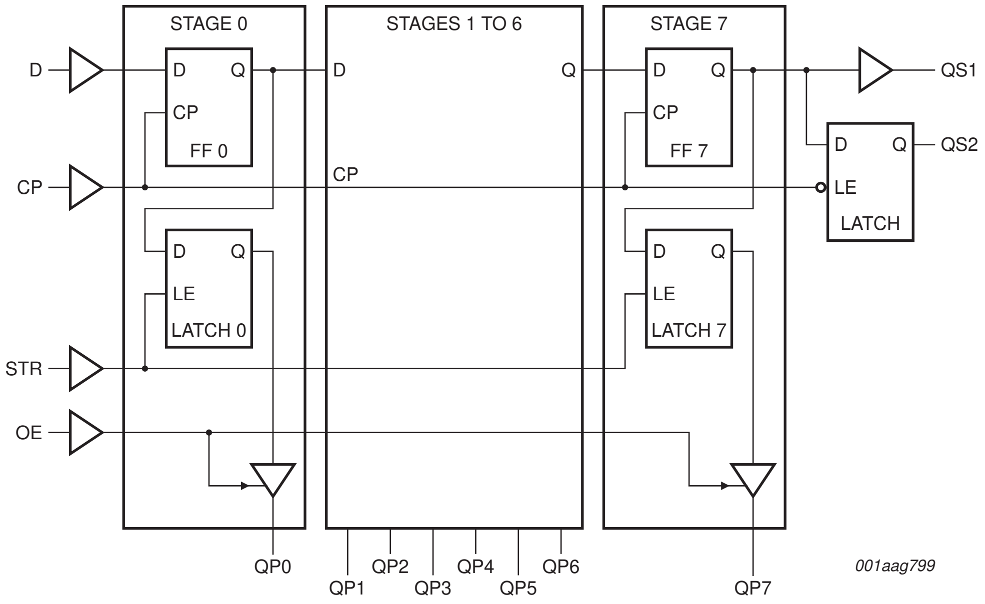


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

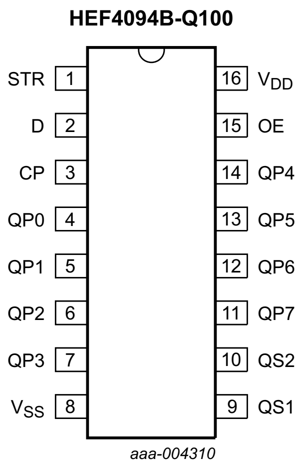


Fig 4. Pin configuration SOT109-1

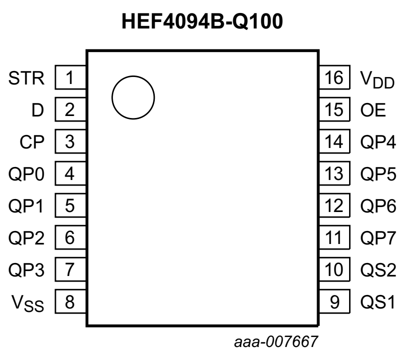


Fig 5. Pin configuration SOT403-1

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
STR	1	strobe input
D	2	data input
CP	3	clock input
QP0 to QP7	4, 5, 6, 7, 14, 13, 12, 11	parallel output
V_{SS}	8	ground supply voltage
QS1	9	serial output
QS2	10	serial output
OE	15	output enable input
V_{DD}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Inputs				Parallel outputs		Serial outputs	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn −1	Q6S	NC
↑	H	H	H	H	QPn −1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

[1] At the positive clock edge, the information in the 7th register stage is transferred to the 8th register stage and the QSn outputs.
H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = positive-going transition; ↓ = negative-going transition;
Z = HIGH-impedance OFF-state; NC = no change;
Q6S = the data in register stage 6 before the LOW to HIGH clock transition;
Q7S = the data in register stage 7 before the HIGH to LOW clock transition.

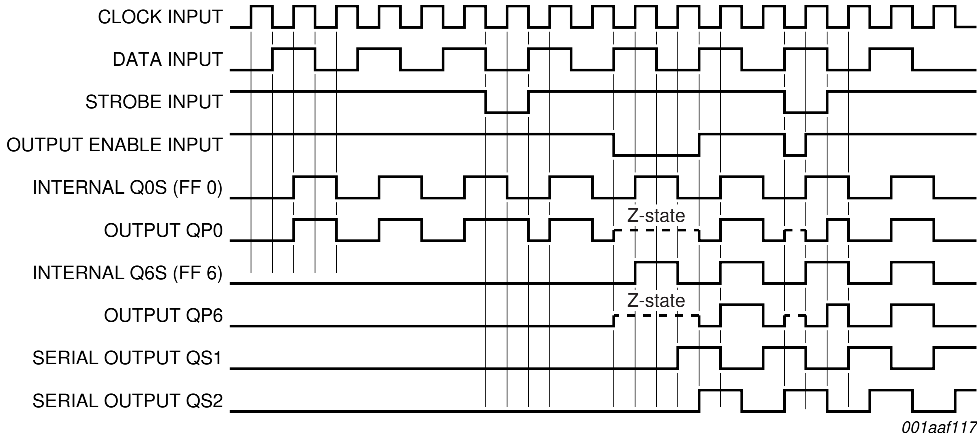


Fig 6. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+18	V
I_{IK}	input clamping current	V_I < –0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		–0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < –0.5 V or V_O > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+125	°C
P_{tot}	total power dissipation	[1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		T_{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	–1.7	-	–1.4	-	–1.1	-	–1.1	mA
		V_O = 4.6 V	5 V	-	–0.64	-	–0.5	-	–0.36	-	–0.36	mA
		V_O = 9.5 V	10 V	-	–1.6	-	–1.3	-	–0.9	-	–0.9	mA
		V_O = 13.5 V	15 V	-	–4.2	-	–3.4	-	–2.4	-	–2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_{OZ}	OFF-state output current	QPn output is HIGH; V_O = 15 V	15 V	-	0.4	-	0.4	-	12	-	12	μA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I_{DD}	supply current	all valid input combinations; I_O = 0 A	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C_I	input capacitance			-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 11; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP to QS1; see Figure 7	5 V	[1]	108 ns + (0.55 ns/pF)C_L	-	135	270	ns
			10 V		54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V		42 ns + (0.16 ns/pF)C_L	-	50	100	ns
		CP to QS2; see Figure 7	5 V		78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V		39 ns + (0.23 ns/pF)C_L	-	50	100	ns
			15 V		32 ns + (0.16 ns/pF)C_L	-	40	80	ns
		CP to QPn; see Figure 7	5 V		138 ns + (0.55 ns/pF)C_L	-	165	330	ns
			10 V		64 ns + (0.23 ns/pF)C_L	-	75	150	ns
			15 V		47 ns + (0.16 ns/pF)C_L	-	55	110	ns
		STR to QPn; see Figure 8	5 V		83 ns + (0.55 ns/pF)C_L	-	110	220	ns
			10 V		39 ns + (0.23 ns/pF)C_L	-	50	100	ns
			15 V		27 ns + (0.16 ns/pF)C_L	-	35	70	ns
t_{PLH}	LOW to HIGH propagation delay	CP to QS1; see Figure 7	5 V	[1]	78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V		39 ns + (0.23 ns/pF)C_L	-	50	100	ns
			15 V		32 ns + (0.16 ns/pF)C_L	-	40	80	ns
		CP to QS2; see Figure 7	5 V		78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V		39 ns + (0.23 ns/pF)C_L	-	50	100	ns
			15 V		32 ns + (0.16 ns/pF)C_L	-	40	80	ns
		CP to QPn; see Figure 7	5 V		123 ns + (0.55 ns/pF)C_L	-	150	300	ns
			10 V		59 ns + (0.23 ns/pF)C_L	-	70	140	ns
			15 V		47 ns + (0.16 ns/pF)C_L	-	55	110	ns
		STR to QPn; see Figure 8	5 V		73 ns + (0.55 ns/pF)C_L	-	100	200	ns
			10 V		34 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V		27 ns + (0.16 ns/pF)C_L	-	35	70	ns
t_t	transition time		5 V	[1]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V		9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V		6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{PZH}	OFF-state to HIGH propagation delay	OE to QPn; see Figure 9	5 V			-	40	80	ns
			10 V			-	25	50	ns
			15 V			-	20	40	ns
t_{PZL}	OFF-state to LOW propagation delay	OE to QPn; see Figure 9	5 V			-	40	80	ns
			10 V			-	25	50	ns
			15 V			-	20	40	ns
t_{PHZ}	HIGH to OFF-state propagation delay	OE to QPn; see Figure 9	5 V			-	75	150	ns
			10 V			-	40	80	ns
			15 V			-	30	60	ns

Table 7. Dynamic characteristics *...continued*

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 11; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{PLZ}	LOW to OFF-state propagation delay	OE to QPn; see Figure 9	5 V		-	80	160	ns
			10 V		-	40	80	ns
			15 V		-	30	60	ns
t_{su}	set-up time	D to CP; see Figure 10	5 V		60	30	-	ns
			10 V		20	10	-	ns
			15 V		15	5	-	ns
t_h	hold time	D to CP; see Figure 10	5 V		+5	−15	-	ns
			10 V		20	5	-	ns
			15 V		20	5	-	ns
t_W	pulse width	minimum LOW clock pulse; see Figure 7	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		minimum HIGH strobe pulse; see Figure 8	5 V		40	20	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
f_{max}	maximum frequency	see Figure 7	5 V		5	10	-	MHz
			10 V		11	22	-	MHz
			15 V		14	28	-	MHz

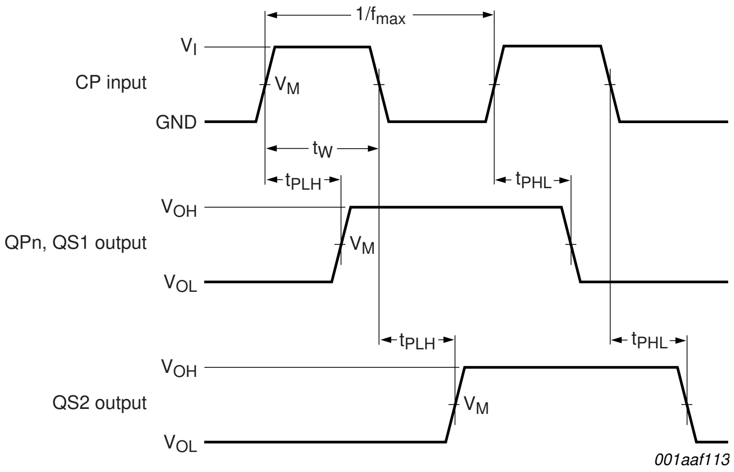
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation

V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 2100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 9700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 26000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

11. Waveforms



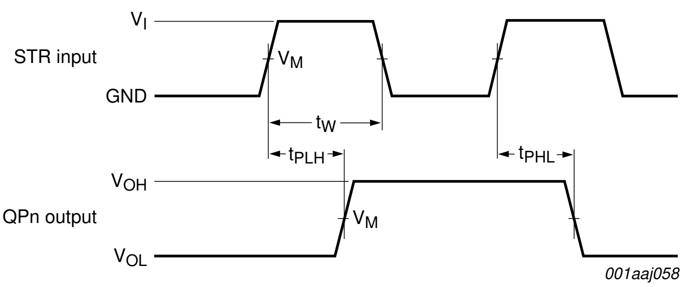
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Clock to outputs propagation delays, and clock pulse width and maximum frequency

Table 9. Measurement points

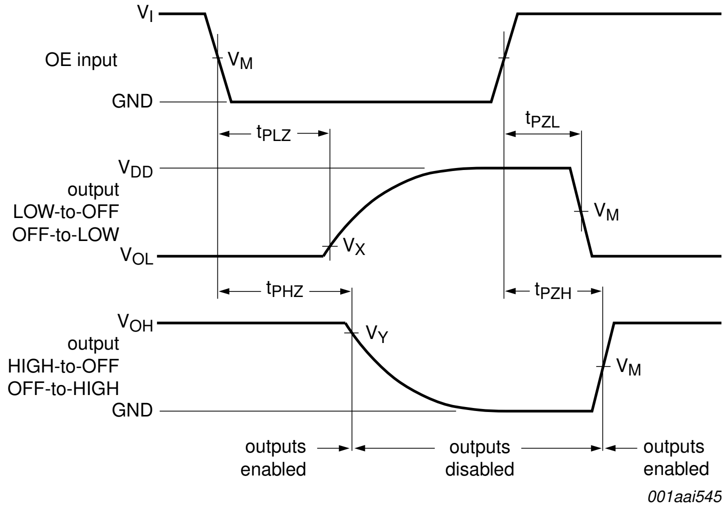
Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

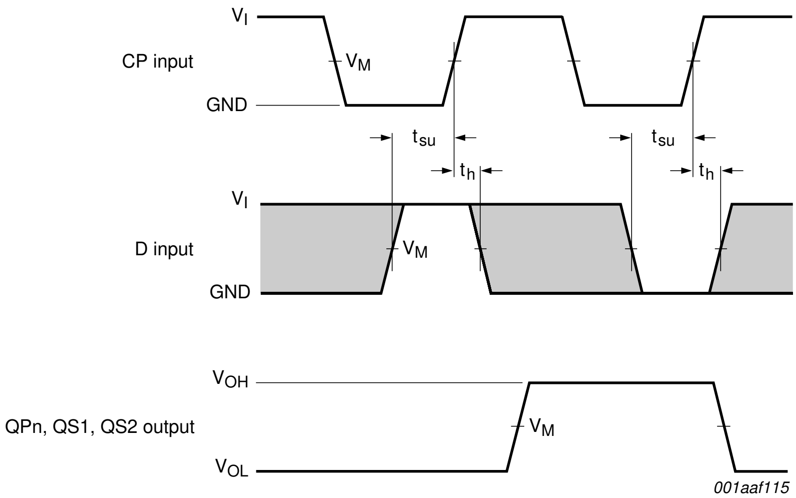
Fig 8. Strobe to output propagation delays, and strobe pulse width, set up and hold times



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

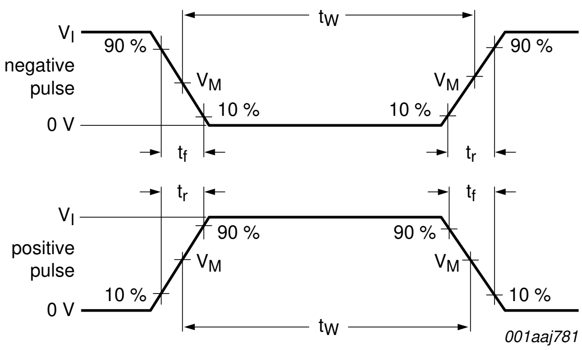
Fig 9. 3-state output enable and disable times for OE input



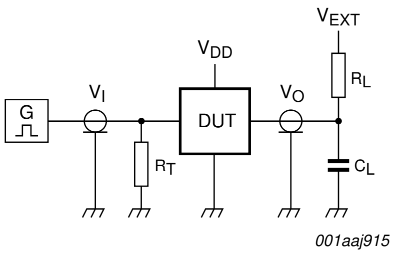
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Data input data set up and hold times



a. Input waveform



b. Test circuit

Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 11. Test circuit

Table 10. Test data

Supply voltage	Input		V_{EXT}			Load	
V_{DD}	V_I	t_r, t_f	t_{PHL}, t_{PLH}	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	C_L	R_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	open	V_{SS}	V_{DD}	50 pF	1 kΩ

12. Application information

Some examples of applications for the HEF4094B-Q100 are:

- Serial-to-parallel data conversion
- Remote control holding register

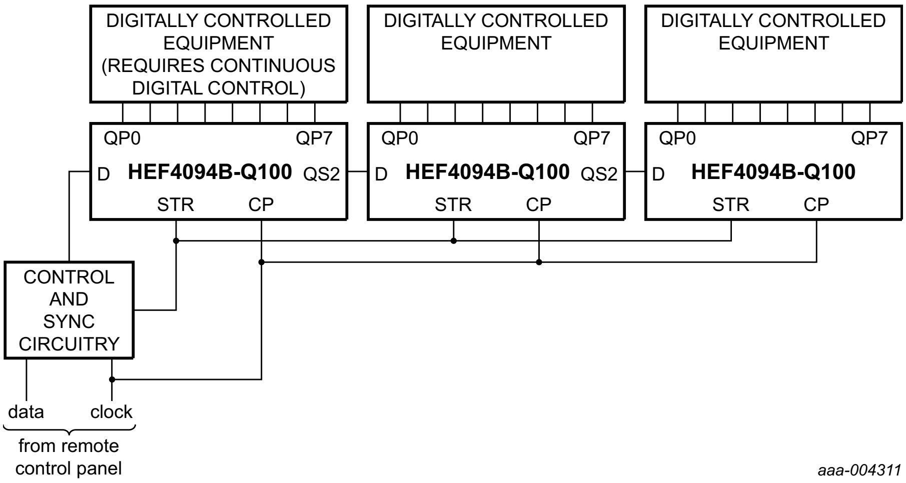
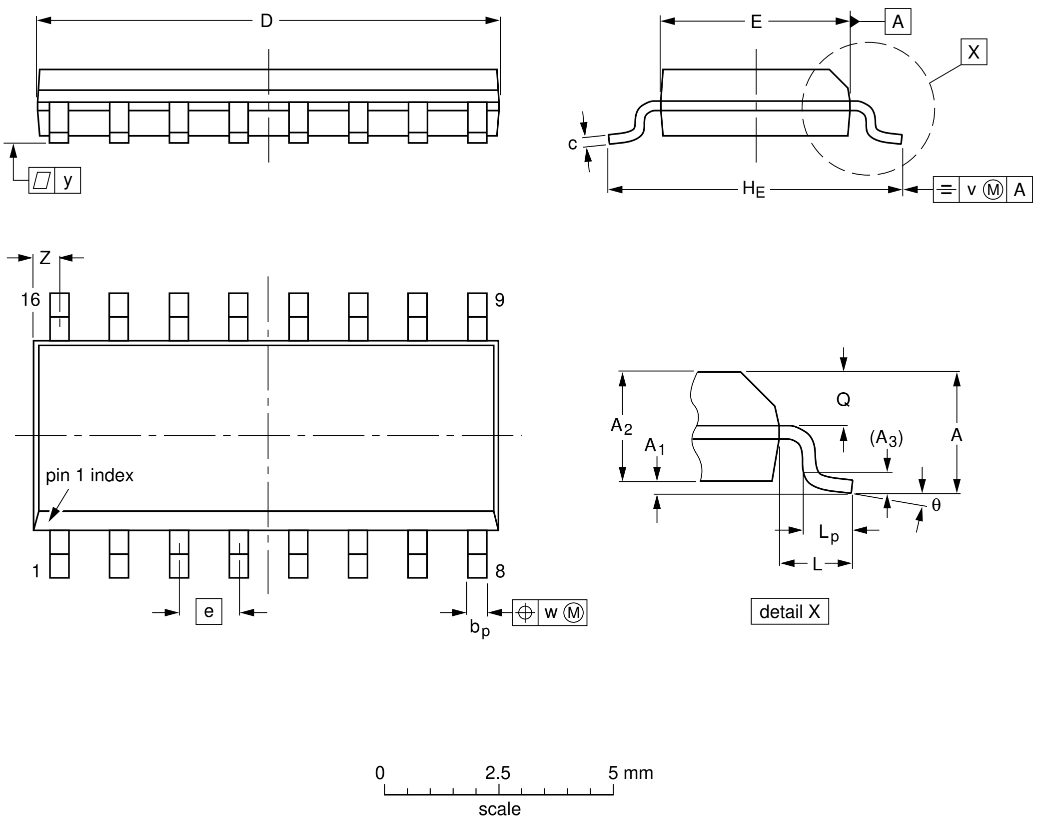


Fig 12. Remote control holding register

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

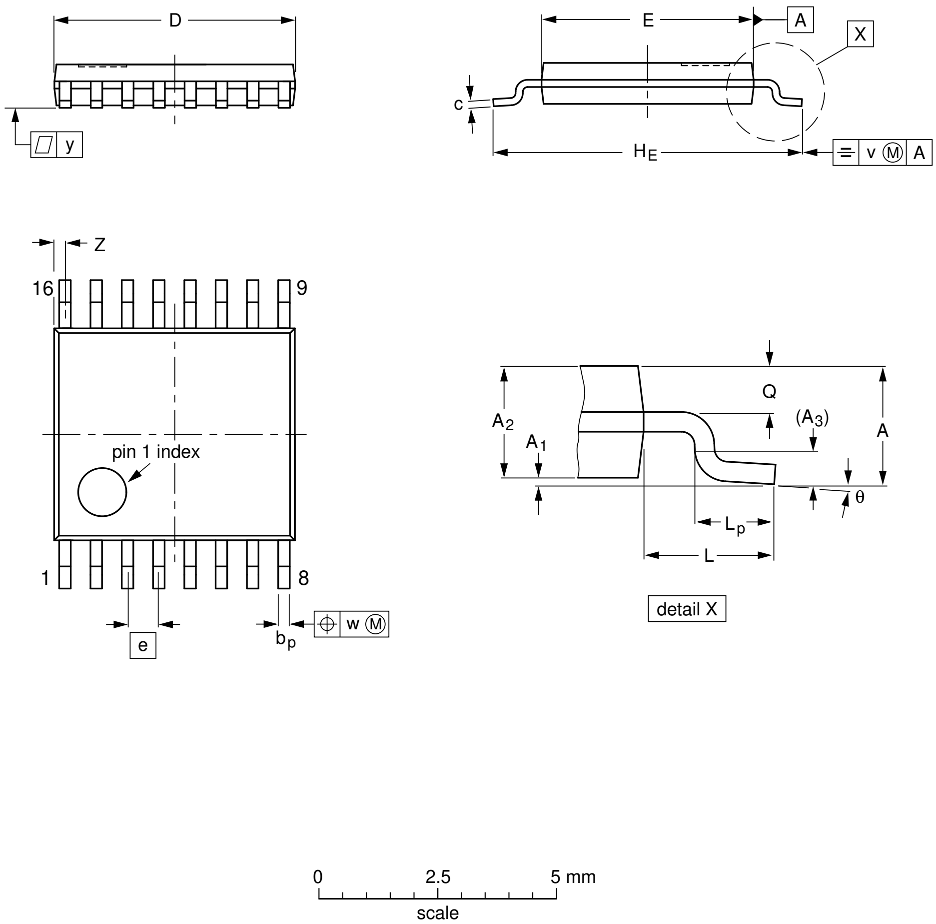
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

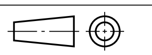
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
MIL	Military

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4094B_Q100 v.3	20130704	Product data sheet	-	HEF4094B_Q100 v.2
Modifications:	• Figure 3 corrected (errata).			
HEF4094B_Q100 v.2	20130606	Product data sheet	-	HEF4094B_Q100 v.1
Modifications:	• added type number HEF4094BTT-Q100.			
HEF4094B_Q100 v.1	20120807	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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