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HI-3110, HI-3111, HI-3112, HI-3113

Avionics CAN Controller with Integrated Transceiver

February 2017

GENERAL DESCRIPTION

The HI-3110 is a standalone Controller Area Network (CAN) controller with built in transceiver. The device provides a complete, integrated, cost-effective solution for avionics applications implementing the CAN 2.0B specification and can be configured to comply with both the ARINC 825 (General Standardization of CAN Bus Protocol for Airborne Use) and CANaerospace standards. The HI-3110 is capable of transmitting and receiving standard data frames, extended data frames and remote frames. The internal transceiver allows direct connection to the CAN bus without using external components and coupled with the host Serial Peripheral Interface (SPI), results in minimal board space.

The HI-3110 provides the optimum solution for applications where minimum host (MCU) overhead is required, filtering unwanted messages using a maskable identifier filter and storing up to 8 messages in the receive FIFO. A flexible interrupt scheme allows real time servicing of the FIFO by the host, if required. Transmissions are handled using an 8 message transmit FIFO. A Transmit Enable pin can be used by the host to initiate a transmission. The device also provides monitor or listen-only mode, low power sleep mode, loopback mode for self-test and a re-transmission disable capability (necessary to implement TTCAN protocol).

The HI-3111 is a digital only version of the HI-3110 (no transceiver). This version provides a “protocol only” solution for customers who wish to use an external transceiver and may be used in situations where the customer requires galvanic isolation between the bus and digital protocol logic. The HI-3112 provides an option of a CLKOUT pin instead of a SPLIT pin, which may be used as the main system clock or as a clock input for other devices in the system. Finally, the HI-3113 provides all options (both CLKOUT and SPLIT pins) in a very compact QFN-44 package.

The HI-3110 family is available in industrial and full extended temperature ranges, with a “RoHS compliant” lead-free option. The design has been independently validated by C&S group, GmbH, an ISO/IEC 17025 accredited test house. A copy of the test report is available from Holt on request.

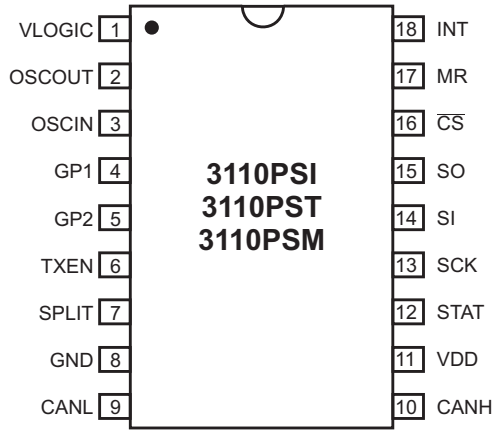
FEATURES

- Implements CAN version 2.0B with programmable bit rate up to 1Mbit/sec. ISO 11898-5 compliant.
- Configurable to support ARINC 825 and CANaerospace Standards.
- Serial Peripheral Interface (SPI) (20MHz).
- Standard, Extended and Remote frames supported.
- 8 maskable identifier filters.
- Filtering on ID and first two data bytes for both Standard and Extended Identifiers.
- Loopback mode for self-test.
- Monitor (Listen-only) and Low Power Sleep Modes with automatic wake-up possible.
- 8-message Transmit and Receive FIFOs.
- Internal 16-bit free running counter for time tagging of transmitted or received messages.
- Permanent dominant timeout protection.
- Short Circuit Protection of -58V to + 58V on CAN_H, CAN_L and SPLIT pins (ISO 11898-5).
- Re-transmission disable capability.
- Transmit Enable pin.
- Industrial and Full Extended temperature ranges supported:

  Industrial: -40°C to + 85°C.

  Extended: -55°C to + 125°C.

PIN CONFIGURATION (Top View)



18-Pin Plastic SOIC - WB Package

BLOCK DIAGRAM

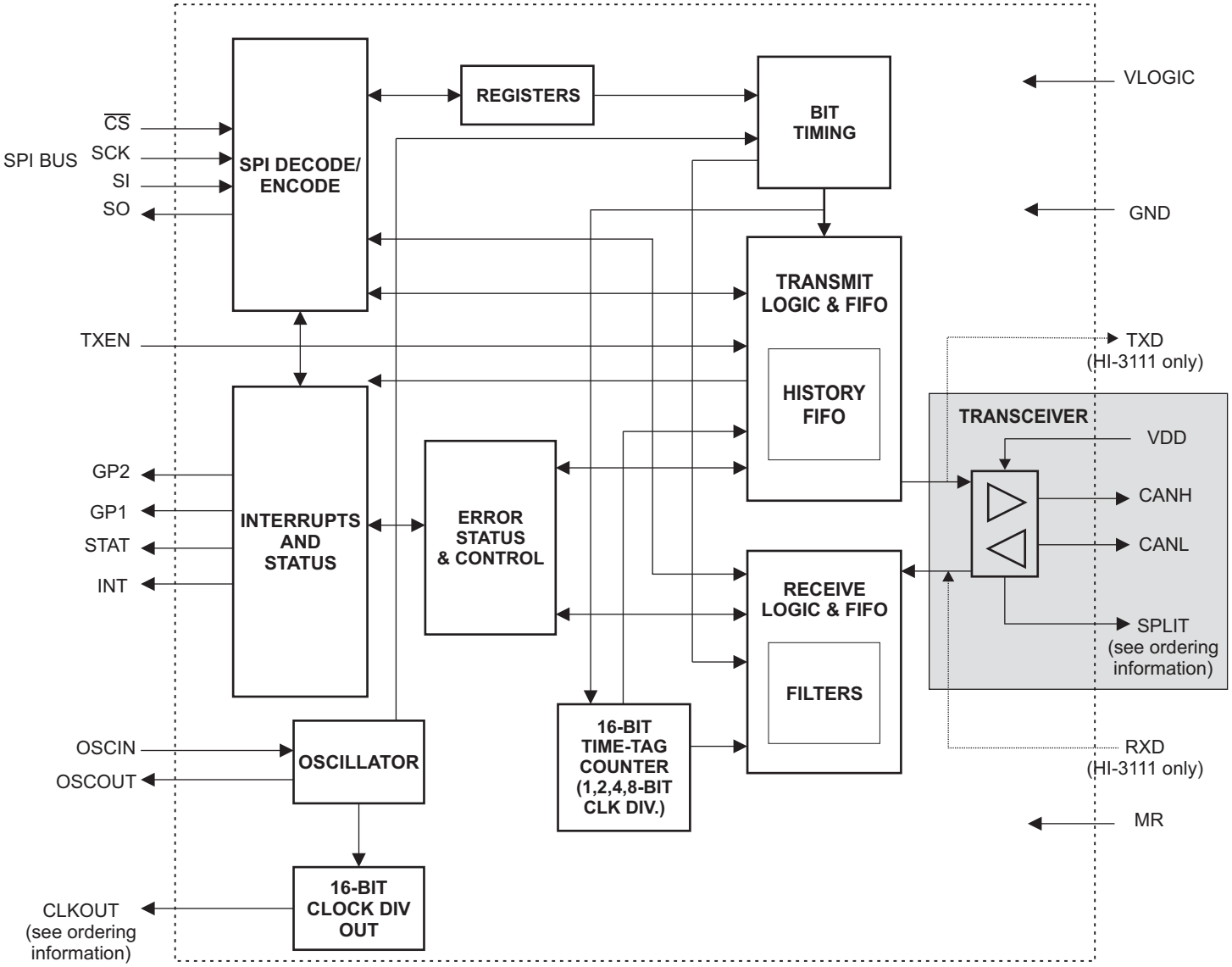


Figure 1. Block Diagram

PRIMARY FUNCTIONS OF HI-3110 LOGIC BLOCKS

SPI PROTOCOL BLOCK
Handles data transfers between the host and the chip

REGISTERS BLOCK
Stores configuration data

BIT TIMING BLOCK
Sets the data strobe and bit period

TRANSMIT BLOCK
Manages transmission protocol
8 message FIFO
Confirmation and time stamp of each message sent is available in the History FIFO

RECEIVER BLOCK
Manages reception protocol
8 message FIFO with optional filters
Forwards message data and optional time stamp to the host

ERROR BLOCK
Detects and records errors for protocol management

STATUS AND INTERRUPT
Provides hardware and software options for managing communications

OSCILLATOR
Configuration chooses either the crystal oscillator or and external clock

TRANSCEIVER
Analog interface connects directly to the CAN bus

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION	NOTES
SCK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK	50K ohm pull-down
$\overline{CS}$	INPUT	Chip Select. Data is shifted into SI and out of SO when $\overline{CS}$ is low.	50K ohm pull-up
SI	INPUT	SPI interface serial data input	50K ohm pull-down
SO	OUTPUT	SPI interface serial data output	
INT	OUTPUT	Active high. Programmable interrupt output	
STAT	OUTPUT	Active high. Programmable status output.	
TXEN	INPUT	Active high. Transmit Enable pin. When the TXEN pin is asserted, any message in the Transmit FIFO will be automatically loaded to the Transmit buffer and sent if the bus is available. This pin is logically ORed with the TXEN and TX1M bits in the CTRL1 register. When the TXEN pin is reset, messages loaded to the FIFO will not be sent until TXEN or TX1M bits are set in the CTRL1 register.	100K ohm pull-down
OSCIN	INPUT	Crystal input. A parallel resonant crystal can be connected between OSCIN and OSCOUT. If an external clock is used, it should be connected to the OSCIN pin and the OSCOUT pin should be left floating. The internal oscillator should be shut off by setting the OSCOFF bit in the CTRL1 register.	
OSCOUT	OUTPUT	Crystal output. If an external clock is used, this pin should be left floating and disabled by setting the OSCOFF bit in the CTRL1 register.	
GP1	OUTPUT	General purpose pin 1, which can be programmed to reflect the values of interrupt and status flag bits.	
GP2	OUTPUT	General purpose pin 2, which can be programmed to reflect the values of interrupt and status flag bits.	
CLKOUT	OUTPUT	Clock output pin with programmable frequency divider.	
SPLIT	OUTPUT	VDD/2 output bias (Powered off in Sleep Mode and when the common mode bias is greater than 25V).	
CANH	BUS I/O	CAN bus line high.	
CANL	BUS I/O	CAN bus line low.	
TXD	OUTPUT	Transmit Data Out. Connect to TXD input pin on CAN transceiver (e.g. HI-3000).	HI-3111 only
RXD	INPUT	Receive Data In. Connect to RXD output pin on CAN transceiver (e.g. HI-3000).	HI-3111 only 5V Logic Tolerant
MR	INPUT	Active High. Device Master Reset input pin. Asserting this pin resets all registers and memory buffers to their default state at start-up.	50K ohm pull-down
VDD	POWER	5V supply voltage input.	
VLOGIC	POWER	3.3V supply voltage input. This supply is used to drive the host digital logic I/O. It can either be connected directly to VDD (+5V) or a +3.3V supply.	
GND	POWER	Supply voltage ground.	

FUNCTIONAL OVERVIEW

The HI-3110 is the first single chip product to integrate both the CAN (Controller Area Network) protocol and analog interface transceiver on a single IC. The protocol conforms to CAN version 2.0B and is compliant with ISO 11898-1:2003(E) specification. The transceiver is compliant with ISO 11898-5 specification.

Configuration options include an internal Loopback mode that does not disturb the bus, a Monitor only mode, and a Sleep mode that includes an option to either wake up automatically when data is present on the bus, or by host command. The following sections describe some of the key features.

SPI and REGISTERS

To minimize the footprint, a 20 MHz standard four wire SPI (Serial Peripheral Interface) is provided to manage the flow of data between the host microcontroller and the HI-3110. Complete messages are loaded and retrieved with single SPI op codes. On the receive side, SPI op code options may be used to retrieve the whole message or just the data. An option to include a time tag or no time tag may also be specified. On the transmit side, each message can be assigned an identifier which allows monitoring of the Transmit History FIFO to confirm the successful completion of a transmission along with the time stamp. In addition the transmitter logic automatically assembles the message frame based on the data presented.

BIT TIMING

Bit timing is controlled with standard CAN options. These include control of the Resychronization Jump Width (SJW), Prop delay Phase Seg 1 (TSeg1), Phase Seg 2 (TSeg2), the number of samples, and the derivation of Tq from the system clock using a prescaler. The maximum bit rate is 1 MBit/sec. Upon reset, the chip automatically enters Initialization mode which allows programming of the Bit Timing before entering Normal mode.

TRANSMITTER

The transmitter state machine automatically handles all CAN 2.0B protocol requirements. Messages for transmission are first loaded into a FIFO and transmission may start upon availability of data in the FIFO. Assertion of the TXEN pin or configuration bits in Control Register 1 allow either continuous transmission until the FIFO is empty or only one message from the FIFO at a time. One shot (no retry) transmission may also be enabled by setting the OSM and TX1M bits. SPI op codes are provided to clear the Transmit FIFO and to abort transmission.

RECEIVER

The receiver state machine automatically handles all CAN 2.0B protocol requirements. The receiver supports eight sets of filters and masks and each allows filtering of a full CAN ID (extended or not) and two bytes of data. Even when filtering is enabled, message data is always accessible as received via the Temporary Receive Buffer, and retrievable by SPI op codes 0x42 and 0x44.

If the Filter/Mask option is set (FILTON bit in Control Register 1), only messages that match one of the 8 stored data patterns are passed into the FIFO. Note that the Mask option allows certain bits of the programmed filter bits to be “don't care.” If the Filter/Mask option is not set, then all valid messages are passed to the FIFO. When the FIFO is full (8 completed messages received), the next received message is not loaded in the FIFO.

ERROR CONTROL

Errors are detected per ISO 11898-1:2003(E) and detections are counted and used by the protocol state machines. Active, Passive, and Bus Off conditions are managed per the CAN standard. A configuration bit is provided to allow automatic recovery from Bus Off.

STATUS and INTERRUPTS

The Message Status Register, MESSTAT, provides information about the current state of the receiver and transmitter operation. In addition, the Interrupt Flag Register, INTF, monitors 8 operational conditions, any or all of which may be directed to the INT pin by enabling bits in the Interrupt Enable Register, INTE. Similarly, the Status Flag Register, STATF, bits reflect the status of selected FIFO and Error properties. Any or all of these conditions may be directed to the STAT pin by setting the enable bits in the Status Flag Enable Register, STATFE.

To provide additional hardwired flag options, the GP1 and GP2 pins may also be programmed to reflect any of the Interrupt or Status Flag bits.

OSCILLATOR and TIME TAG

A configuration bit allows a choice for the source of the system clock. Either the on-board crystal oscillator may be selected or an external clock may be provided at the OSCIN pin.

On product versions with the CLKOUT pin, a programmable division of the system clock is provided. The clock source for the 16 bit Time Tag Counter is derived from a separate programmable division of the system clock. SPI op codes provide for reading and resetting the Time Tag Counter.

TRANSCEIVER

The HI-3110 contains an integrated transceiver operating

from 5V and the line driver is capable of maintaining a detectable signal for bus lengths well in excess of recommended CAN 2.0B standards. The digital logic and IO can be powered from 3.3V or 5V.

PROTECTION FEATURES

The BUS and SPLIT pins are protected against ESD to over 4KV (HBM) and from shorts between -58V to +58V continuous, as specified in ISO 11898-5.

In addition, a Permanent Dominant Timeout protection is implemented by means of an independent counter monitoring the dominant transmission state and automatically shutting off the transmission if it exceeds typically 2ms.

MODES OF OPERATION

The HI-3110 supports five modes of operation, namely, Initialization Mode, Normal Mode, Loopback Mode, Monitor Mode and Sleep Mode.

INITIALIZATION MODE

Initialization mode is used to configure the device before normal operation. **Bit timing registers and acceptance filters and masks can only be modified in this mode.** Initialization mode is the default mode following RESET and can also be activated by programming the MODE<2:0> bits to <1xx> in the CTRL0 register. Switching to Initialization mode resets the receiver and transmitter. During initialization mode, the error counters are held reset.

NORMAL MODE

Normal mode is the standard operating mode of the HI-3110. In this mode, the HI-3110 can transmit, receive and acknowledge messages from the CAN bus, handling all aspects of the CAN protocol. Normal mode is activated by programming the MODE<2:0> bits to <000> in the CTRL0 register.

LOOPBACK MODE

Loopback mode is used for self-test. The transceiver digital input is fed back to the receiver without being transmitted to the bus. Messages are transmitted from the transmit FIFO in the usual way and received by the receive FIFO as if they were received from a remote node on the bus.

Acceptance filters can be set up to accept or reject specific messages into the FIFO and all interrupt flags are set as required in the usual way. While in this mode, any bus activity is ignored. Loopback is activated by programming the MODE<2:0> bits to <001> in the CTRL0 register.

MONITOR MODE

Monitor mode (also known as listen-only or silent mode) allows the HI-3110 to monitor all bus activity without disturbing the bus. No messages or dominant bits (such as ACK or active error frame bits) are transmitted to the bus while in this mode. Also, the error counters are reset and deactivated. Messages from the bus are received in the same way as Normal Mode and messages that are not acknowledged by another node on the bus are ignored i.e. any frame containing an error will be ignored. Acceptance filters can be set up to reject or accept specific messages into the FIFO and all interrupt flags are set as required in the usual way. Monitor mode is activated by programming the MODE<2:0> bits to <010> in the CTRL0 register.

SLEEP MODE

The HI-3110 can be placed in a low power sleep mode if there is no bus activity and the transmit FIFO is empty. In this mode, the internal oscillator and all analog circuitry (transceiver) are off, drawing typically less than 20μA. Note that the SPI bus is active during sleep mode, so it is possible for the host to communicate with the HI-3110 while it is asleep (e.g. load transmit FIFO). Sleep mode is exited by selecting an alternative mode of operation, or automatic wake up following bus activity can be enabled by setting the WAKEUP bit in the CTRL0 register - in this case a low power receiver monitors the bus for a detectable dominant bit.. The device will wake up in Monitor Mode. Note that it will take a finite time for the oscillator and analog circuitry to come back on line. Since the internal oscillator takes a finite time to wake up, the message which caused the wake-up may not be stored.

Sleep mode is activated by programming the MODE<2:0> bits to <011> in the CTRL0 register. However, the actual mode change will only occur whenever the CAN bus is quiet. If the chip is transmitting, the mode change is delayed until the transmission is complete. If there is bus activity, the mode change is delayed until the receiver protocol control detects an inter-message gap.

CAN PROTOCOL OVERVIEW

The HI-3110 supports Standard, Extended and Remote Frames, as defined in the CAN specification IS0 11898-1:2003(E) (also known as CAN 2.0B).

BIT ENCODING

CAN frames are encoded according to the Non-Return-To-Zero (NRZ) method with bit stuffing. NRZ means that the generated bit level is constant during the total bit time and consecutive bits do not return to a neutral or rest condition.

This means that a bit stream of “1s” or “0”s appears continuous on the bus. A logic “0” is called a dominant bit and a logic “1” is called a recessive bit.

Bit stuffing is used to ensure frequent enough transitions occur to achieve synchronization. Every time a transmitter detects five consecutive bits of the same polarity in the bit stream to be transmitted, it inserts a bit of opposite polarity into the actual transmitted bit stream.

This bit stuffing rule applies to the Start-of-Frame field, arbitration field, control field, data field and CRC sequence. The CRC delimiter, ACK field and End-Of-Frame fields are of fixed form and not stuffed (see below for definition of these fields). Furthermore, Error frames and Overload frames are also of fixed form and not stuffed.

An example of how the bits in a stuffed bit stream might look is shown below.

00101011111**O**0000**I**1100000**I**11000

0 = dominant bit, **O** = dominant stuffed bit.
1 = recessive bit, **I** = recessive stuffed bit.

MESSAGE FRAMES

STANDARD DATA FRAME

The standard data frame is shown in figure 2. The frame starts with a Start-of-Frame (SOF) bit. This is a dominant bit that identifies the start of the data frame on the bus.

The SOF is followed by the 12-bit arbitration field. The arbitration field consists of an 11-bit identifer, ID28 - ID18, and the Remote Transmission Request (RTR) bit. The RTR bit is used to distinguish between a data frame (RTR bit dominant, logic 0) and a remote frame (RTR bit recessive, logic 1).

Following the arbitration field is the 6-bit control field. The first bit of the control field is the Identifier Extension flag bit (IDE). This is used to distinguish between standard and extended identifiers and must be dominant (logic 0) for standard data frames. The next bit, r0, is specified by the CAN protocol as a reserved bit for future expansion. This bit must be transmitted dominant, but receivers must be capable of receiving either a dominant or recessive bit. The final 4 bits of the control field make up the data length code (DLC). The binary value of this 4-bit field specifies the number of data bytes in the data payload (0 - 8 bytes). **Note:** All binary combinations greater than or equal to <1 0 0 0> specify 8 bytes of data.

After the control field is the data field, which contains a data payload equal to the number of bytes specified by the DLC (see note above).

The data field is followed by the 16-bit Cyclic Redundancy Check (CRC) field. This is used to check transmission errors by computing a 15-bit CRC sequence from the previous bit stream (SOF, arbitration field, control field and data field, excluding stuff bits). The last bit in the CRC field is the CRC delimiter bit (always recessive).

After the CRC field is the Acknowledge Field (ACK Field). The first bit is the ACK Slot bit. A transmitting node sends a recessive bit (logic 1) during the ACK slot. Any node which receives the message error-free acknowledges the reception by placing a dominant bit (logic 0) in the ACK slot, over-writing the recessive bit of the transmitter. The final bit in the ACK field is a recessive ACK delimiter bit. Therefore, the dominant ACK slot bit is surrounded on each side by a recessive bit.

Each data frame is delimited by an End-Of-Frame field (EOF). The EOF consists of seven recessive bits.

Following the EOF, there is a gap to the next frame called the Interframe Space (IFS) . The IFS consists of two bit fields, Intermission and Bus-Idle. The Intermission consists of three recessive bits, however the following notes apply:
a) detection of a dominant bit on the bus at the third slot is interpreted as a SOF,
b) detection of a dominant bit in either the first or second slots results in generation of an overload frame (see below).

The bus idle period is of arbitrary length and consists of recessive bits. A dominant bit detected during this period is interpreted as a SOF.

EXTENDED DATA FRAME

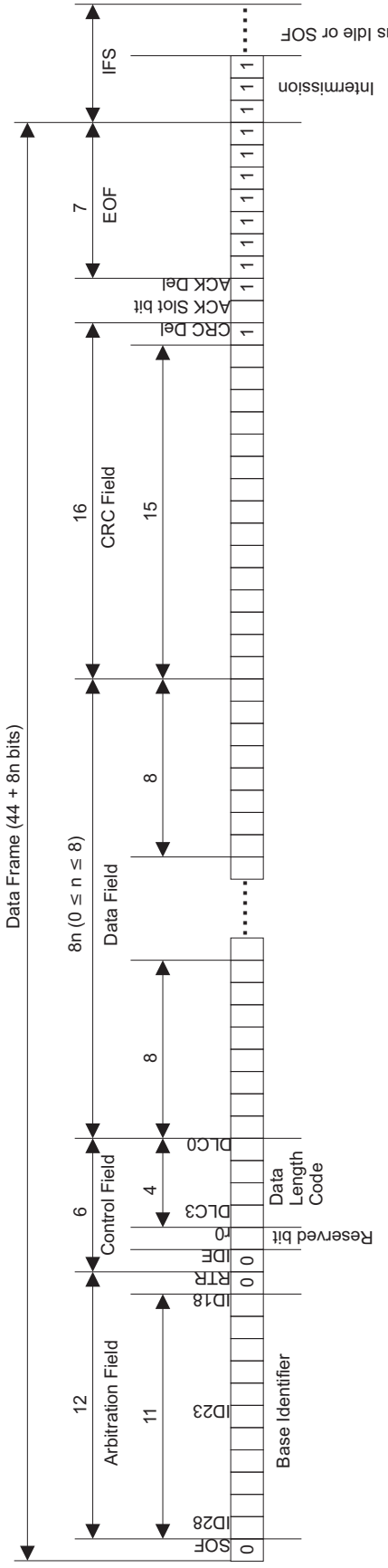
The extended data frame is shown in figure 3. In this frame format, SOF is followed by a 32-bit arbitration field consisting of a 29-bit identifier, ID28 - ID0. The first 11 most significant bits of the ID are know as the base identifier. This is followed by the Substitute Remote Request (SRR) bit, which is defined as recessive. Following the SRR bit is the IDE bit, which is defined as recessive for extended data frames. Note that the SRR bit is in the same slot as the RTR bit of the standard frame and the IDE bits are also in corresponding slots. This means if standard and extended identifier data frames with identical base identifiers are transmitted simultaneously, the standard identifier data frame will win arbitration (see Bitwise Arbitration section below).

The SRR and IDE bits are followed by the remaining 18 bits of the identifier (extended ID) and the last bit of the arbitration field is the RTR bit. The RTR bit has the same function as in the standard frame format.

Following the arbitration field is the 6-bit control field. The first two bits, r1 and r0, are specified by the CAN protocol as reserved bits for future expansion. Both these bits must be transmitted dominant, but receivers must be able to receive all combinations of dominant or recessive bits. The final 4 bits of the control field is the data length code (DLC). The binary value of this 4-bit field specifies the number of data bytes in the data payload (0 - 8 bytes). **Note:** All binary

combinations greater than or equal to <1 0 0 0> specify 8 bytes of data.

Standard Data Frame

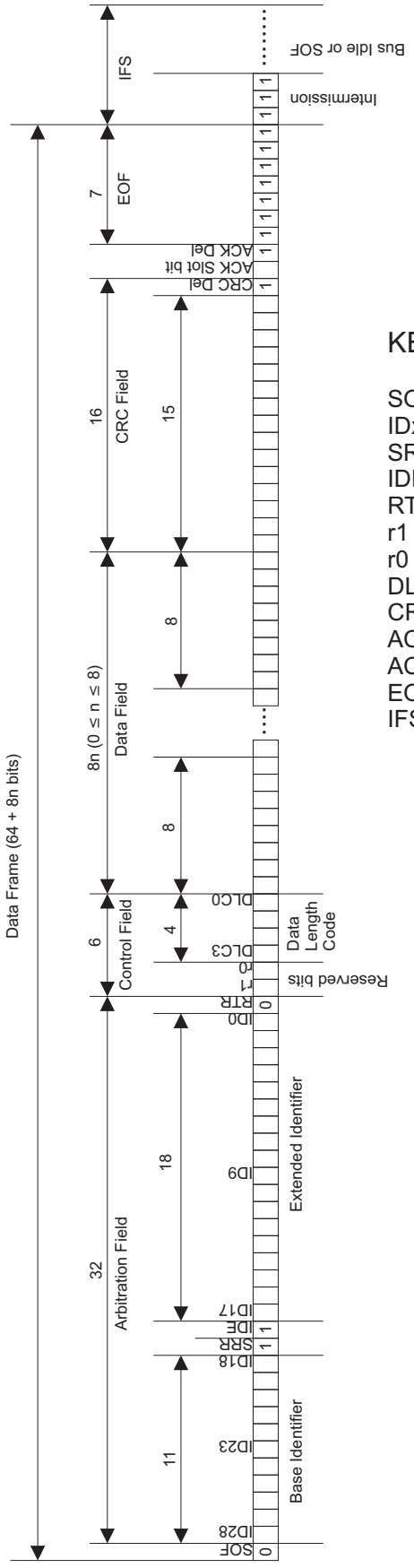


KEY.

SOF	Start-Of-Frame
IDxx	Identifier bit xx
RTR	Remote Transmission Request bit
IDE	Identifier Extension Flag
r0	Reserved bit 0
DLCx	Data Length Code bit x
CRC Del	Cyclic Redundancy Check Delimiter
ACK Slot bit	Acknowledge Slot bit
ACK Del	Acknowledge Delimiter
EOF	End-Of-Frame
IFS	Interframe space

Figure 2. Standard Frame Format.

Extended Data Frame



KEY.

SOF	Start-Of-Frame
IDxx	Identifier bit xx
SRR	Substitute Remote Request bit
IDE	Identifier Extension Flag
RTR	Remote Transmission Request bit
r1	Reserved bit 1
r0	Reserved bit 0
DLCx	Data Length Code bit x
CRC Del	Cyclic Redundancy Check Delimiter
ACK Slot bit	Acknowledge Slot bit
ACK Del	Acknowledge Delimiter
EOF	End-Of-Frame
IFS	Interframe space

Figure 3. Extended Frame Format.

Remote Frame

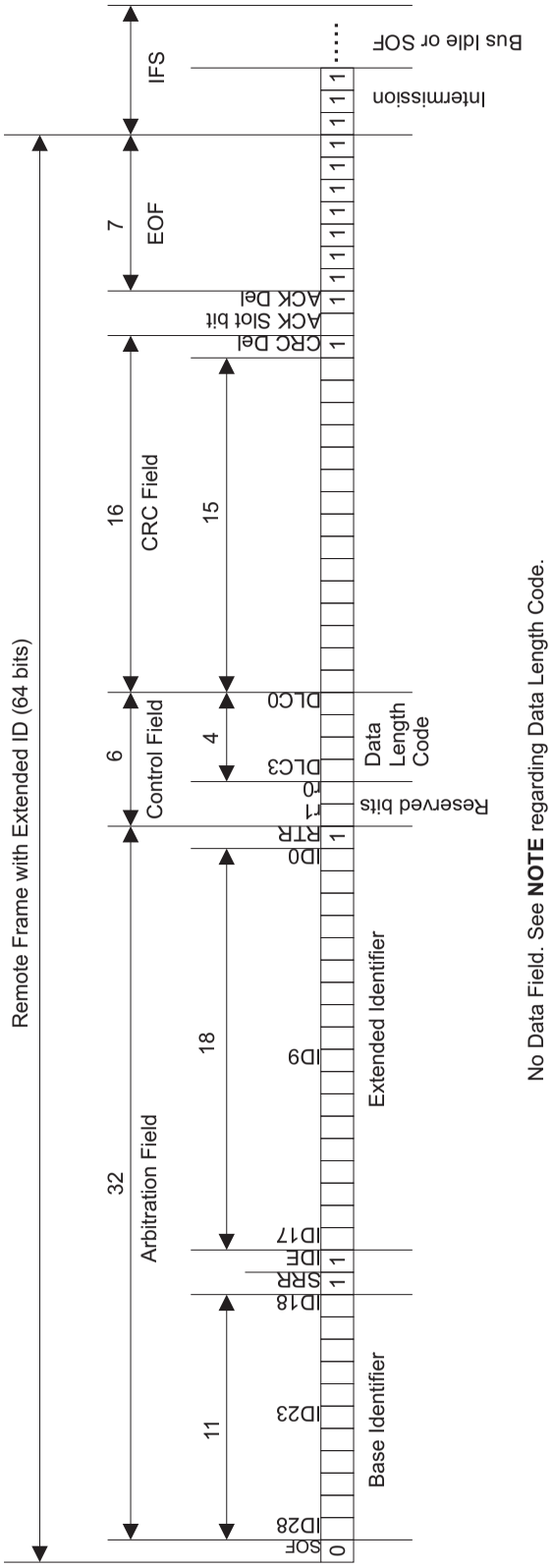


Figure 4. Remote Frame Format (Extended Identifier).

Error Frame

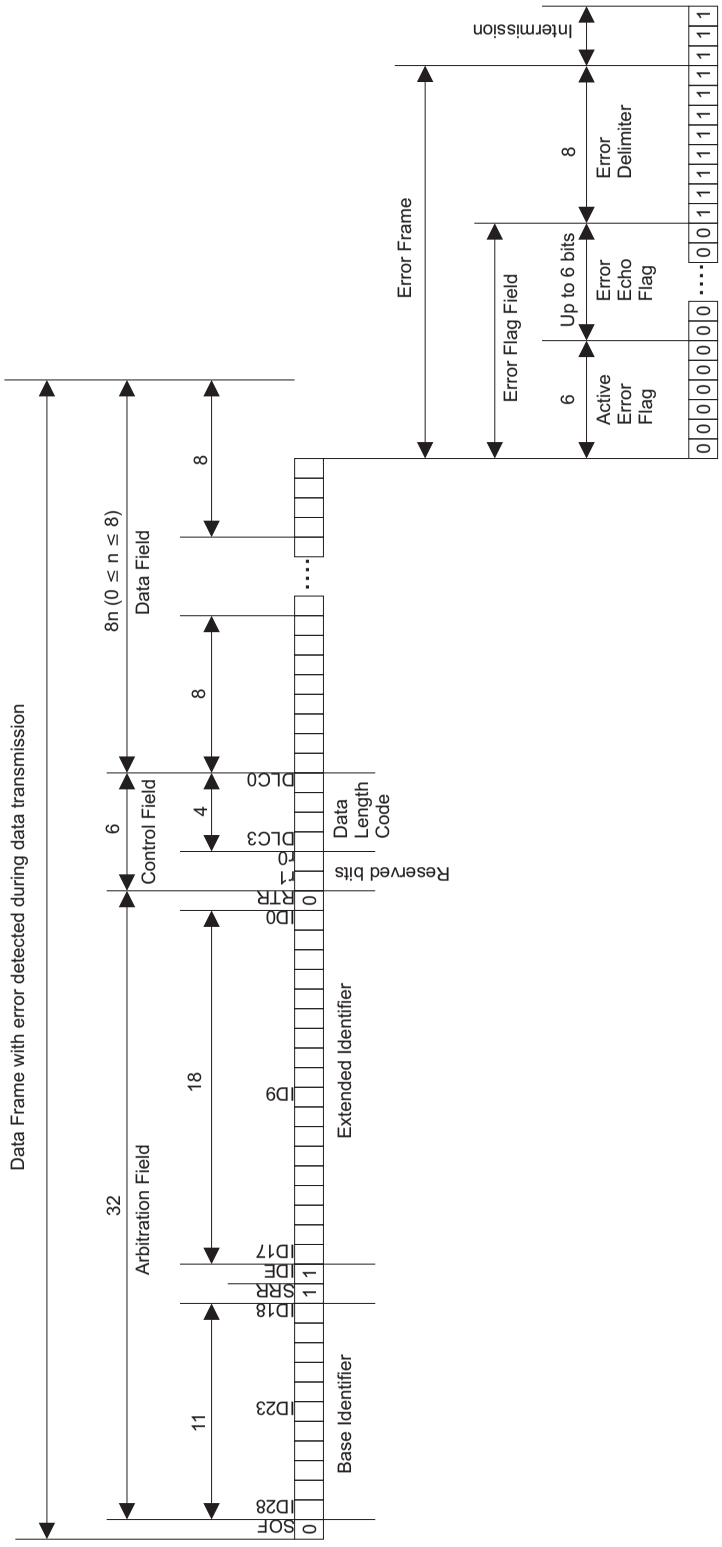


Figure 5. Error Frame Format.

Overload Frame

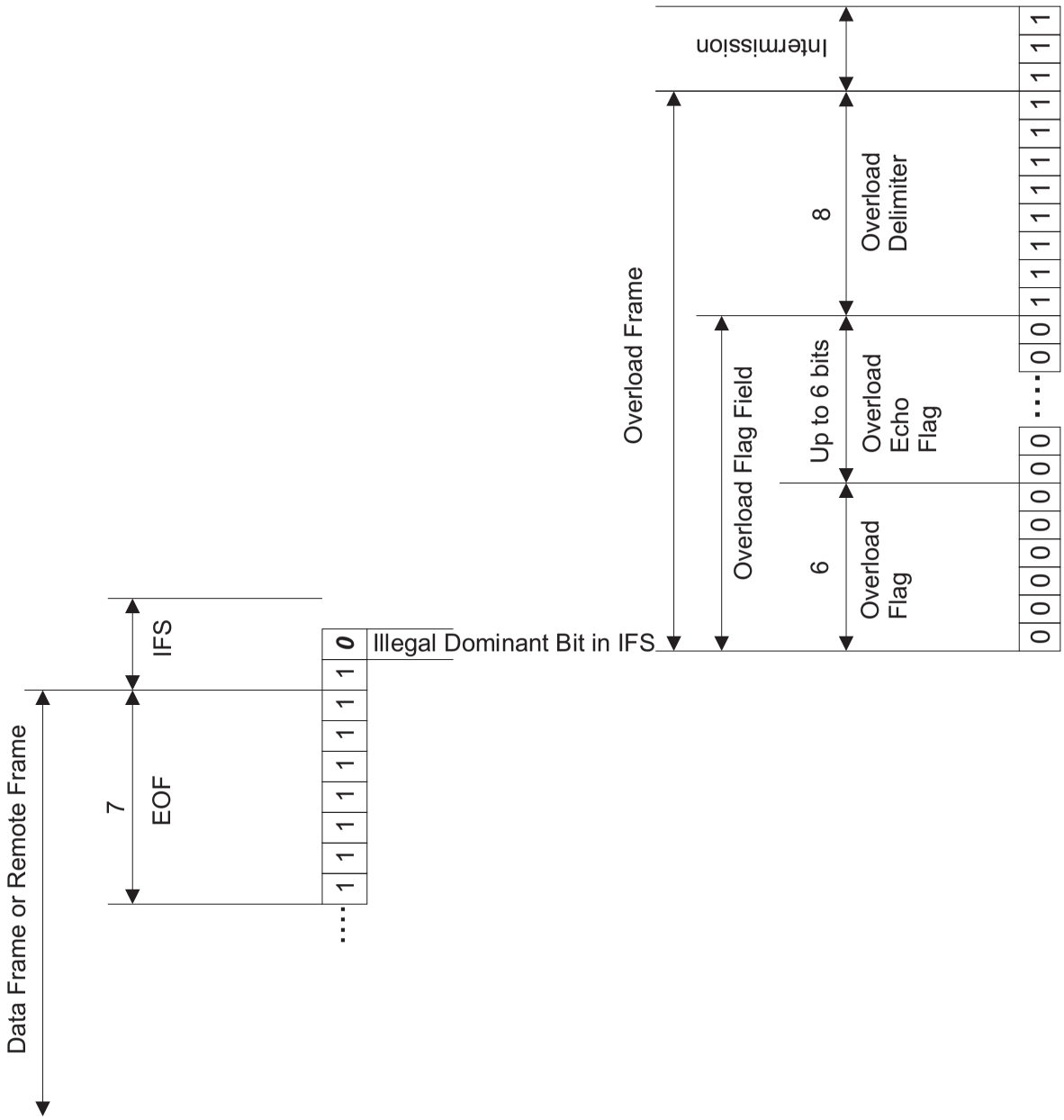


Figure 6. Overload Frame Format

BIT WISE ARBITRATION

The CAN standard resolves data contention on the bus using a scheme called Carrier Sense Multiple Access/Collision Detection-Carrier Resolution (CSMA/CD-CR).

Carrier Sense: Each node waits for a period without bus activity (bus idle state) before attempting transmission.
Multiple Access: Every node on the bus has equal access to the bus for transmitting.
Collision Detection: Collisions occur if two nodes attempt to transmit at the same time.
Collision Resolution: Collisions are resolved by bitwise arbitration. Highest priority messages (lowest binary identifiers) are sent first without delay and lower-priority messages are automatically re-transmitted later. A dominant bit (logic 0) has priority over a recessive bit (logic 1).

Bitwise arbitration works by comparing each node's transmitted data bit by bit. All nodes are synchronized by adjusting individual bit times as a function of bit time quanta (see section on bit timing). Synchronization takes place on recessive to dominant edges. A Hard Synchronization at the start of each frame and subsequent re-synchronizations during a message frame ensures corresponding bits match in time during a given transmission cycle. When a node transmits a recessive bit on the bus, but detects a dominant bit on it's receiver, it realizes arbitration is lost and it immediately ceases transmission and becomes a receiver. It will then wait for the next bus idle state and attempt to re-transmit. Eventually, lower priority messages will gain access to the bus. Figure 7 shows an example of how this works for a frame with a standard identifier.

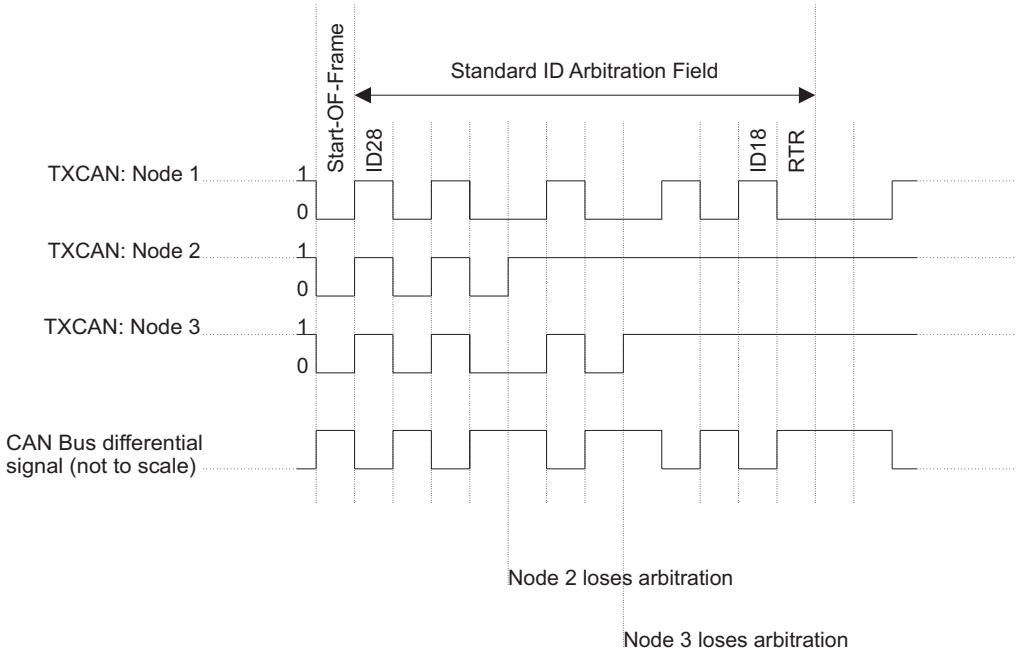


Figure 7. Bitwise Arbitration.

BIT TIMING

The CAN protocol supports a broad range of bit rates, from a few kHz up to 1MHz (**Note:** the minimum bit rate of the HI-3110 is limited to 40kHz by the permanent dominant timeout protection of the transceiver). Every node on the network has it's own clock generator (typically a quartz oscillator), however the bit rate must obviously be the same for every node on the bus. Therefore, each CAN node must be configurable to generate the nominal bit rate as a function of it's own oscillator frequency, f_{OSC}. This is done by generating a time quanta (TQ) clock, whose period t_{TQ} is related to the oscillator frequency by a Baud Rate Prescaler value, BRP as follows:

$$t_{TQ} = 2 \bullet BRP / f_{OSC} \qquad (1)$$

The TQ clock is used to construct the bit time in terms of time quanta, such that one time quantum, Tq, equals one TQ clock period, t_{TQ}, as shown in figure 8 below.
The CAN system nominal bit rate (BR) is defined in terms of the nominal bit time, t_b, as

$$BR = 1/t_b \qquad (2)$$

Therefore, the nominal bit rate is related to the TQ clock period by the following relationship

$$BR = 1/(t_{TQ} \text{ x (number of time quanta per bit))} \qquad (3)$$

The CAN standard divides the bit time into four segments, namely, synchronization segment (Sync Seg), propagation time segment (Prop Seg), phase buffer segment 1 (Phase Seg1) and phase buffer segment 2 (Phase Seg2). This is illustrated in figure 8. The HI-3110 fixes the Sync Seg at 1Tq. Prop Seg and Phase Seg1 are treated as one time segment, TSeg1, which is programmable from 2Tq to 16Tq. Phase Seg2 is a second time segment, TSeg2, which is programmable from 2Tq to 8Tq (**Note:** Not all combinations are valid, see below for examples).

Synchronization Segment (Sync Seg)

The Sync Seg is the first segment of the bit time and is used to synchronize the various nodes on the bus. A bit edge is expected to occur within the Sync Seg.

Propagation Time Segment (Prog Seg)

The Prog Seg is used to compensate for physical delays on the bus, which include signal propagation delay time on the bus and internal node delay times. For two nodes A and B communicating on the bus, Prog Seg must be greater than or equal to the sum of both nodes internal delays plus twice the bus line propagation delay between the two nodes.

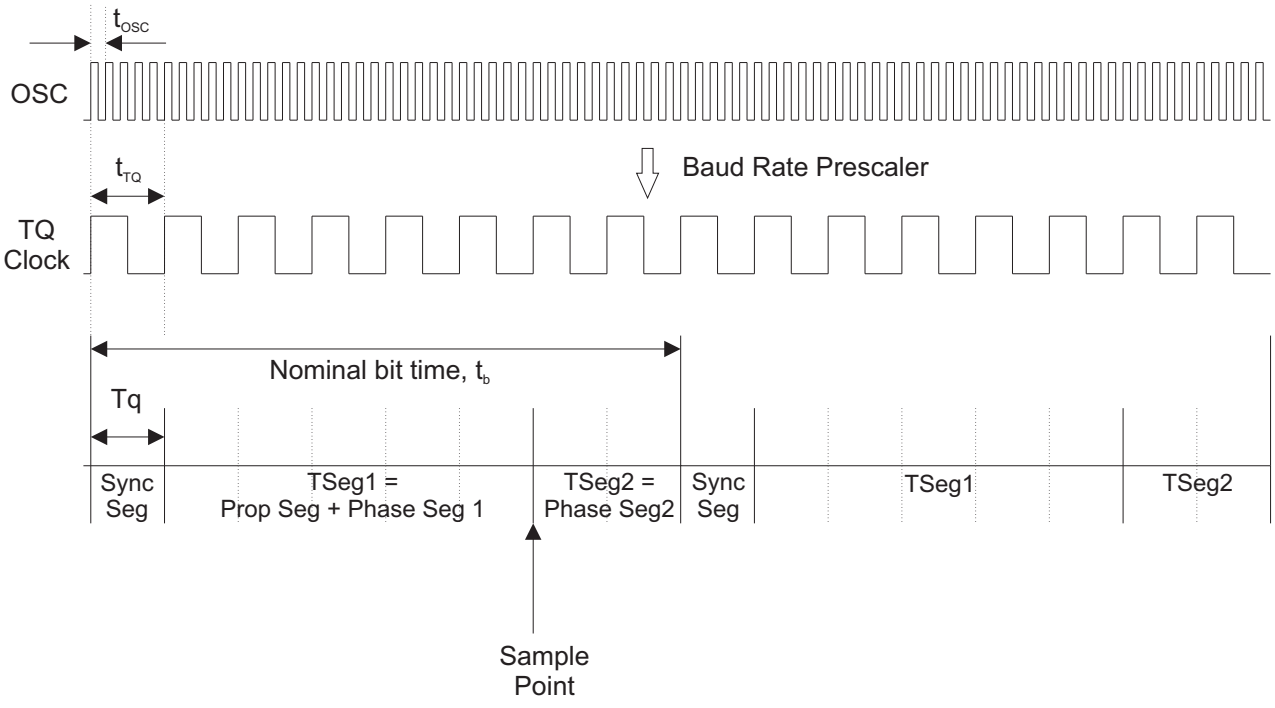


Figure 8. CAN Bit Time

Phase Buffer Segment 1 and Phase Buffer Segment 2 (Phase Seg1 and Phase Seg2)

The phase buffer segments are used to compensate for phase errors on the bus. Phase Seg1 can be lengthened or Phase Seg2 can be shortened duringthe re-synchronization bit period automatically by the HI-3110 so that the bit time can be adjusted to account for phase errors. The upper limit by which the lengthening (or shortening) can occur is set by the **re-synchronization jump width (SJW),** explained in more detail below.

Sample Point

The sample point is the point in the bit time at which the bit logic level is interpreted. It is located at the end of Phase Seg1. The HI-3110 also allows three sample points to be taken. In this case, two other sample points are taken prior to the end of Phase Seg1 (at one-half TQ intervals) and the value of the bit is determined by a majority decision. Three sample points are typically only used at low bit rates. **Note:** ARINC 825 states that there shall be only one sample per bit, taken at the end of Phase Seg1.

The time required for the logic to determine the bit level of a sampled bit is known as the **information processing time (IPT)**. According to the standard, IPT can be up to 2Tq. Since Phase Seg2 occurs after the sample point, Phase Seg2 must be greater than or equal to the worst case IPT (2Tq).

Phase Errors (e)

If a bit edge occurs within the Sync Seg as expected, there is no phase error (e = 0). However, if an edge occurs outside Sync Seg, a phase error is deemed to have occurred. If the edge occurs after Sync Seg (edge occurs “late”), the phase error is positive (e > 0), whereas if the edge occurs before Sync Seg (edge occurs “early”), the phase error is negative (e < 0).

Synchronization

Synchronization is carried out only on recessive-to-dominant bit edges and is used to ensure the bit times of all nodes on the bus are synchronized. This is necessary for arbitration and message acknowledgment to function properly. Only one synchronization can occur per bit time.

Hard synchronization forces the bit edge to lie within the Sync Seg, regardless of the phase error. Hard synchronization only occurs on reception of the start of a frame.

Re-synchronization results in the shortening or lengthening of the bit time such that the position of the sample point is shifted with respect to the edge causing the re-synchronization. **For e > 0**, Phase Seg 1 is lengthened by the magnitude of the phase error, up to a maximum of SJW. **For e < 0**, Phase Seg 2 is shortened by the magnitude of the phase error, up to a maximum of SJW.

Examples

1) CAN bit rate (BR) = 125kHz, f_{osc} = 12MHz.
Assume sample point (at end of TSeg1) will occur at 75% of bit time. Hence, for Sync Seg = 1Tq, TSeg1 = 5 Tq and TSeg2 = 2Tq. Therefore, total bit time will be 8Tq. Chose SJW = 1Tq.
For 125kHz, the bit time needs to be 1/125kHz = 8µs. Hence, 1Tq = 1µs. Using equation (1) => BRP = 6.

2) CAN bit rate (BR) = 1MHz, f_{osc} = 32MHz.
Assume sample point (at end of TSeg1) will occur at 75% of bit time. For Sync Seg = 1Tq, then TSeg1 = 11Tq and TSeg2 = 4Tq. Therefore, total bit time will be 16Tq. Chose SJW = 1Tq.
For 1MHz, the bit time needs to be 1/1MHz = 1µs. Hence, 1Tq = 62.5ns. Using equation (1) => BRP = 1.

Note: Choosing the sample point at 75% of the bit time is a requirement of ARINC 825. The oscillator frequency must be chosen such that a valid value of BRP (integer) can generate the TQ clock (e.g. in example 2 above, using a lower oscillator frequency than 32MHz results in BRP < 1).

REGISTERS

This section describes the HI-3110 registers. All register bits are active high. Unless otherwise indicated, all registers are reset in software to the logic zero condition after Master Reset. For all registers, bit 7 is the most significant:

REGISTER	R/W	DESCRIPTION	SPI WRITE OP-CODE	SPI READ OP-CODE
CTRL0	R/W	Control Register 0	0x14	0xD2
CTRL1	R/W	Control Register 1	0x16	0xD4
BTR0	R/W	Bit Timing Register 0	0x18	0xD6
BTR1	R/W	Bit Timing Register 1	0x1A	0xD8
TEC	R/W	Transmit Error Counter Register	0x26	0xEC
REC	R/W	Receive Error Counter Register	0x24	0xEA
MESSTAT	R	Message Status Register	N/A	0xDA
ERR	R	Error Register	N/A	0xDC
INTF	R	Interrupt Flag Register	N/A	0xDE
INTE	R/W	Interrupt Enable Register	0x1C	OxE4
STATF	R	Status Flag Register	N/A	0xE2
STATFE	R/W	Status Flag Enable Register	0x1E	0xE6
GPINE	R/W	General Purpose Pins Enable Register	0x22	0xE8
TIMERUB	R	Free-Running Timer Upper Byte Register	N/A	0xFA*
TIMERLB	R	Free-Running Timer Lower Byte Register	N/A	0xFA*

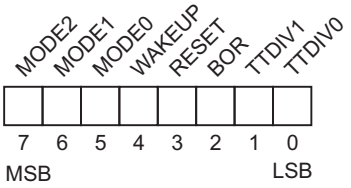
Note: Free-running counter registers, TIMERUB:TIMERLB are read with a single SPI Op-code (0xFA) as a 16-bit value in two SPI data bytes.

Power-On-Reset

Following power-on, the HI-3110 will automatically perform a Master Reset and return all registers to the default state. Following reset, the device will default to Initialization Mode to allow programming of Control and Bit Timing Registers (see following sections).

CONTROL REGISTER 0: CTRL0

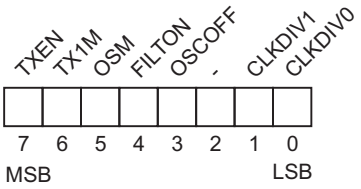
(Write, SPI Op-code 0x14)
(Read, SPI Op-code 0xD2)



Bit	Name	R/W	Default	Description
7-5	MODE2:0	R/W	1,0,0	Mode select bits <2:0>. These bits select the mode of operation as follows. 000: Normal Mode. Normal CAN operation. 001: Loopback Mode. The transceiver digital input is fed back to the receiver without disturbing the bus. This mode can be used for test purposes, allowing the HI-3110 to receive its own messages. 010: Monitor Mode. The HI-3110 can be set up to monitor bus activity without transmitting to the bus (no ACK bits or error frames are sent in this mode). Receive filters can be programmed in Initialization Mode to buffer selected messages. 011: Sleep Mode. The HI-3110 can be placed in a low power sleep mode if there is no bus activity and the transmit FIFO is empty. Sleep mode is exited by selecting an alternative mode of operation, or automatic wake up following bus activity can be enabled by setting the WAKEUP bit. The device will wake up in Monitor mode. 1xx: Initialization Mode. The device **must** be in this mode for bit timing and filter set-up. This is the default following reset. The host exits initialization mode by selecting an alternative mode of operation.
4	WAKEUP	R/W	0	Wake-Up Enable. When this bit is set, the HI-3110 will automatically wake up from Sleep Mode to Monitor Mode when it detects activity on the bus. 1 = Automatic wake-up enabled. When the device wakes up from Sleep Mode, the WAKEUP bit will be set in the Interrupt Flag Register, INTF. A hardware interrupt can be generated at the INT pin by setting the WAKEUPIE bit in the Interrupt Enable Register. 0 = Automatic wake-up not enabled. In this case, wake-up from Sleep Mode is initiated by the host by selecting another mode of operation. When WAKEUP = 0, all bus activity is ignored.
3	RESET	R/W	0	Setting this bit causes HI-3110 reset to occur. Following reset, the CTRL0 register should be written with < 1 x x x 0 x x x >. This will clear the RESET bit and also avoid unpredictable behavior by ensuring the part is programmed to Initialization Mode, ready for set-up. A reset may also be performed by setting the MR pin or issuing the “MR” SPI command, 0x56. 1 = Master Reset (same as MR pin = 1). 0 = Normal Operation (same as MR pin = 0).
2	BOR	R/W	0	Bus-off Reset. When this bit is set, automatic bus-off recovery is initiated following 128 occurrences of 11 consecutive recessive bits on the bus. The HI-3110 will become error-active with both its error counters set to zero and resume operation in Normal Mode. 1 = Automatic bus-off recovery. 0 = The host is responsible for bus-off recovery (default).
1-0	TDIV1:0	R/W	0,0	Time Tag Clock Division Bits <1:0>. See TIMERUB and TIMERLB register descriptions. 00 = No division (counts every bit clock). 01 = Divide by 2 (counts every 2 bit clocks). 10 = Divide by 4 (counts every 4 bit clocks). 11 = Divide by 8 (counts every 8 bit clocks).

CONTROL REGISTER 1: CTRL1

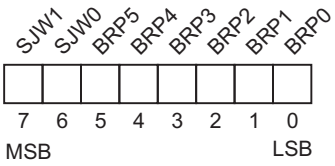
(Write, SPI Op-code 0x16)
(Read, SPI Op-code 0xD4)



Bit	Name	R/W	Default	Description
7	TXEN	R/W	0	Transmission Enable. This bit is logically ORed with the TXEN pin. When this bit is asserted, each message in the FIFO will be sequentially loaded to the transmit buffer and sent if the bus is available. If this bit is not set, a transmission can be enabled by either the TXEN pin or the TX1M bit. If the TXEN pin is pulled low during a transmission, the current message being transmitted will be completed. Any additional messages in the FIFO will not be transmitted. 1 = Enable transmission and send any messages in FIFO (until empty if TXEN is held set). 0 = Wait for transmission enable or TX1M bit set before sending next message in FIFO.
6	TX1M	R/W	0	Enable transmission of only next message. This bit is applicable only if TXEN = 0. It is reset automatically upon completion of a successful transmission or by initiation of transmission if the OSM bit is set. 1 = Enable transmission of only next message in FIFO when TXEN = 0. 0 = Wait for transmission enable or TX1M bit set before sending next message in FIFO.
5	OSM	R/W	0	One-Shot Mode Enable. OSM is intended to be used ONLY with the TX1M bit. If OSM is enabled and TX1M is set, the controller transmits only once and does not attempt re-transmission upon loss of arbitration or error. This feature is necessary to support the implementation of fixed time slots in the Time-Triggered CAN standard (TTCAN). Note**: Un-transmitted messages will remain in the FIFO. If a new message is required on the next transmission cycle, the user must first clear the FIFO with SPI command 0x54 and then reload the new message.** 1 = Enable one-shot mode. 0 = Messages will re-transmit according to CAN protocol.
4	FILTON	R/W	0	Filter on enable. This bit is set to turn on the HI-3110 CAN ID filtering mechanism. The default after reset is FILTON = 0, meaning filtering is turned off and every valid CAN message is accepted into the receive FIFO. **Note: The device must be in initialization mode in order to program the acceptance filters and masks.** 1 = Enable CAN ID filtering. 0 = No CAN ID filtering (every valid message accepted into receive FIFO).
3	OSCOFF	R/W	0	Oscillator off. This bit should be set to a one if an external clock is used. In this case the external clock is connected to the OSCIN pin and OSCOUT should be left floating. 1 = Shuts off external OSCOUT pin. 0 = OSCOUT pin enabled.
2	Not used	R/W	0	
1-0	CLKDIV1:0	R/W	00	External CLKOUT division bits <1:0> 00: Divide by 1. 01: Divide by 2. 10: Divide by 4. 11: Divide by 8.

BIT TIMING REGISTER 0: BTR0

(Write, SPI Op-code 0x18)
(Read, SPI Op-code 0xD6)

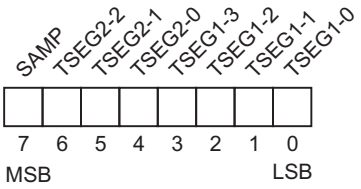


BTR0 defines the value of the Re-synchronization Jump Width (SJW) and the Baud Rate Prescaler (BRP). This register can be read anytime and written only in init mode (MODE<2:0> bits set to <1xx> in the CTRL0 register).

Bit	Name	R/W	Default	Description
7-6	SJW1:0	R/W	0	Re-synchronization Jump Width bits <1:0>. These bits are used to compensate for phase shifts between different clock oscillators on the bus. They define the maximum number of time quanta (Tq) a bit can be shortened or lengthened to allow a node achieve re-synchronization to the edge of an incoming signal. Note that one time quantum (Tq) is the single unit of time within a bit time (see Bit Timing section). **SJW bits <1:0>** 00: SJW = 1 Tq 01: SJW = 2 Tq 10: SJW = 3 Tq 11: SJW = 4 Tq **Note:** ARINC 825 states that the Re-synchronization Jump Width shall be 1 Tq
5-0	BRP5:0	R/W	0	Baud Rate Prescaler bits <5:0>. The baud rate prescaler relates the system oscillator frequency, f_{OSC}, to the CAN bit time as described in the bit timing section. **BRP bits <5:0>** 000000: BRP = 1 000001: BRP = 2 000010: BRP = 3 000011: BRP = 4 . etc. . 111111: BRP = 64

BIT TIMING REGISTER 1: BTR1

(Write, SPI Op-code 0x1A)
(Read, SPI Op-code 0xD8)

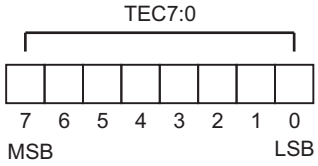


BTR1 configures the CAN protocol bit timing segments in terms of time quanta (Tq) and sets the number of sampling points. This register can be read anytime and written only in init mode (MODE<2:0> bits set to <1xx> in the CTRL0 register).

Bit	Name	R/W	Default	Description
7	SAMP	R/W	0	Samples per bit. This bit configures how many samples are taken per bit. 1 = three samples per bit. 0 = one sample per bit. **Notes:** ARINC 825 states that there shall be only one sample per bit. Furthermore, it is recommended to sample only once at higher CAN bit rates. Bit sampling occurs at the end of Phase Seg1.
6-4	TSEG2-2:0	R/W	0	Time Segment 2 bits <2:0>. Tseg2 = Phase Seg2 of the CAN protocol bit timing specification. Bits TSEG2-2:0 specify the number of time quanta in Phase Seg2. **Note:** Not all combinations are valid, since Phase Seg 2 must be greater than SJW. **TSEG2 bits <2:0>** 000: Not valid 001: Tseg2 = 2 Tq clock cycles 010: Tseg2 = 3 Tq clock cycles . etc. . 111: Tseg2 = 8 Tq clock cycles
3-0	TSEG1-3:0	R/W	0	Time Segment 1 bits <3:0>. Tseg1 = Prop Seg + Phase Seg1 of the CAN protocol bit timing specification. Bits TSEG1-3:0 specify the number of time quanta in Prop Seg + Phase Seg1. Note: Not all combinations are valid, since Prop Seg + Phase Seg1 ≥ Phase Seg 2. **The CAN protocol states that the minimum number of Tq in a bit time shall be 8.** **TSEG1 bits <3:0>** 0000: Not valid 0001: Tseg1 = 2 Tq clock cycles 0010: Tseg1 = 3 Tq clock cycles 0011: Tseg1 = 4 Tq clock cycles 0100: Tseg1 = 5 Tq clock cycles . . . 1111: Tseg1 = 16 Tq clock cycles **Notes:** ARINC 825 states that the sample point shall not be less than 75% of the bit time. In this case, Tseg1 should be a minimum of 5Tq for Phase Seg2 (Tseg2) = 2Tq and SJW = 1Tq.

TRANSMIT ERROR COUNTER REGISTER: TEC

(Write, SPI Op-code 0x26)
(Read, SPI Op-code 0xEC)



The TEC register reflects the current value of the CAN Transmit Error Counter. This register can be written by SPI command for test purposes.

Bit	Name	R/W	Default	Description
7-0	TEC7:0	R/W	0x00	Transmit Error Counter bits <7:0>.

0 ≤ TEC ≤ 95: Error active status.

96≤ TEC ≤ 127: Error active status. Error warning flag, ERRW, set in STATF register. This may be used to generate a hardware interrupt if ERRWIE bit is set in STATFE register.

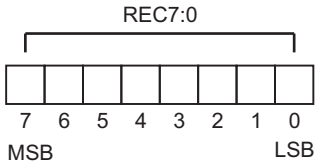
128 ≤ TEC≤ 255: Error passive status. Transmit error passive flag, TXERRP, set in ERR register. ERRP also set in STATF register. This may be used to generate a hardware interrupt if ERRPIE bit is set in STATFE register.

TEC > 255: Bus-off status. Bus-off flags, BUSOFF, set in ERR and STATF registers. The latter may be used to generate a hardware interrupt if BUSOFFIE bit is set in STATFE register.

The HI-3110 will, after entering bus-off state, automatically recover to error active status without host intervention if the BOR bit is set in control register CTRL0 and 128 x 11 consecutive recessive bits are detected on the bus. If the BOR bit is not set, bus-off recovery is managed by the host.

RECEIVE ERROR COUNTER REGISTER: REC

(Write, SPI Op-code 0x24)
(Read, SPI Op-code 0xEA)



The REC register reflects the current value of the CAN Receive Error Counter. This register can be written by SPI command for test purposes.

Bit	Name	R/W	Default	Description
7-0	REC7:0	R/W	0x00	Receiver Error Counter bits <7:0>.

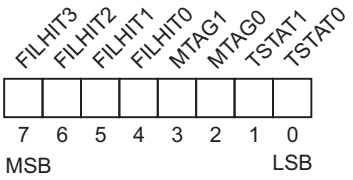
0 ≤ REC ≤ 95: Error active status.

96 ≤ REC ≤ 127: Error active status. Error warning flag, ERRW, set in STATF register. This may be used to generate a hardware interrupt if ERRWIE bit is set in STATFE register.

128 ≤ REC ≤ 255: Error passive status. Receive error passive flag, RXERRP, set in ERR register. ERRP also set in STATF register. This may be used to generate a hardware interrupt if ERRPIE bit is set in STATFE register.

MESSAGE STATUS REGISTER: MESSTAT

(Read only)
(Read, SPI Op-code 0xDA)

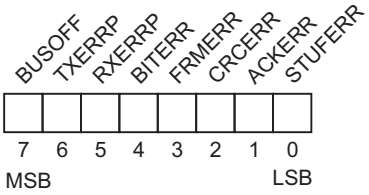


This register reflects transmission status and also which filters were responsible for filtering valid received messages. It is read-only.

Bit	Name	R/W	Default	Description
7-4	FILHIT3:0	R	0	Filter hit bits <3:0>. These bit combinations indicate which filters were responsible for filtering received messages . 0000: No filter matches the received message. 1000: Filter 0 matches, but filters 1, 2, 3, 4, 5, 6 or 7 may also match. 1001: Filter 1 matches, filter 0 does not, but filters 2, 3, 4, 5, 6 or 7 may also match. 1010: Filter 2 matches, filters 0 and 1 do not, but filters 3, 4, 5, 6 or 7 may also match. 1011: Filter 3 matches, filters 0 through 2 do not, but filters 4, 5, 6 or 7 may also match. 1100: Filter 4 matches, filters 0 through 3 do not, but filters 5, 6, or 7 may also match. 1101: Filter 5 matches, filters 0 through 4 do not, but filters 6 or 7 may also match. 1110: Filter 6 matches, filters 0 through 5 do not, but filter 7 may also match. 1111: Filter 7 matches, all other filters do not. **Note:** Filter checking is carried out by the internal logic in order of increasing filter number. Once a filter matches, no further checking takes place. Therefore, in the case of more than one filter matching for a given message, the lowest filter will be given priority and the FILHIT3:0 bits will reflect this value.
3-2	MTAG1:0	R	0	Message Tag bits <1:0>. These bits will reflect the last two bits of the host assigned message tag of the last successful transmission.
1-0	TSTAT1:0	R	0	Transmission Status bits <1:0>. These bits reflect the transmission status. 00: Transmission not enabled (TXEN = 0). 01: Transmission is enabled (TXEN = 1), but FIFO is empty. 10: Waiting to transmit or re-transmit. 11: Transmitter is currently transmitting a message or a flag.

ERROR REGISTER: ERR

(Read only)
(Read, SPI Op-code 0xDC)

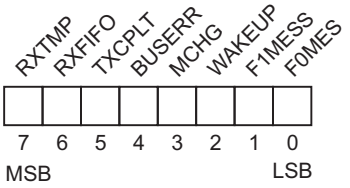


The ERR register indicates CAN bus status and protocol errors. It is read only. All bits default to 0 at power up and maintain their current status following reset. Bits 4:0 are reset following a host read.

Bit	Name	R/W	Default	Description
7	BUSOFF	R	0	Bus-off status indicator. This bit is set when TEC > 255. Node is in bus off condition. The bit is reset by HI-3110 when a successful bus recovery sequence is detected (128 x 11 consecutive recessive bits). d the FILHIT3:0 bits will reflect this value.
6	TXERRP	R	0	Transmit Error Passive status indicator. This bit is set when 128 ≤ TEC ≤ 255.
5	RXERRP	R	0	Receive Error Passive status indicator. This bit is set when 128 ≤ REC ≤ 255.
4	BITERR	R	0	Bit Error. A bit error was detected in a transmitted frame (the bit observed on the bus was opposite to what was expected).
3	FRMERR	R	0	Form Error. A Form error was detected in a receive frame.
2	CRCERR	R	0	CRC Error. A CRC error was detected in a receive frame.
1	ACKERR	R	0	Acknowledgement Error. An ACK error was detected in a receive frame.
0	STUFERR	R	0	Stuff Error. A bit stuffing error was detected in a received frame.

INTERRUPT FLAG REGISTER: INTF

(Read only)
(Read, SPI Op-code 0xDE)

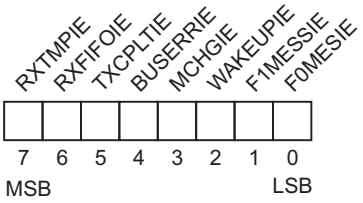


The Interrupt Flag Register INTF bits will be set by HI-3110 when the corresponding related events described below occur. If individual bits in the Interrupt Enable Register INTE are set, the INT pin will be latched high when any of the corresponding INTF bits are set. This alerts the host that one of the conditions below has occurred. Reading this register will clear all bits and reset the INT pin. The value of individual bits in the INTF register may also be reflected on the GP1 and GP2 pins by setting the correct bit combinations in the General Purpose Pins Enable Register GPINE (see section General Purpose Pins Enable Register).

Bit	Name	R/W	Default	Description
7	RXTMP	R	0	Message received in temporary receive buffer (unfiltered). This bit is set when a valid message is received in the temporary receive buffer.
6	RXFIFO	R	0	Message received in FIFO (filtered). This bit is set when a valid message passes the filter criteria and is passed from the temporary receive buffer to the receive FIFO.
5	TXCPLT	R	0	Successful transmission complete. This bit is set when a message is successfully transmitted.
4	BUSERR	R	0	Bus Error. This bit is set when a bus error occurs. Bits 4:0 in the ERR register can be read to determine the source of the error.
3	MCHG	R	0	Mode Change bit. This bit is set when the mode of operation is changed. Any pending transmissions in the transmit FIFO will be completed (FIFO will be emptied) before the mode change occurs.
2	WAKEUP	R	0	Wake-Up detected. This bit is set when the HI-3110 wakes up from Sleep Mode in response to bus activity.
1	F1MESS	R	0	Filter 1 passed a valid message. This bit is set when receive filter one passes a valid message. FILHIT3:0 bits will also be set to <1001> in the Message Status Register, MESSTAT.
0	F0MESS	R	0	Filter 0 passed a valid message. This bit is set when receive filter zero passes a valid message. FILHIT3:0 bits will also be set to <1000> in the Message Status Register, MESSTAT.

INTERRUPT ENABLE REGISTER: INTE

(Write SPI Op-code 0x1C)
(Read, SPI Op-code 0xE4)



Setting bits in the Interrupt Enable Register causes a hardware interrupt to be generated at the INT pin when the corresponding bits in the Interrupt Flag Register are set by HI-3110 as a result of the related events described below.

Bit	Name	R/W	Default	Description
7	RXTMPIE	R/W	0	Enable interrupt when a message is received in the temporary receive buffer (unfiltered). Setting this bit causes a hardware interrupt to be generated at the INT pin when the RXTMP bit is set in the INTF register.
6	RXFIFOIE	R/W	0	Enable interrupt when a message is received in the receive FIFO (filtered). Setting this bit causes a hardware interrupt to be generated at the INT pin when the RXFIFO bit is set in the INTF register.
5	TXCPLTIE	R/W	0	Enable interrupt when a successful transmission is complete. Setting this bit causes a hardware interrupt to be generated at the INT pin when the TXCPLT bit is set in the INTF register.
4	BUSERRIE	R/W	0	Enable interrupt when a bus error occurs. Setting this bit causes a hardware interrupt to be generated at the INT pin when the BUSERR bit is set in the INTF register.
3	MCHGIE	R/W	0	Enable interrupt when a mode change occurs. Setting this bit causes a hardware interrupt to be generated at the INT pin when the MCHG bit is set in the INTF register.
2	WAKEUPIE	R/W	0	Enable interrupt when HI-3110 wakes up from Sleep Mode. Setting this bit causes a hardware interrupt to be generated at the INT pin when the WAKEUP bit is set in the INTF register.
1	F1MESSIE	R/W	0	Enable interrupt when filter one passes a message. Setting this bit causes a hardware interrupt to be generated at the INT pin when the F1MESS bit is set in the INTF register.
0	F0MESSIE	R/W	0	Enable interrupt when filter zero passes a message. Setting this bit causes a hardware interrupt to be generated at the INT pin when the F0MESS bit is set in the INTF register.