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HI-5200

10 Base-T/100Base-TX Physical Layer Transceiver with Extended Temperature Operation

May 2018

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1. General Description

The HI-5200 is a single supply 10Base-T/100Base-TX physical layer transceiver, which provides MII/RMII interfaces to transmit and receive data.

HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables. An optional interrupt pin provides status updates to the external controller, avoiding the need for continuous polling.

The HI-5200 is available in 32-pin QFN (5mm x 5mm) or QFP packages. The device is capable of enhanced (−40°C to +105°C) and extended (−55°C to +125°C) operating temperature ranges.

2. Features

- Single-chip 10Base-T/100Base-TX physical layer solution with auto-negotiation
- Pin selectable 10Base-T or 100Base-Tx at power-up/reset with auto-negotiation disable option
- Fully compliant to IEEE 802.3u standard
- Low power CMOS design, power consumption of <180mW
- HP auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Robust operation over standard cables
- Power down and power saving modes
- MII interface support
- RMII interface support with external 50MHz system clock
- MIIM (MDC/MDIO) management bus to 6.25MHz for rapid PHY register configuration
- Interrupt pin option
- Programmable LED outputs for link, activity and speed
- ESD rating (6kV)
- Single power supply (3.3V)
- Built-in 1.8V regulator for core
- Enhanced (−40°C to +105°C) and extended (−55°C to +125°C) operating temperature ranges
- Full range of supporting magnetics available in both industrial and extended operating temperature ranges
- Available in a 32-pin QFN (5mm x 5mm) or thermally enhanced QFP packages

3. Pin Configurations (Top)

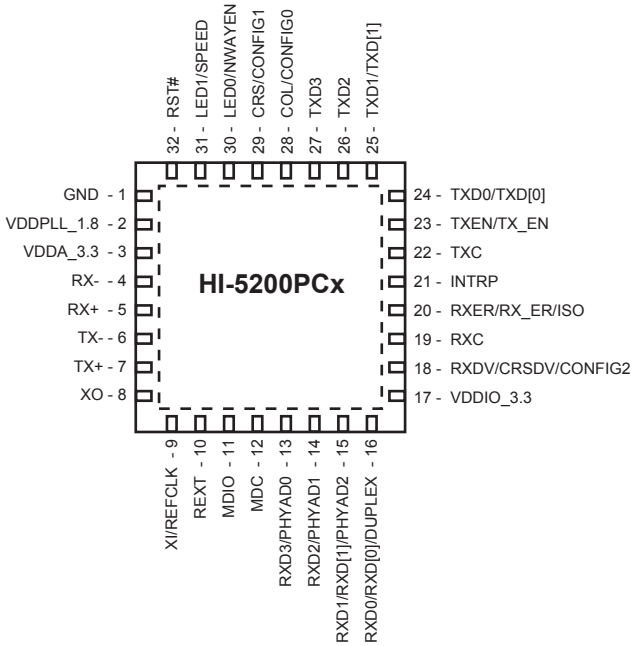


Figure 1. HI-5200: 32-Pin Plastic 5mm x 5mm QFN

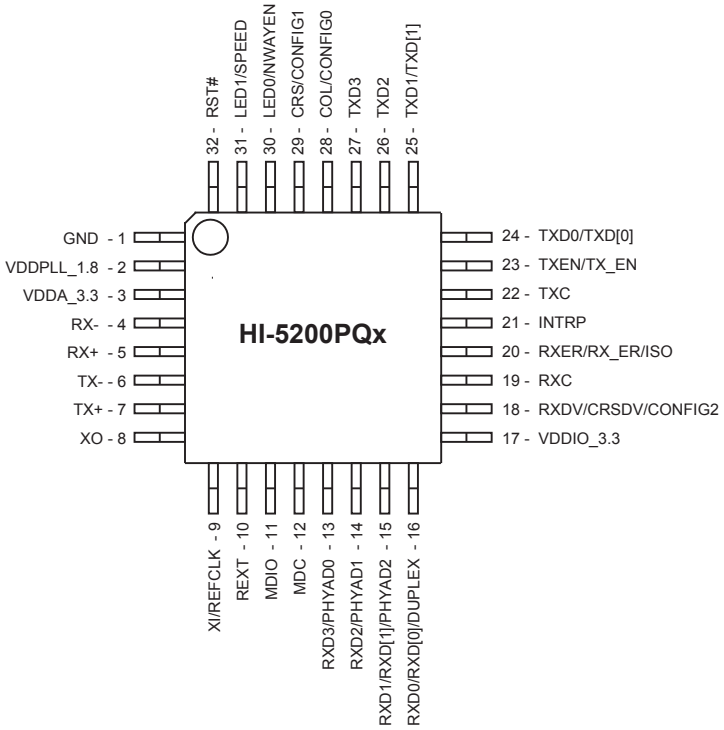


Figure 2. HI-5200: 32-Pin Plastic 9mm x 9mm TQFP

4. Block Diagram

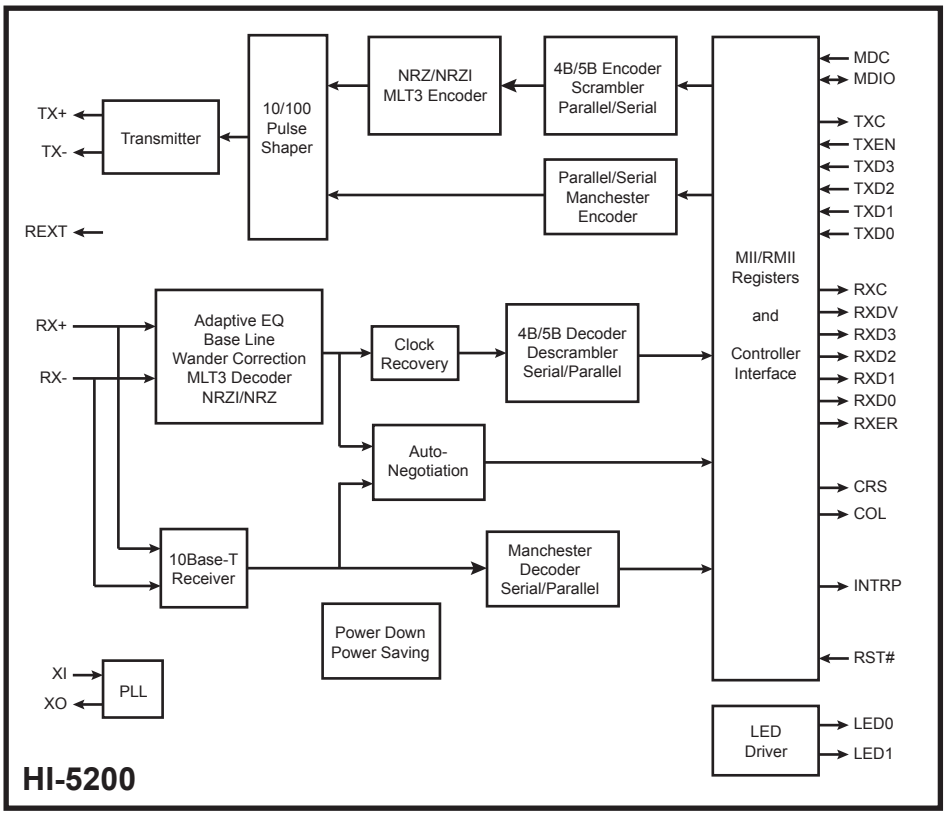


Figure 3. HI-5200 Block Diagram

5. Pin Descriptions

Table 1. HI-5200 Pin Descriptions

Pin Number	Pin Name	Function [1]	Description
1	GND	Gnd	Ground.
2	VDDPLL_1.8	P	1.8V Analog V_{DD} Decouple with 1.0pF and 0.1pF capacitors to ground.
3	VDDA_3.3	P	3.3V Analog V_{DD}.
4	RX-	I/O	Physical receive or transmit signal (- differential).
5	RX+	I/O	Physical receive or transmit signal (+ differential).
6	TX-	I/O	Physical transmit or receive signal (- differential).
7	TX+	I/O	Physical transmit or receive signal (+ differential).
8	XO	O	Crystal Feedback. This pin is used only in MII mode when a 25MHz crystal is used. This pin is a no connect if oscillator or external clock source is used, or if RMII mode is selected.
9	XI / REFCLK	I	Crystal / Oscillator / External Clock Input: **MII Mode:** 25MHz ± 50ppm (crystal, oscillator or external clock) **RMII Mode:** 50MHz ± 50ppm (oscillator or external clock only)
10	REXT	I/O	Set physical transmit output current. Connect a 6.49kΩ resistor in parallel with a 100pF capacitor to ground on this pin. See HI-5200 reference schematics.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7kΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
13	RXD3 / PHYAD0	Ipu/O	**MII Mode:** Receive Data Output[3][2]. **Config Mode:** The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See “Strapping Options” for details.
14	RXD2 / PHYAD1	Ipd/O	**MII Mode:** Receive Data Output[2][2]. **Config Mode:** The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See “Strapping Options” for details.
15	RXD1 / RXD[1] / PHYAD2	Ipd/O	**MII Mode:** Receive Data Output[1][2]. **RMII Mode:** Receive Data Output[1][3]. **Config Mode:** The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See “Strapping Options” for details.

Pin Number	Pin Name	Function [1]	Description
16	RXD0 / RXD[0] / DUPLEX	Ipu/O	**MII Mode:** Receive Data Output[0][2]. **RMII Mode:** Receive Data Output[0][3]. **Config Mode:** Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See “Strapping Options” for details.
17	VDDIO_3.3	P	3.3V Digital V_{DD}.
18	RXDV / CRSDV / CONFIG2	Ipd/O	**MII Mode:** Receive Data Valid Output. **RMII Mode:** Carrier Sense/Receive Data Valid Output. **Config Mode:** The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See “Strapping Options” for details.
19	RXC	O	**MII Mode:** Receive Clock Output.
20	RXER / RX_ER / ISO	Ipd/O	**MII Mode:** Receive Error Output. **RMII Mode:** Receive Error Output. **Config Mode:** The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See “Strapping Options” for details.
21	INTRP	Opu	Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
22	TXC	O	**MII Mode:** Transmit Clock Output.
23	TXEN / TX_EN	I	**MII Mode:** Transmit Enable Input. **RMII Mode:** Transmit Enable Input.
24	TXD0 / TXD[0]	I	**MII Mode:** Transmit Data Input[0][4]. **RMII Mode:** Transmit Data Input[0][5].
25	TXD1 / TXD[1]	I	**MII Mode:** Transmit Data Input[1][4]. **RMII Mode:** Transmit Data Input[1][5].
26	TXD2	I	**MII Mode:** Transmit Data Input[2][4]. Connect to GND in RMII Mode.
27	TXD3	I	**MII Mode:** Transmit Data Input[3][4]. Connect to GND in RMII Mode.
29	COL / CONFIG0	Ipd/O	**MII Mode:** Collision Detect Output. **Config Mode:** The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See “Strapping Options” for details.
29	CRS / CONFIG1	Ipd/O	**MII Mode:** Carrier Sense Output. **Config Mode:** The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See “Strapping Options” for details.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Function (1)</th><th>Description</th></tr>
<tr><td>30</td><td>LED0 /
NWAYEN</td><td>Ipu/O</td><td>
LED Mode: Programmable LED0 Output.

Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See “Strapping Options” for details.

The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00] (register 1Eh [15:14] = [0:0])</th></tr>
<tr><th>Link/Activity</th><th>LED0 Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01] (register 1Eh [15:14] = [0:1])</th></tr>
<tr><th>Link</th><th>LED0 Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>

LED Mode = [10] or [11]
Reserved.
</td></tr>
<tr><td>31</td><td>LED1 /
SPEED</td><td>Ipu/O</td><td>
LED Mode: Programmable LED1 Output /

Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See “Strapping Options” for details.

The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00] (register 1Eh [15:14] = [0:0])</th></tr>
<tr><th>Speed</th><th>LED1 Pin State</th><th>LED Definition</th></tr>
<tr><td>10BT</td><td>H</td><td>OFF</td></tr>
<tr><td>100BT</td><td>L</td><td>ON</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01] (register 1Eh [15:14] = [0:1])</th></tr>
<tr><th>Activity</th><th>LED1 Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

LED Mode = [10] or [11]
Reserved.
</td></tr>
<tr><td>32</td><td>RST#</td><td>I</td><td>Chip Reset (active low).</td></tr>
<tr><td>PACKAGE
PADDLE</td><td>GND</td><td>Gnd</td><td>Ground.</td></tr>
</table>

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Opu = Output with internal pull-up (40K ± 30%).
   Ipu/O = Input with internal pull-up (40K ± 30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K ± 30%) during power-up/reset; output pin otherwise.
2. MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.
3. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.
4. MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.
5. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

5.1. Strapping Options

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

Table 2. HI-5200 Strapping Options

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Function (1)</th><th>Description</th></tr>
<tr><td>15</td><td>PHYAD2</td><td>Ipd/O</td><td rowspan="3">The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>14</td><td>PHYAD1</td><td>Ipd/O</td></tr>
<tr><td>13</td><td>PHYAD0</td><td>Ipd/O</td></tr>
<tr><td>18</td><td>CONFIG2</td><td>Ipd/O</td><td rowspan="4">The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>010</td><td>Reserved − not used</td></tr><tr><td>011</td><td>Reserved − not used</td></tr><tr><td>100</td><td>MII 100Mbps Preamble Restore</td></tr><tr><td>101</td><td>Reserved − not used</td></tr><tr><td>110</td><td>Reserved − not used</td></tr><tr><td>111</td><td>Reserved − not used</td></tr></table></td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td></tr>
</table>

Pin Number	Pin Name	Function [1]	Description
20	ISO	Ipd/O	ISOLATE Mode: Pull-up = Enable Pull-down (default) = Disable During power-up / reset, this pin value is latched into register 0h bit 10.
31	SPEED	Ipu/O	SPEED Mode: Pull-up (default) = 100Mbps Pull-down = 10Mbps During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
16	DUPLEX	Ipu/O	DUPLEX Mode: Pull-up (default) = Half Duplex Pull-down = Full Duplex During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
30	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.

Notes:

1. Ipu/O = Input with internal pull-up (40K ± 30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K ± 30%) during power-up/reset; output pin otherwise.

6. Functional Description

The HI-5200 is a single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3u Specification.

The device supports 10Base-T and 100Base-TX with HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

The HI-5200 offers a choice of MII or RMII data interface connection with the MAC processor. The MII management bus option gives the MAC processor complete access to the HI-5200 control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status changes.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

6.1. 100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.

The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio. It has typical rise/fall times of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10Base-T output drivers are also incorporated into the 100Base-TX drivers.

6.2. 100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

6.3. PLL Clock Synthesizer

The HI-5200 generates 125MHz, 25MHz and 20MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator. For the HI-5200 in RMII mode, these internal clocks are generated from an external 50MHz oscillator or system clock.

6.4. Scrambler/De-Scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

6.5. 10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetics. The drivers also perform internal wave-shaping and pre-emphasize, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

6.6. 10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RX+ and RX- inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the HI-5200 decodes a data frame. The receive clock is kept active during idle periods in between data reception.

6.7. SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

6.8. Auto-Negotiation

The HI-5200 conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation is enabled by either hardware pin strapping (pin 30) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the HI-5200 link partner is forced to bypass auto-negotiation, the HI-5200 sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the HI-5200 to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the flow chart illustrated in Figure 4.

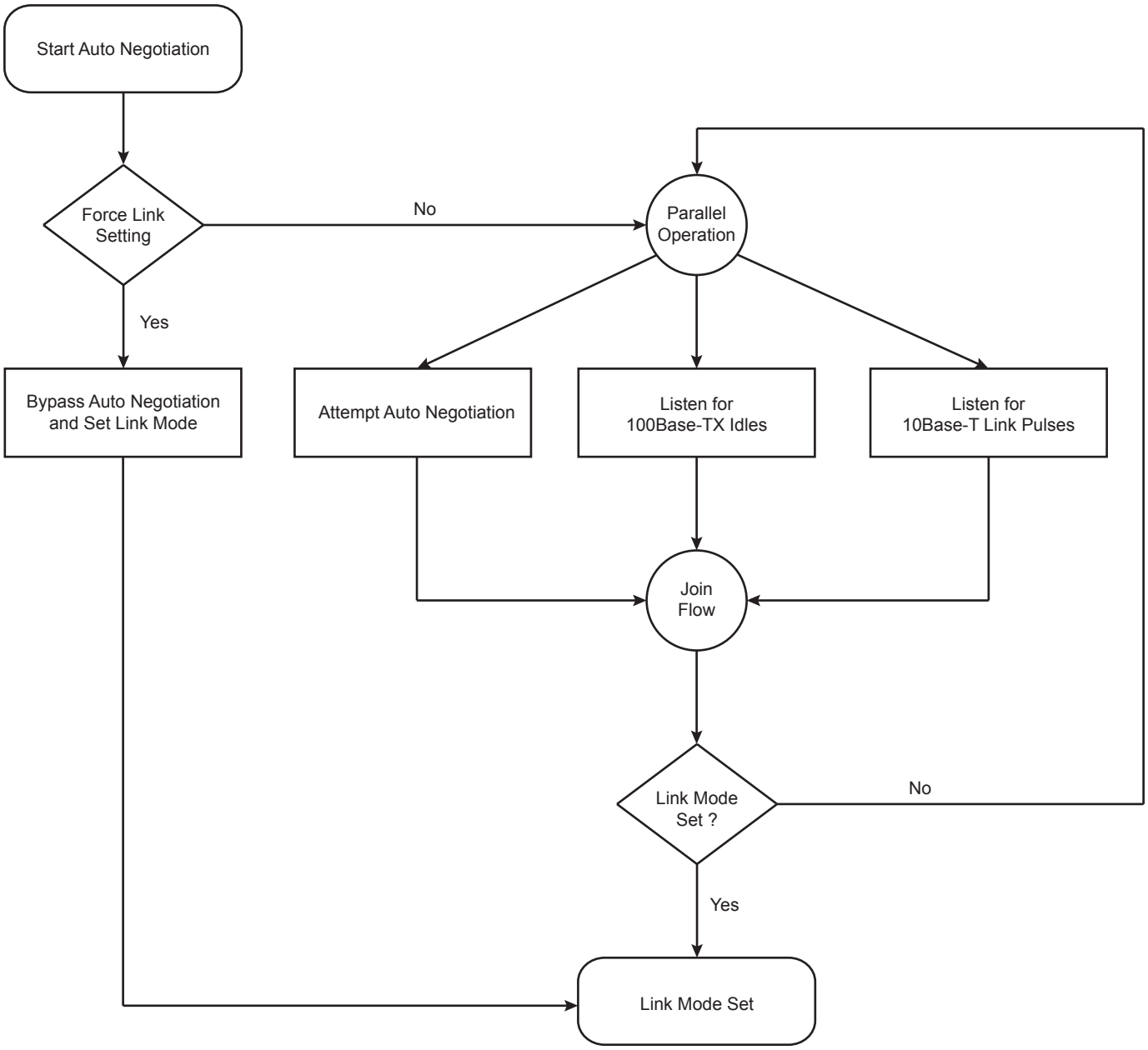


Figure 4. Auto Negotiation Flow Chart

6.9. MII Management (MIIM) Interface

The HI-5200 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the HI-5200. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows a external controller to communicate with one or more PHY devices. Each HI-5200 device is assigned a unique PHY address between 1 and 7 by its PHYAD[2:0] strapping pins. Also, every device supports the broadcast PHY address 0, as defined per the IEEE 802.3 Specification, which can be used to read/write to a single device, or write to multiple HI-5200 devices simultaneously.
- A set of 16-bit MDIO registers. Register [0:6] are required, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality.

Table 3 shows the MII Management frame format for the HI-5200.

Table 3. MII Management Frame Format

	Preamble	Start of Frame	Read/Write Op Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

6.10. Interrupt (INTRP)

INTRP (pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the PHY registers. Bits[15:8] of register 1Bh are the interrupt control bits, and are used to enable and disable the conditions for asserting the INTRP signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit 9 of register 1Fh sets the interrupt level to active high or active low.

6.11. MII Data Interface

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 Specification. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 25MHz reference clock, sourced by the PHY.
- Provides independent 4-bit wide (nibble) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The HI-5200 is configured to MII mode after it is power-up or reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- CONFIG[2:0] (pins 18, 29, 28) set to '000' (default setting).

6.12. MII Signal Definition

Table 4 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

Table 4. MII Signal Definition

MII Signal Name	Direction (with respect to PHY, HI-5200 signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

6.12.1. Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

6.12.2. Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

6.12.3. Transmit Data [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is “00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

6.12.4. Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY's reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY's reference clock.

RXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

6.12.5. Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), "5D", and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame. RXDV transitions synchronously with respect to RXC.

6.12.6. Receive Data [3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

6.12.7. Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

6.12.8. Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter, or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter, or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

6.12.9. Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

6.13. Reduced MII (RMII) Data Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 50MHz reference clock.
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The HI-5200 is configured in RMII mode after it is power-up or reset with the following:

- A 50MHz reference clock connected to REFCLK (pin 9).
- CONFIG[2:0] (pins 18, 29, 28) set to '001'.

In RMII mode, unused MII signals, TXD3 and TXD2 (pins 27 and 26 respectively), are tied to ground.

6.14. RMII Signal Definition

Table 5 describes the RMII signals for HI-5200. Refer to RMII Specification for detailed information.

Table 5. HI-5200 RMII Signal Definition

RMII Signal Name	Direction (with respect to PHY, HI-5200 signal)	Direction (with respect to MAC)	Description
REFCLK	Input	Input or Output	Synchronous 50 MHz clock reference for receive, transmit and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRSDV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RXER	Output	Input or (not required)	Receive Error

6.14.1. Reference Clock (REFCLK)

REFCLK is a continuous 50MHz clock input that provides the timing reference for TXEN, TXD[1 :0], CRSDV, RXD[1:0], and RXER.

The 50MHz REFCLK input may come from the MAC or system board (see Figure 5).

6.14.2. Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented on the RMII, and is negated prior to the first REFCLK following the final di-bit of a frame.

TXEN transitions synchronously with respect to REFCLK.

6.14.3. Transmit Data [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REFCLK. When TXEN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] is “00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[1:0] while TXEN is de-asserted are ignored by the PHY.

6.14.4. Carrier Sense/Receive Data Valid (CRSDV)

CRSDV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of carrier. This is when squelch is passed in 10Mbps mode, and when 2 non-contiguous zeroes in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRSDV.

So long as carrier detection criteria are met, CRSDV remains asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit, and it is negated prior to the first REFCLK that follows the final di-bit. The data on RXD[1:0] is considered valid once CRSDV is asserted. However, since the assertion of CRSDV is asynchronous relative to REFCLK, the data on RXD[1:0] is “00” until proper receive signal decoding takes place.

6.14.5. Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REFCLK. For each clock period in which CRSDV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. RXD[1:0] is “00” to indicate idle when CRSDV is de-asserted. Values other than “00” on RXD[1:0] while CRSDV is de-asserted are ignored by the MAC.

6.14.6. Receive Error (RXER)

RXER is asserted for one or more REFCLK periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

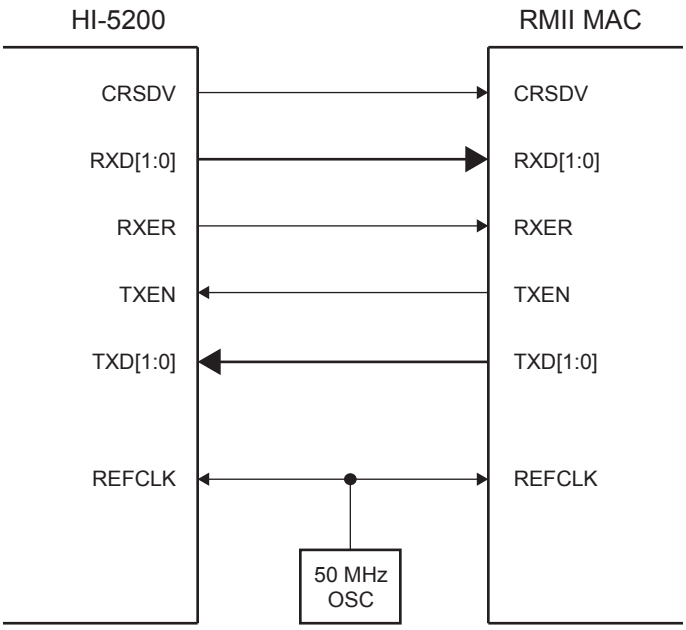
RXER transitions synchronously with respect to REFCLK. While CRSDV is de-asserted, RXER has no effect on the MAC.

6.14.7. Collision Detection

The MAC regenerates the COL signal of the MII from TXEN and CRSDV.

6.15. RMII Signal Diagram

The HI-5200 RMII pin connections to the MAC are shown in Figure 5.



OR

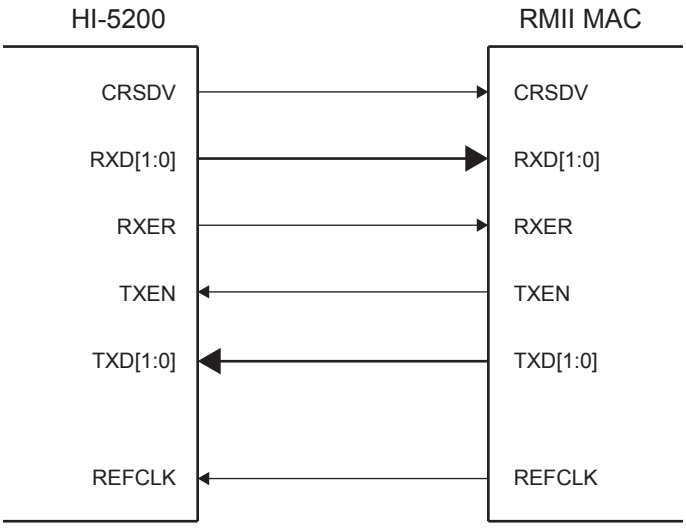


Figure 5. HI-5200 RMII Interface

6.16. HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the HI-5200 and its link partner. This feature allows the device to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner, and then assigns transmit and receive pairs of the HI-5200 accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 1Fh bit 13. MDI and MDI-X mode is selected by register 1Fh bit 14 if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X. The IEEE 802.3 Standard defines MDI and MDI-X as shown in Table 6:

Table 6. MDI/MDI-X Pin Description

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

6.16.1. Straight Cable

A straight cable connects a MDI device to a MDI-X device, or a MDI-X device to a MDI device. Figure 6 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

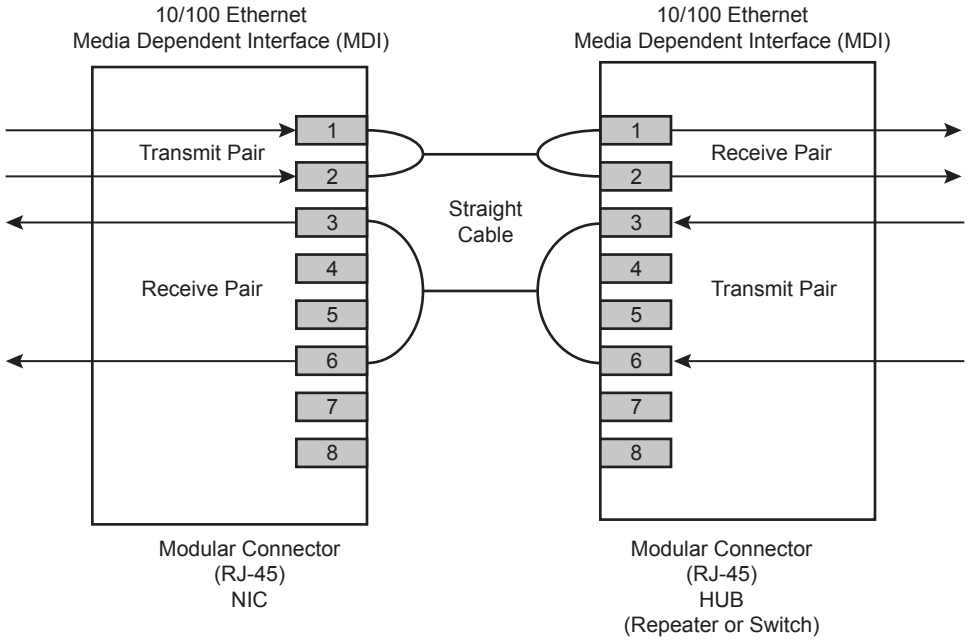


Figure 6. Typical Straight Cable Connection

6.16.2. Crossover Cable

A crossover cable connects a MDI device to another MDI device, or a MDI-X device to another MDI-X device. Figure 7 depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

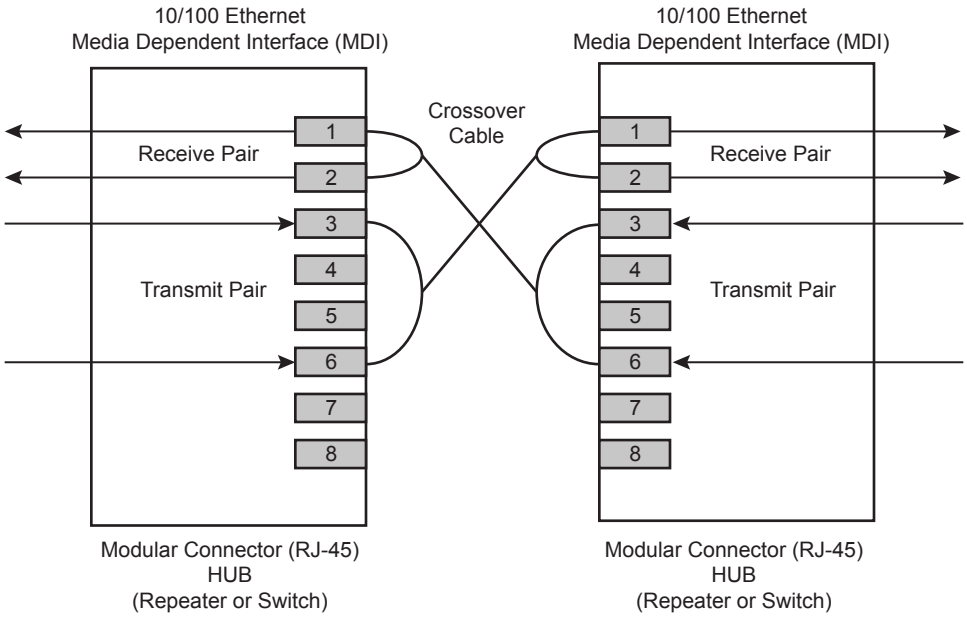


Figure 7. Typical Crossover Cable Connection