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HOLT INTEGRATED CIRCUITS INC.

# HI-8585, HI-8586

ARINC 429
Line Driver

February 2017

## DESCRIPTION

The HI-8585 and HI-8586 are CMOS integrated circuits designed to directly drive the ARINC 429 bus in an 8-pin package. Two logic inputs control a differential voltage between the output pins producing a +10 volt One, a -10 volt Zero, and a 0 volt Null.

The CMOS/TTL control inputs are translated to ARINC specified amplitudes using on board band-gap reference. A logic input is provided to control the slope of the differential output signal. Timing is set by on-chip resistor and capacitor and tested to be within ARINC requirements.

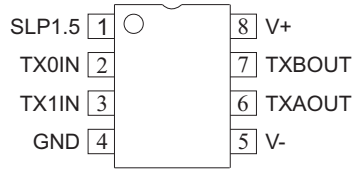
The HI-8585 has 37.5 ohms in series with each line driver output. The HI-8586 provides the option to bypass part of the output resistance so that series resistance can be used in external protection circuitry.

The HI-8585 or the HI-8586 along with the HI-8588 or the Hi-8591 line receivers offer the smallest options available to get on and off the ARINC bus.

## FEATURES

- Direct ARINC 429 line driver interface in a small package
- On-chip band-gap reference to set output levels
- On-chip line driver slope control and selection by logic input
- Low current 12 to 15 volt supplies
- CMOS / TTL logic pins
- Plastic and ceramic package options - surface mount and DIP
- Thermally enhanced SOIC packages
- Industrial & extended temperature ranges

## PIN CONFIGURATION




## SUPPLY VOLTAGES

V+ = 12V to 15V
V- = -12V to -15V

## FUNCTION TABLE

| TX1IN | TX0IN | SLP1.5 | TXAOUT | TXBOUT | SLOPE |
|---|---|---|---|---|---|
| 0 | 0 | X | 0V | 0V | N/A |
| 0 | 1 | 0 | -5V | 5V | 10$\mu$s |
| 0 | 1 | 1 | -5V | 5V | 1.5$\mu$s |
| 1 | 0 | 0 | 5V | -5V | 10$\mu$s |
| 1 | 0 | 1 | 5V | -5V | 1.5$\mu$s |
| 1 | 1 | X | 0V | 0V | N/A |

## PIN DESCRIPTION TABLE

| PIN | SYMBOL | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 1 | SLP 1.5 | LOGIC INPUT | CMOS OR TTL, V+ IS OK |
| 2 | TX0IN | LOGIC INPUT | CMOS OR TTL |
| 3 | TX1IN | LOGIC INPUT | CMOS OR TTL |
| 4 | GND | POWER | GROUND |
| 5 | V- | POWER | -12 TO -15 VOLTS |
| 6 | TXAOUT | OUTPUT | LINE DRIVER TERMINAL A |
| 7 | TXBOUT | OUTPUT | LINE DRIVER TERMINAL B |
| 8 | V+ | POWER | +12 TO +15 VOLTS |

# FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the line driver. The +5V and -5V levels are generated internally using a on-chip band-gap reference. Currents for slope control are set by zener voltages across on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as the HI-6010, HI-3282 or HI-8282. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an “A” side internal capacitor while the “B” side is enabled to -5V. The charging current is selected by the SLP1.5 pin. If the SLP1.5 pin is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If SLP1.5 is low, the rise and fall times are 10µs.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8585 as exists on the Hi-8382.

The HI-8585 has 37.5 ohms in series with each output and the HI-8586 has 2 ohms in series with each output. The HI-8586 is for applications where external series resistance is required, typically for lightning protection devices.

Both the HI-8585 and HI-8586 are built using high-speed CMOS technology. Care should be taken to ensure the V+ and V- supplies are locally decoupled and that the input waveforms are free from negative voltage spikes which may upset the chip’s internal slope control circuitry.

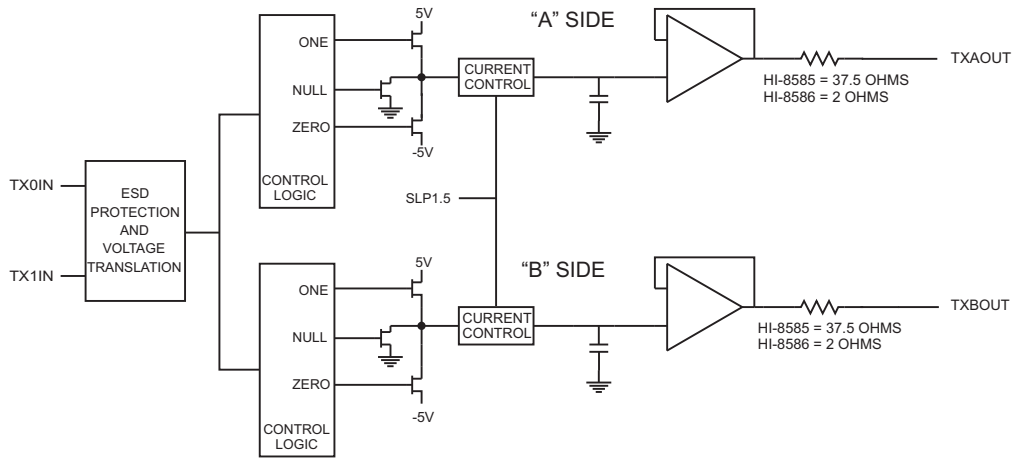



FIGURE 1 - LINE DRIVER BLOCK DIAGRAM

## APPLICATION INFORMATION

Figure 2 shows a possible application of the HI-8585/86 interfacing an ARINC transmit channel from the HI-6010.

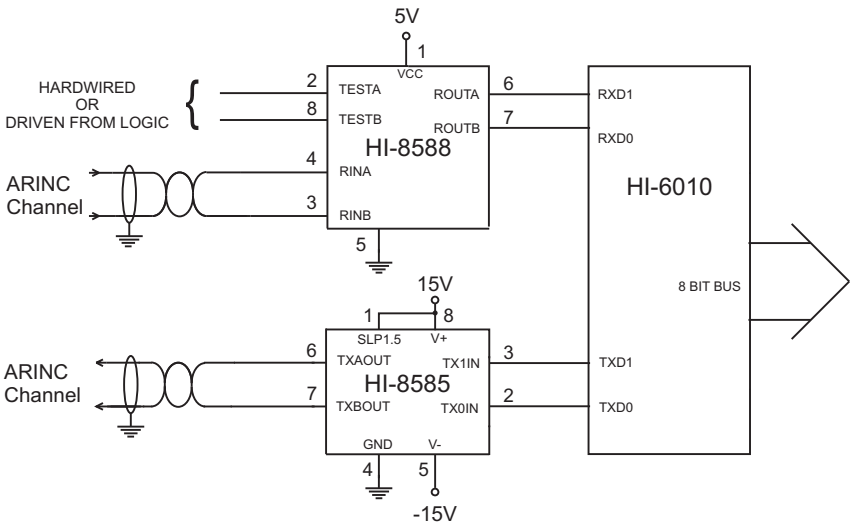



FIGURE 2 - APPLICATION DIAGRAM

## ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages
V+ ..... 20V
V- ..... -20V

DC current per input pin ..... +10mA

Power dissipation at 25°C
plastic DIP ..... 1.0W, derate 10mW/°C
ceramic DIP ..... 0.5W, derate 7mW/°C

Solder Temperature (Reflow) ..... 260°C

Storage Temperature ..... -65°C to +150°C

## RECOMMENDED OPERATING CONDITIONS

Supply Voltages
V+.....+11.4V to +16.5V
V-..... -11.4V to -16.5V

Temperature Range
Industrial .....-40°C to +85°C
Extended .....-55°C to +125°C

*NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.*

## DC ELECTRICAL CHARACTERISTICS

V+ = +12V to +15V, V- = -12V to -15V, $T_A$ = Operating Temperature Range (unless otherwise stated)

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input voltage (TX1IN, TX0IN, SLP1.5) | | | | | | |
| high | $V_{IH}$ | | 2.1 | - | V+ | volts |
| low | $V_{IL}$ | | - | - | 0.5 | volts |
| Input current (TX1IN, TX0IN, SLP1.5) | | | | | | |
| source | $I_{IH}$ | $V_{IN}$ = 0V | - | - | 0.1 | $\mu$A |
| sink | $I_{IL}$ | $V_{IN}$ = 5V | - | - | 0.1 | $\mu$A |
| ARINC output voltage (Differential) | | | | | | |
| one | $V_{DIFF1}$ | no load; TXAOUT - TXBOUT | 9.00 | 10.00 | 11.00 | volts |
| zero | $V_{DIFF0}$ | no load; TXAOUT - TXBOUT | -11.00 | -10.00 | -9.00 | volts |
| null | $V_{DIFFN}$ | no load; TXAOUT - TXBOUT | -0.50 | 0 | 0.50 | volts |
| ARINC output voltage (Ref. to GND) | | | | | | |
| one or zero | $V_{DOUT}$ | no load & magnitude at pin | 4.50 | 5.00 | 5.50 | volts |
| null | $V_{NOUT}$ | no load | -0.25 | 0 | 0.25 | volts |
| Operating supply current | | SLP1.5 = V+ | | | | |
| V+ | $I_{DD}$ | TX1IN & TX0IN = 0V: no load | - | 6.0 | 14.0 | mA |
| V- | $I_{EE}$ | TX0IN & TX1IN = 0V: no load | -14.0 | -6.0 | - | mA |
| ARINC output impedence | $Z_{OUT}$ | | | | | |
| HI-8585 | | | - | 37.5 | - | ohms |
| HI-8586 | | | - | - | 2 | ohms |

## AC ELECTRICAL CHARACTERISTICS

V+ = 15.0V, V- = -15V, $T_A$ = Operating Temperature Range (unless otherwise stated)

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Line Driver propagation delay | | defined in Figure 3, no load | | | | |
| Output high to low | $t_{phlx}$ | | - | 500 | - | ns |
| Output low to high | $t_{plhx}$ | | - | 500 | - | ns |
| Line Driver transition times | | | | | | |
| High Speed | | SLP 1.5 = V+ | | | | |
| Output high to low | $t_{fx}$ | pin 1 = logic 1 | 1.0 | 1.5 | 2.0 | µs |
| Output low to high | $t_{rx}$ | pin 1 = logic 1 | 1.0 | 1.5 | 2.0 | µs |
| Low Speed | | SLP 1.5 = GND | | | | |
| Output high to low | $t_{fx}$ | pin 1 = logic 1 | 5.0 | 10.0 | 15.0 | µs |
| Output low to high | $t_{rx}$ | pin 1 = logic 1 | 5.0 | 10.0 | 15.0 | µs |
| Input capacitance (1) | | | | | | |
| logic | $C_{IN}$ | | - | - | 10 | pF |

Notes:
1. Guaranteed but not tested

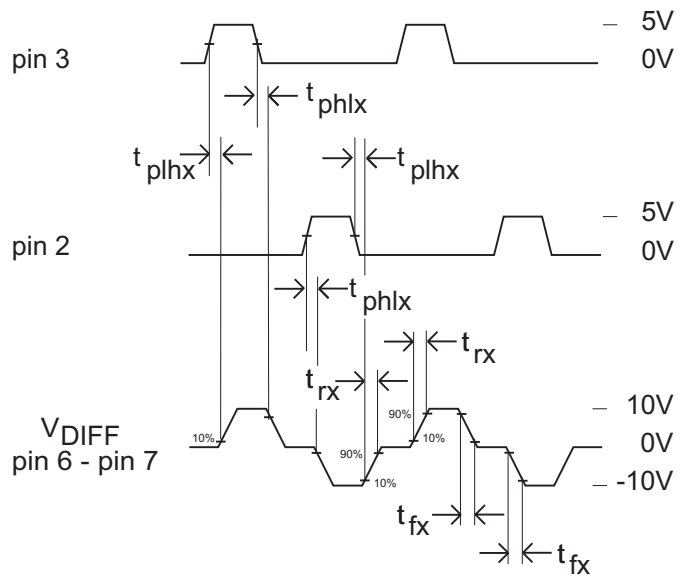



FIGURE 3 - LINE DRIVER TIMING

## PACKAGE THERMAL CHARACTERISTICS

### MAXIMUM ARINC LOAD [9, 10]

| PACKAGE STYLE [1] | ARINC 429 DATA RATE | SUPPLY CURRENT (mA) [2] | | | JUNCTION TEMP, Tj (°C) | | |
|---|---|---|---|---|---|---|---|
| | | Ta = 25°C | Ta = 85°C | Ta=125°C | Ta = 25°C | Ta = 85°C | Ta=125°C |
| 8 Lead Plastic DIP | Low Speed [3] | 16.8 | 17.2 | 16.9 | 58 | 116 | 157 |
| | High Speed [4] | 27.3 | 26.7 | 25.9 | 75 | 132 | 169 |
| 8 Lead Plastic ESOIC [5] | Low Speed | 17.4 | 17.5 | 16.9 | 68 | 126 | 166 |
| | High Speed | 27.6 | 27.1 | 25.9 | 97 | 147 | 186 |
| 8 Lead Plastic ESOIC [6] | Low Speed | 17.1 | 17.2 | 16.7 | 52 | 110 | 151 |
| | High Speed | 27.3 | 27.1 | 26.2 | 57 | 112 | 157 |

### TXAOUT and TXBOUT Shorted to Ground [7, 8, 9, 10]

| PACKAGE STYLE [1] | ARINC 429 DATA RATE | SUPPLY CURRENT (mA) [2] | | | JUNCTION TEMP, Tj (°C) | | |
|---|---|---|---|---|---|---|---|
| | | Ta = 25°C | Ta = 85°C | Ta=125°C | Ta = 25°C | Ta = 85°C | Ta=125°C |
| 8 Lead Plastic DIP | Low Speed [3] | 53.6 | 50.7 | 52.2 | 131 | 181 | 217 |
| | High Speed [4] | 46.9 | 38.7 | 42.5 | 135 | 181 | 219 |
| 8 Lead Plastic ESOIC [5] | Low Speed | 46.4 | 47.6 | 68.1 | 167 | 191 | 221 |
| | High Speed | 42.1 | 43.8 | 67.1 | 177 | 212 | 223 |
| 8 Lead Plastic ESOIC [6] | Low Speed | 48.5 | 45.6 | 46.1 | 112 | 161 | 186 |
| | High Speed | 46.8 | 41.1 | 40.5 | 116 | 168 | 197 |

Notes:

1. All data taken in still air on devices soldered to single layer copper PCB (3" X 4.5" X .062").
2. At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
5. 8 Lead Plastic ESOIC (Thermally enhanced SOIC with built in heat sink). Heat sink not soldered to the PCB.
6. 8 Lead Plastic ESOIC (Thermally enhanced SOIC with built in heat sink). Heat sink soldered to the PCB.
7. Similar results would be obtained with TXAOUT shorted to TXBOUT.
8. For applications requiring survival with continuous short circuit, operation above Tj = 175°C is not recommended.
9. Data will vary depending on air flow and the method of heat sinking employed.
10. Current values are per supply.

## HEAT SINK - ESOIC PACKAGES

An 8-pin thermally enhanced SOIC package is used for the HI-8585/HI-8586 products. The ESOIC package includes a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated from the chip and can be soldered to any ground or power plane. However, since the chip's substrate is at V+, connecting the heat sink to this power plane is recommended to avoid coupling noise into the circuit.

## ORDERING INFORMATION

**HI - 85XX xx x x**

| PART NUMBER | LEAD FINISH |
|---|---|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|---|---|---|---|
| I | -40°C TO +85°C | I | No |
| T | -55°C TO +125°C | T | No |
| M | -55°C TO +125°C | M | Yes |

| PART NUMBER | PACKAGE DESCRIPTION |
|---|---|
| PD | 8 PIN PLASTIC DIP (8P) |
| PS | 8 PIN PLASTIC NARROW BODY ESOIC (8HNE) |
| CR | 8 PIN CERDIP (8D) not available Pb-free |

| PART NUMBER | OUTPUT SERIES RESISTANCE | |
|---|---|---|
| | BUILT-IN | REQUIRED EXTERNALLY |
| 8585 | 37.5 Ohms | 0 |
| 8586 | 2 Ohms | 35.5 Ohms |

Legend: ESOIC - Thermally Enhanced Small Outline Package (SOIC) with built-in heat sink

**HI - 8585 PS I - N**

| PART NUMBER | LEAD FINISH |
|---|---|
| N | Tin / Lead (Sn / Pb) Solder - No heat-sink |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|---|---|---|---|
| I | -40°C TO +85°C | I | No |

| PART NUMBER | PACKAGE DESCRIPTION |
|---|---|
| PS | 8 PIN PLASTIC NARROW BODY SOIC (8HN) |

| PART NUMBER | OUTPUT SERIES RESISTANCE | |
|---|---|---|
| | BUILT-IN | REQUIRED EXTERNALLY |
| 8585 | 37.5 Ohms | 0 |

Legend: SOIC - Small Outline Package (No Heat-Sink)

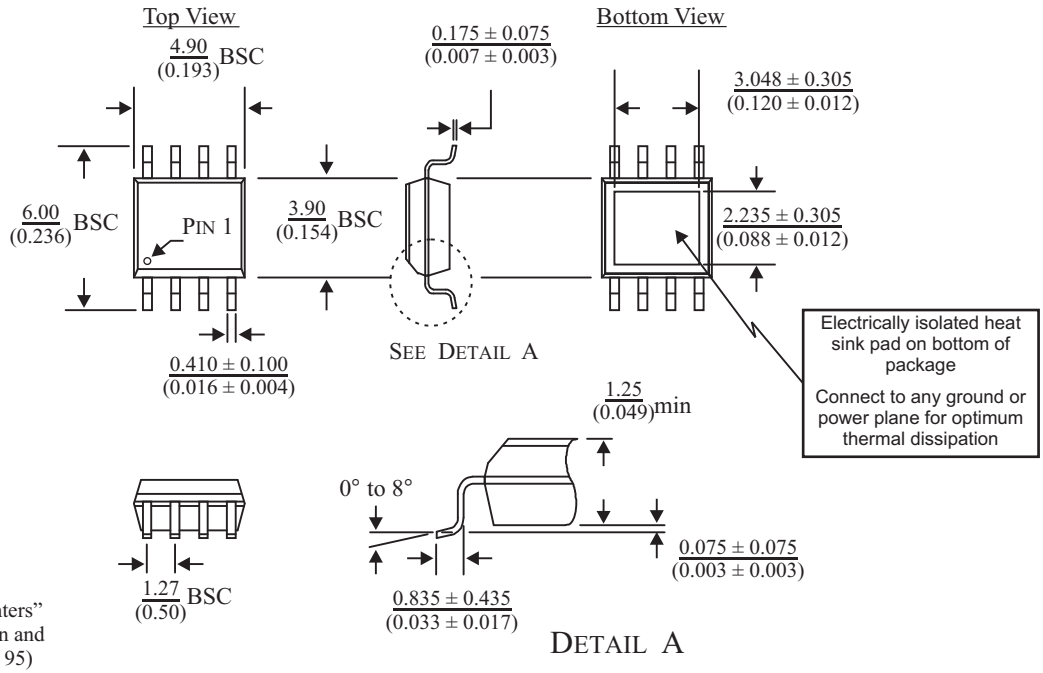
# REVISION HISTORY

| P/N | Rev | Date | Description of Change |
|---|---|---|---|
| DS8585 | M | 05/08/08 | Clarified temperature ranges and added HI-8585PSI-N to Ordering Information |
| | N | 09/09/11 | Replaced references of setting ARINC output levels with zener diodes to using a band-gap reference circuit. |
| | O | 02/08/17 | Update package drawings. Update solder reflow temperature. |

## 8-PIN PLASTIC SMALL OUTLINE (ESOIC) - NB
(Narrow Body, Thermally Enhanced)

*millimeters (inches)*

Package Type: 8HNE

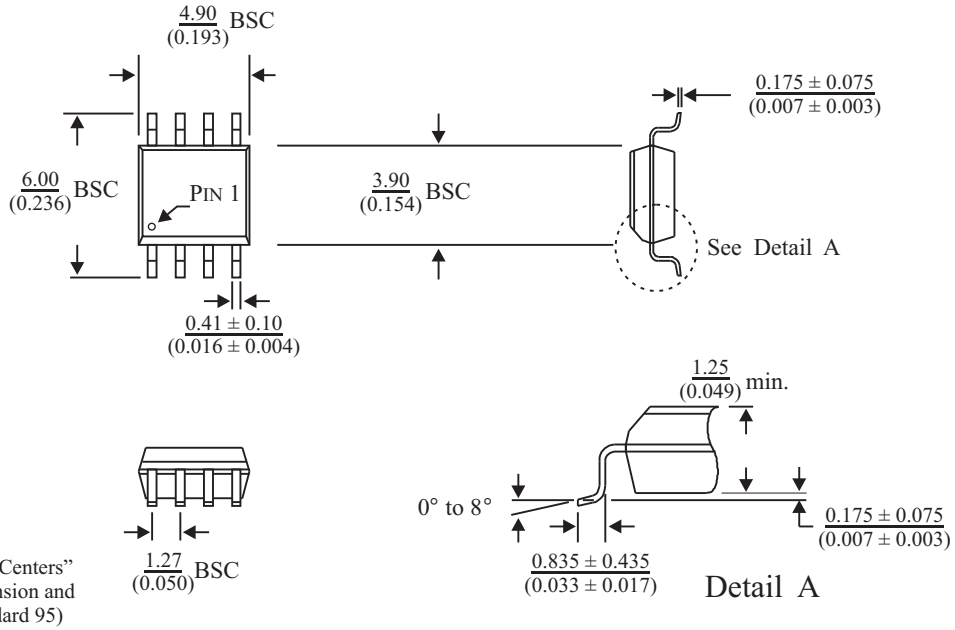



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

## 8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

*millimeters (inches)*

Package Type: 8HN

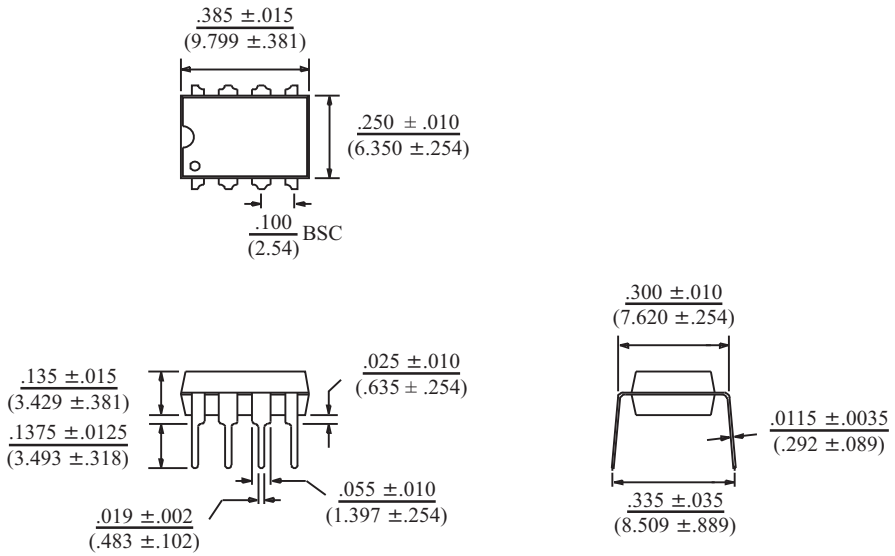



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

## 8-PIN PLASTIC DIP

*inches (millimeters)*

Package Type: 8P

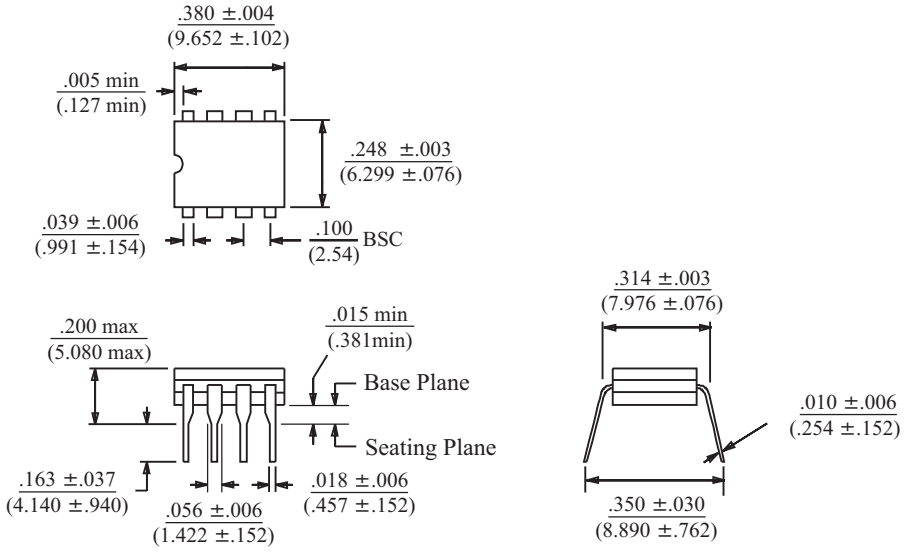



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

## 8-PIN CERDIP

*inches (millimeters)*

Package Type: 8D

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