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HiGig™ MAC

Overview

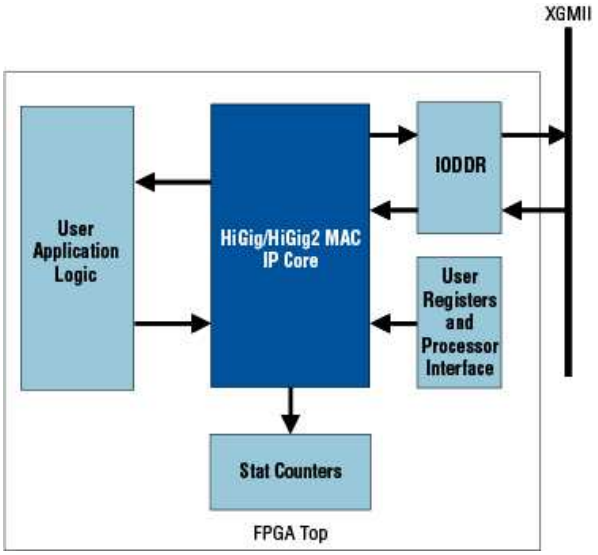
The **HiGig™ MAC** transmits and receives data between a host processor and a HiGig™ / Ethernet network that enables networking customers to add features like quality of service (QoS), port trunking, mirroring across devices, and link aggregation at higher layers of the OSI network model. The HiGig™ MAC ensures that the Media Access rules specified in the 802.3ae IEEE standard and HiGig™ Protocol definitions are met while transmitting a frame of data over Ethernet. On the receive side, it extracts the different components of a frame and transfers them to higher applications through a FIFO interface.

The **HiGig™ / Ethernet MAC IP core** is a user-configurable IP core, which allows the configuration of the IP and generation of a netlist and simulation file for use in designs. Please note that generating a bitstream may be prevented or the bitstream may have time logic present unless a license for the IP is purchased. The HiGig™ MAC IP core from Lattice supports the **LatticeECP3** and **LatticeSC/ M** FPGA families.

Features

- Compliant to the Broadcom HiGig and HiGig2 Protocol Definitions
- 64-bit wide internal data path operating at a maximum frequency of 187.5 MHz (LatticeECP3 maximum 156 MHz)
- XGMII interface to the PHY layer (using IODDR external to the core)
- XAUI interface to the PHY layer (using PCS/SERDES external to the core)
- Simple FIFO interface with user's application
- Optional multicast address filtering
- Transmit and receive statistics vector
- Optional statistics counters of length from 16 to 40 (external to the core)
- Variable-sized packet transmission with fixed sized messaging capability (HiGig2 Only)
- Programmable Inter Frame Gap
- Supports:
  - Full duplex operation
  - Flow control using PAUSE frames (for HiGig) and messaging (for HiGig2)
  - Automatic padding of short frames
  - Optional FCS generation during transmission
  - Optional FCS stripping during reception
  - Jumbo frames up to 16k
  - Inter frame Stretch Mode during transmission
  - Deficit Idle Count

Core Block Diagram



Performance and Resource Utilization

LatticeECP3 FPGA Family

HiGig2 Results for LatticeECP3[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	fMAX (MHz)
With Multicast Address Filtering and 16-bit Statistics Counters	3624	4706	3386	83	4	157

1. Performance and utilization data are generated using an LFE3-35EA-7FN672CES device with Lattice Diamond 1.1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.
2. The HiGig Ethernet MAC IP core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeECP3 series FPGA. Thus the application implementing the HiGig MAC specification will utilize I/O pins.

HiGig Results for LatticeECP3[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	fMAX (MHz)
With Multicast Address Filtering and 16-bit Statistics Counters	3280	4135	3121	78	4	158

1. Performance and utilization data are generated using an LFE3-35EA-7FN672CES device with Lattice Diamond 1.1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.
2. The HiGig Ethernet MAC IP core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeECP3 series FPGA. Thus the application implementing the HiGig MAC specification will utilize I/O pins.

LatticeSC/M FPGA Family

HiGig2 Results for LatticeSC/ M[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	fMAX (MHz)
With Multicast Address Filtering and 16-bit Statistics Counters	3417	4879	3380	83	4	206

1. Performance and utilization data are generated using an LFSCM3GA25EP1-5F900C device with Lattice Diamond 1.1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSCM family.
2. The HiGig2 Ethernet MAC IP core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeSCM series FPGA. Thus the application implementing the HiGig2 MAC specification will utilize I/O pins.

HiGig Results for LatticeSC/ M[1]

Mode	SLICEs	LUTs	Registers	External Pins[2]	sysMEM EBRs	fMAX (MHz)
With Multicast Address Filtering and 16-bit Statistics Counters	2995	4188	3062	78	4	204

1. Performance and utilization data are generated using an LFSCM3GA25EP1-5F900C device with Lattice Diamond 1.1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSCM family.
2. The HiGig Ethernet MAC IP core itself does not use any external pins. However, in an application the core is used together IODDR and I/O Buffers integrated in the LatticeSCM series FPGA. Thus the application implementing the HiGig MAC specification will utilize I/O pins.

Ordering Information

Family	Part Numbers
LatticeECP3	HIG-MAC-E3-U3
LatticeSC	HIG-MAC-SC-U3

Evaluate/ Purchase: Unlike other LatticeCORE IP, the HiGig™ MAC IP core cannot be directly downloaded from the Lattice IPexpress Server. Please request this IP from Lattice at **lic_admn@latticesemi.com** and include your name, company, and complete contact information. A setup file for installation of the IP into IPexpress will be sent to you. Execute the setup file and then use IPexpress to evaluate and configure the IP core. For more information on customizing an IP please read the **IPexpress Quick Start Guide**.

Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.