



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



HMC1035* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC1035LP6G Evaluation Board

DOCUMENTATION

Application Notes

- Frequency Hopping with Hittite PLLVCOs Application Note
- PLL & PLLVCO Serial Programming Interface Mode Selection Application Note
- Power-Up & Brown-Out Design Considerations for RF PLL +VCO Products Application Note
- Wideband RF PLL+VCO and Clock Generation Products FAQs

Data Sheet

- HMC1035 Data Sheet

REFERENCE MATERIALS

Quality Documentation

- HMC Legacy PCN: LP6CE and LP6GE QFN - Alternate assembly source
- Package/Assembly Qualification Test Report: LP6, LP6C, LP6G (QTR: 2014-00368)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

DESIGN RESOURCES

- HMC1035 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC1035 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz****General Description**

The HMC1035LP6GE is a low-noise, wide-band 3.3 V clock generator IC with a fractional-N Phase Locked Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO). The device provides differential clock outputs between 25 MHz and 2500 MHz range. The HMC1035LP6GE features a low noise Phase Detector (PD) and Delta-Sigma modulator, capable of operating at up to 100 MHz which permits wider loop-bandwidths and excellent spurious performance.

The HMC1035LP6GE features industry leading phase noise and jitter performance, across the operating range, that enable it to improve link level jitter performance, Bit-Error-Rates (BER) and eye diagram metrics. The superior noise floor (< -162 dBc/Hz) makes the HMC1035LP6GE an ideal source for a variety of applications –such as clock references for high speed data converters, physical layer devices (PHY), serializer/deserializer (SERDES) circuits, FPGAs and processors. The HMC1035LP6GE can also be used as an LO for 10G/40G/100G optical modules and transponders, as well as primary reference clock for 10G/40G/100G line cards, and for jitter attenuation and frequency translation.

The differential output of the HMC1035LP6GE can be set to either External Termination, which could be used for LVPECL operation, or Internal Termination for operation in an LVDS compatible mode or LVPECL, see [Figure 18](#). Additionally, an output swing adjustment makes the device flexible and compatible with a wide variety of signal level requirements. The output can be internally terminated to reduce component count and cost or could be terminated externally using standard LVPECL termination methods such as [Figure 21](#). An Output Mute function allows the user to shut off the outputs, such as may be required for board testing or debugging. The LVPECL/LVDS, amplitude select and Output Mute function are all programmed SPI serial programming

The HMC1035LP6GE is designed to select between a Power Priority or a Performance Priority mode. The Power Priority setting reduces the current consumption of the part, whereas the Performance Priority setting improves the Jitter and Phase Noise performance.

The 24 bit Delta-Sigma Modulator further enhances Hittite's Exact Frequency Mode, which enables users to generate output frequencies with 0 Hz frequency error in many applications.

HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR 25 - 2500 MHz



Electrical Specifications, VPPCP, VDDLs, 3VRVDD, VCC1, VCC2, VCCHF, VCCPS, VCCPD, = 3.3V Min & Max Specified across Temperature -40 °C to 85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
OUT_N, OUT_P Output Characteristics					
Output Frequency		25		2500	MHz
Differential Output Amplitude	Gain Setting = 0000		690		mVpp
	Gain Setting = 0001		780		mVpp
	Gain Setting = 0010		900		mVpp
	Gain Setting = 0011		980		mVpp
	Gain Setting = 0100		1100		mVpp
	Gain Setting = 0101		1260		mVpp
	Gain Setting = 0110		1400		mVpp
	Gain Setting = 0111		1590		mVpp
	Gain Setting = 1000		1810		mVpp
	Gain Setting = 1001		1980		mVpp
	Gain Setting = 1010		2250		mVpp
Gain Setting = 1011		2560		mVpp	
Output Common Mode Voltage					
LVDS Mode			1.2		mV
LVPECL Mode			2.0		V
Output Rise and Fall Time	LVDS mode, Gain = 0001		120		ps
Output Rise and Fall Time	LVPECL mode, Gain = 0110		130		ps
Duty Cycle	AC coupled, measured at the 0 V crossing, 622.080 MHz and 2.5 GHz Outputs	49	50	51	%
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = $2^{19} - 1$	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional Nominal Divide Ratio Varies (-3 / +4) Dynamically Max	20		524,283	
CLKIN Input Characteristics					
Max Input Frequency ²				350	MHz
Input Amplitude	AC Coupled ^[1]	0.2		3.3	Vp-p
Input Capacitance				5	pF
Input Slew Rate		157			mV/ns
14 Bit R-Divider Range				16,383	
Phase Detector (PD) ^[2]					
PD Frequency Fractional Mode		0.006		100	MHz
PD Frequency Integer Mode		0.006		100	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		μA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 1 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-152		dBc/Hz
Logic Inputs					
Vsw	Switching threshold for logic levels	40	50	60	% DVDD
Logic Outputs					
VOH Output High Voltage			DVDD		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR 25 - 2500 MHz



Electrical Specifications (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Voltages					
+ 3.3V Supplies	AVDD, VPPCP, VDDL3,3VRVDD, DVDD3V, VCC1, VCC2, VCCHF, VCCPS, VCCPD	3.15	3.3	3.5	V
Power Supply Currents					
+3.3V	LVPECL, Performance Priority Mode, 2.5 GHz output, Excluding Load		186		mA
	LVPECL Performance Priority Mode, 2.5 GHz output, Includes Termination		218		mA
	LVPECL Performance Priority Mode, 622.080 MHz Output, Includes Termination		237		mA
	LVDS, Power Priority Mode, 2.5 GHz Output, Includes Termination		173		mA
	LVDS, Power Priority Mode, 622.080 MHz Output, Includes Termination		221		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		μA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		5		mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Minimum DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		μs
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-227		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-226		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
Phase Jitter RMS, Integer Mode	622.08 MHz Output , 12 kHz to 20 MHz		107		fs
	2.5 GHz Output 12 kHz -20MHz		97		fs
Phase Jitter RMS, Fractional Mode	622.08 MHz Output , 12 kHz to 20 MHz		125		fs
	2.5 GHz Output 12 kHz -20MHz		110		fs
<p>[1] Measurements made are AC coupled into a 100 differential load (Except Phase Noise).</p> <p>[2] The maximum phase detector frequency can only be achieved if the minimum N value is respected, eg in the case of fractional feedback mode, the maximum PFD rate = $f_{vco}/20$ or 100 MHz whichever is less. Operation > 70MHz may require offset currents to be disabled and reenabled.</p>					

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**



Figure 1. Typical Phase Noise, Integer Mode, Power Priority^[1]

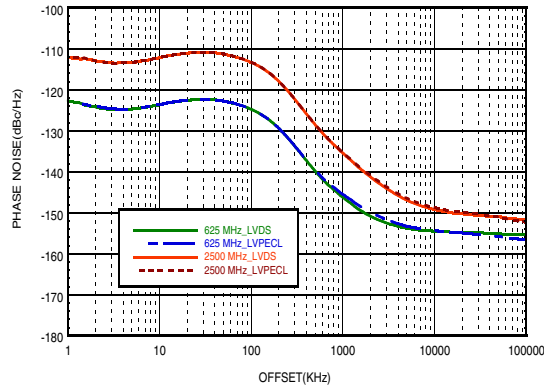


Figure 2. Typical Phase Noise, Integer Mode, Performance Priority^[1]

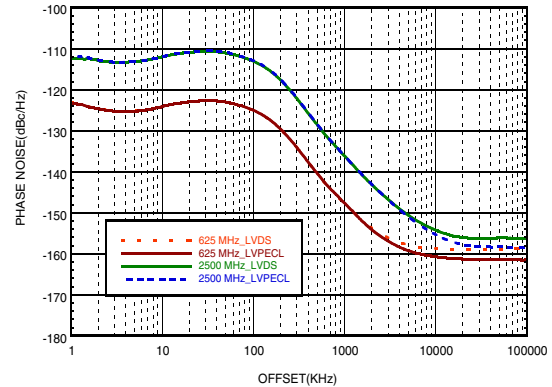


Figure 3. Typical Phase Noise, Fractional Mode, Power Priority^[1]

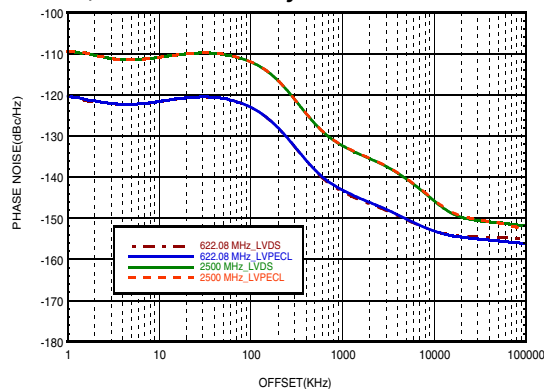


Figure 4. Typical Phase Noise, Fractional Mode, Performance Priority^[1]

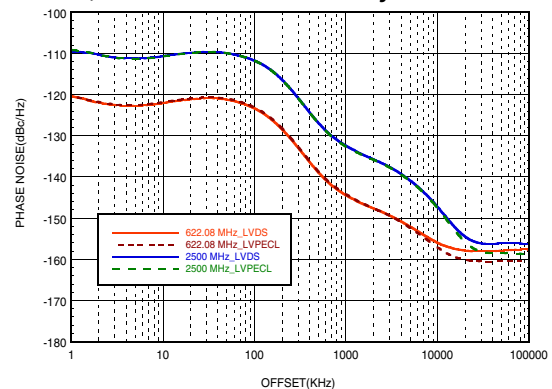


Figure 5. Integer Phase Noise vs Reference Source^[2]

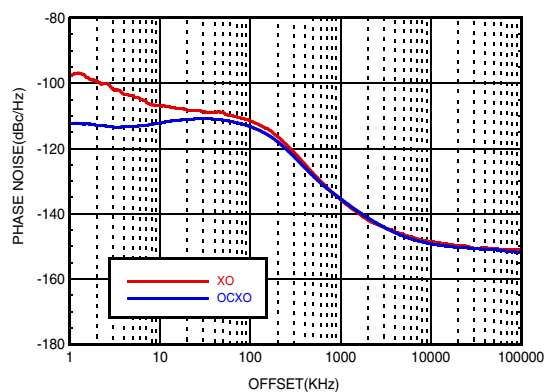
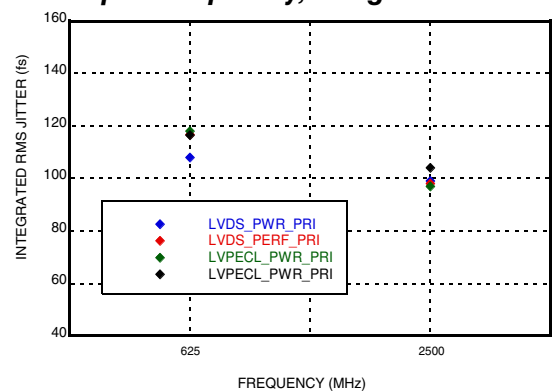


Figure 6. Jitter from Integrated Phase Noise vs Output Frequency, Integer Mode^[2]



[1] The PN plot is measured with a 100MHz OXCO followed with a divide by 2, using the Loop Filter in the Loop Filter Configuration Table

[2] The PN plot is measured with 50 MHz Crystal Oscillator (red) versus a 50MHz OXCO (blue).

[3] Jitter is integrated over a 12kHz to 20MHz Band

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**



Figure 7. Jitter from Integrated Phase Noise vs. Frequency, Fractional Mode^[3]

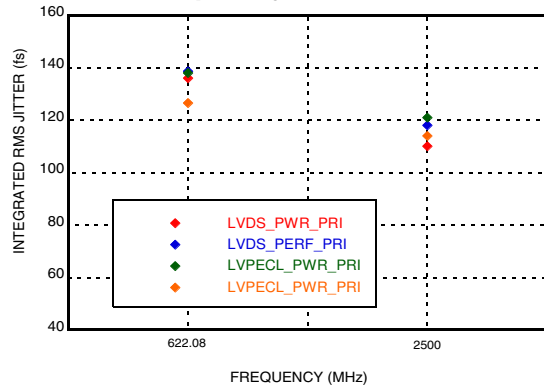


Figure 8. Lock Time vs. Phase Error^[4]

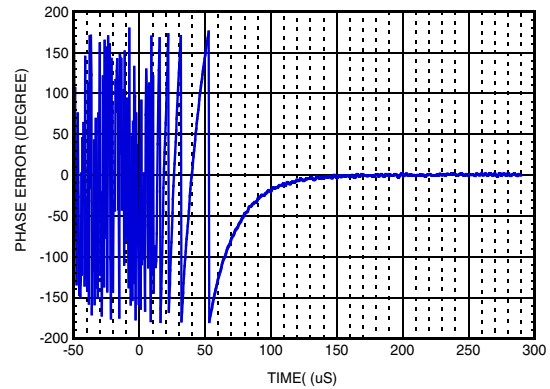


Figure 9. Lock Time vs Frequency Error^[4]

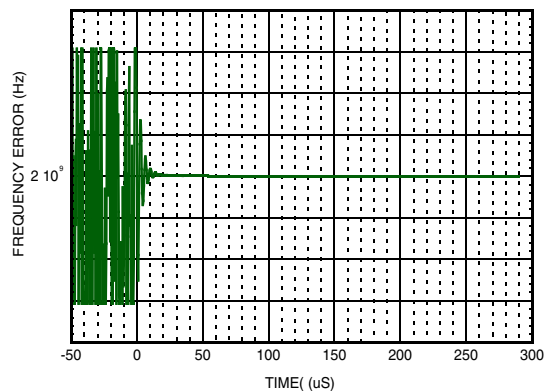


Figure 10. Output Amplitude vs Output Frequency^[5]

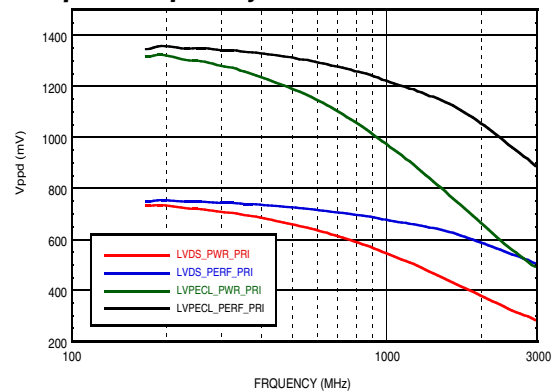


Figure 11. Output Rise Time vs. Output Frequency^[6]

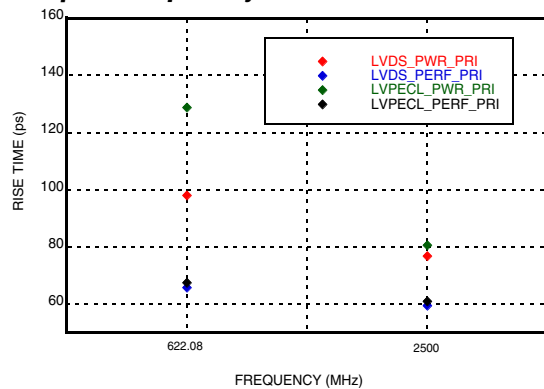
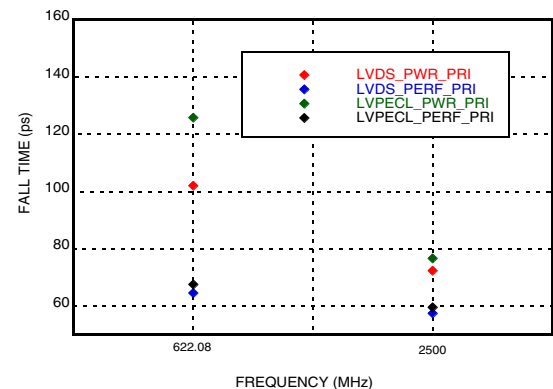


Figure 12. Output Fall Time vs. Output Frequency



[4] The HMC1035LP6GE has a preloaded register file for a 2GHz Output and time is measured from VCO disable to VCO enable, using the Loop Filter in the Loop Filter Configuration Table.

[5] The output signal amplitude is measured with HMC1035 AC coupled to a 100 ohm differential load instrument

[6] Measured at 20% to 80% levels.

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**



Figure 13. Output Duty Cycle vs. Output Frequency^[7]

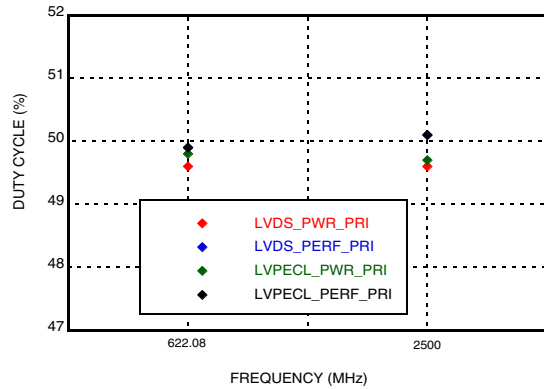


Figure 14. Supply Current vs. Output Frequency^[8]

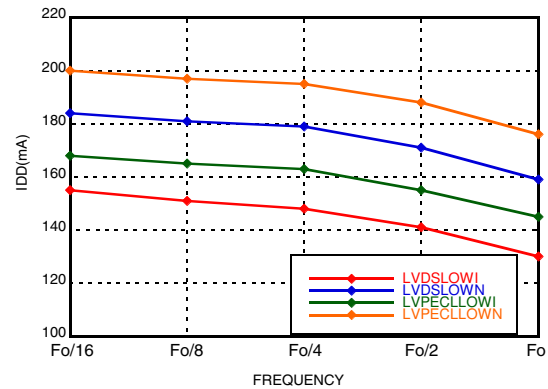


Figure 15. Output Amplitude vs. Gain Setting over Temperature

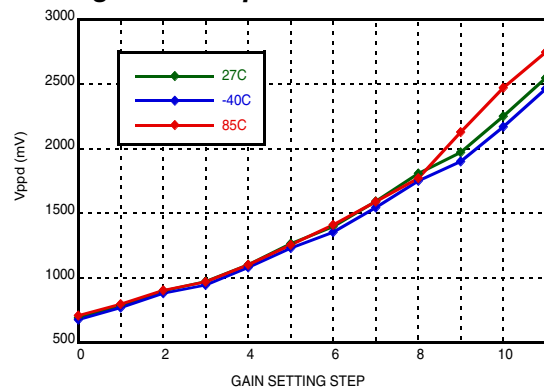
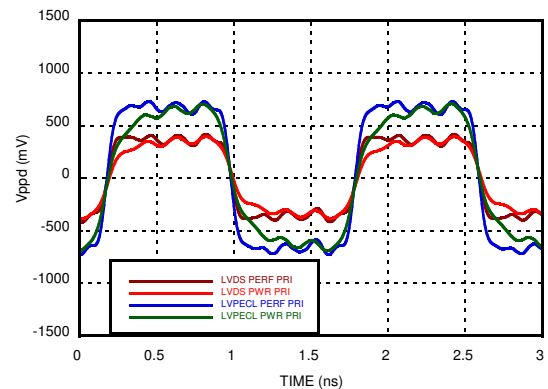


Figure 16. Out Waveform, Performance Priority and Power Priority in LVDS and LVPECL Mode



[7] Duty Cycle is measured with the Output AC coupled at the 0 crossing level.

[8] The current is measured at Nominal VCO VDD Supply under Fractional Locked Condition by varying different the output divider ratio.

Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (Ω)	R3 (Ω)	R4 (Ω)	Loop Filter Design
127	390	10	82	82	750	300	300	
75	270	27	200	390	430	390	390	

HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR 25 - 2500 MHz

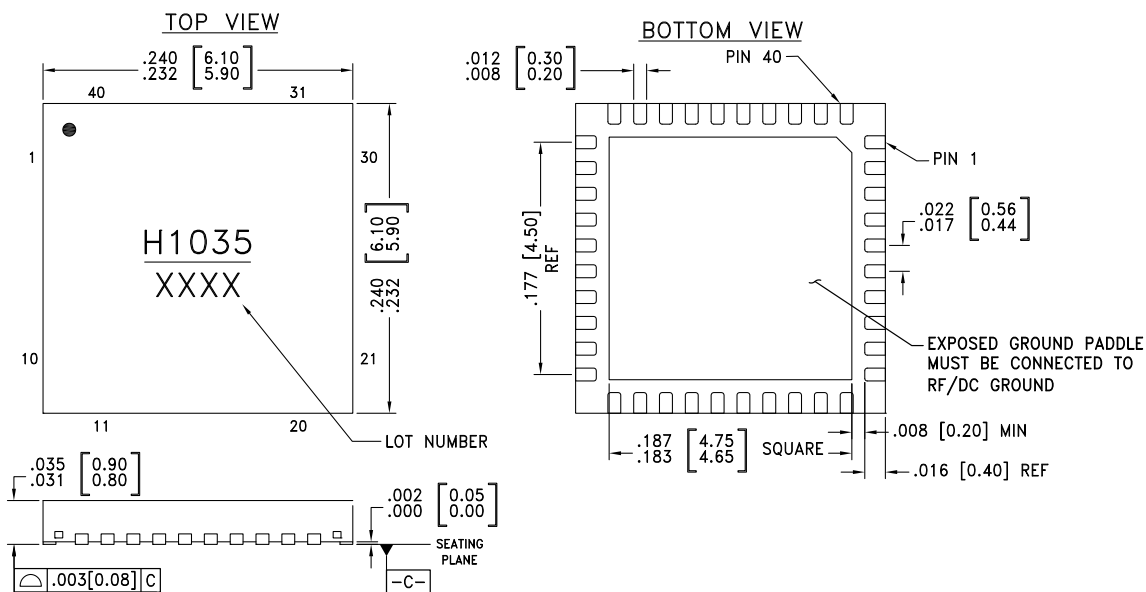


Absolute Maximum Ratings

AVDD, VPPCP, VDDLs, 3VRVDD, DVDD3V, VCC1, VCC2, VCCHF, VCCPS, VCCPD	-0.3V to +3.6V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Maximum Junction Temperature	125 °C
Thermal Resistance (R _{TH}) (junction to ground paddle)	10 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[1]
HMC1035LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H1035 XXXX

[1] 4-Digit lot number XXXX

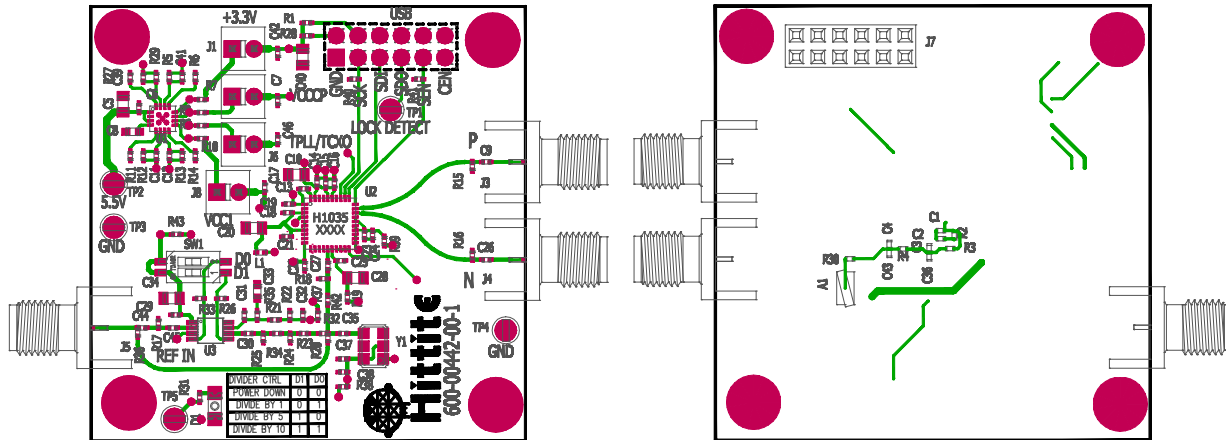
**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**

Pin Descriptions

Pin Number	Function	Description
1	AVDD	3.3 VDC Power Supply for Analog Circuitry
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 34, 37, 38	NC	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	3.3V Power Supply for Charge Pump Analog Section
4	CP	Charge Pump Output
7	VDDL5	3.3V Power Supply for the Charge Pump Digital Section
10	3VRVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	3.3V DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	3.3V VCO Analog Supply 2
27	VCC1	3.3V VCO Analog Supply 1
28	OUT_N	Negative Output Signal (Differential)
29	OUT_P	Positive Output Signal (Differential)
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD/SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	3.3 V DC Power Supply for Analog Circuitry
36	VCCPS	3.3 V DC Power Supply for Analog Prescaler
39	VCCPD	3.3 V DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V \pm 20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10G Ω meter such as Agilent 34410A, normal 10M Ω DVM will read erroneously.



Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

The HMC1035 evaluation board and associated software offers the user an easy way to quickly evaluate the performance and flexibility of the HMC1035. The evaluation board operates off a +5V supply and includes an HMC1060 LDO, which generates a low noise 3.3V source, and a precision PLL which generates a 50MHz clock, which is locked to an externally supplied 10 MHz reference.

The PLL design is an HMC1031 phase/frequency detector, passive loop filter and a low noise 50 MHz VCXO. The PLL is normally, or default upon shipping, set to lock on to a 10 MHz reference feed into "REF IN". A 5MHz input reference can be used if D1, D0 is reconfigured to "1,1", or 50 MHz if D1, D0 is reconfigured to "0,1". The "REF IN" would normally have a +/-50 ppm tolerance which falls within the VCXO pull range. Although not recommended, the HMC1035 EB can be operated without supplying an external reference, and the PLL will pull the VCXO to about 49.992 MHz, or 180 ppm low. Alternatively, an external 50 MHz reference can be feed into the HMC1035 evaluation board which requires removing C44,C35, R32 and J6, the TPLL/TCXO, and placing a 0 Ohm resistor in the R20 and R36 locations.

Evaluation PCB Schematic

To view this [Evaluation PCB Schematic](#) please visit www.hittite.com and choose HMC1035LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1035LP6G Evaluation PCB	EVAL01-HMC1035LP6G
Evaluation Kit	HMC1035LP6G Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC1035LP6G

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**



HMC1035LP6GE Input Stage

A representative schematic for the HMC1035LP6GE output stage is given in Figure 17 below. The buffer is internally DC biased with 100 ohm internal termination. For 50 ohm match, an external 100 ohm resistor to ground should be added, followed by an AC coupling capacitor (impedance < 1 ohm) then to the XREFP pin of the part.

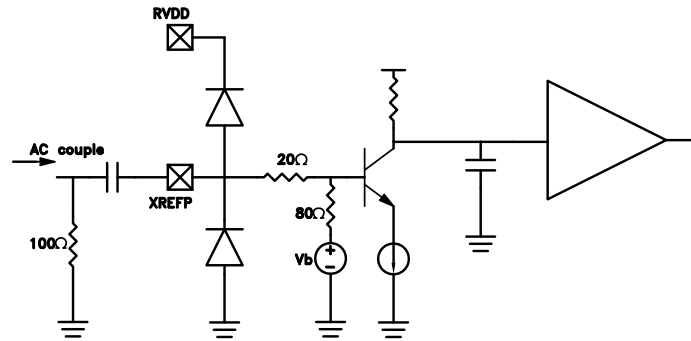


Figure 17. Input Stage

HMC1035LP6GE Output Stage

A representative schematic for the HMC1035LP6GE output stage is given in Figure 18 below. The output is derived from an emitter which can be internally biased to a current source (the default setting), or the Internal Termination switch can be opened, VCO_Reg03[4], and external termination used. The internal bias would be used when LVDS levels are required and the load would normally be a 100 differential load as shown in Figure 19. With the internal bias set, the HMC1035LP6GE output can also be used to drive 50 ohm single ended loads, see Figures 19 and 20. This would simplify LVPECL designs and reduce component cost.

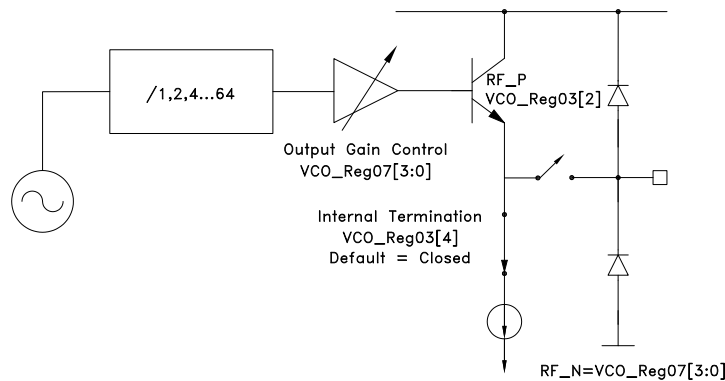


Figure 18. Output Stage

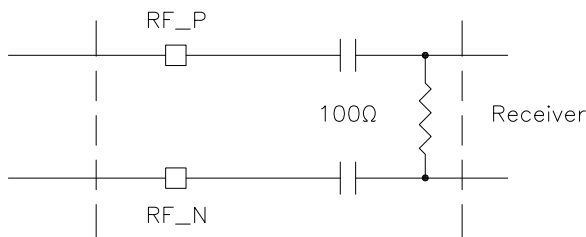


Figure 19. AC Coupling into 100 Ohm Differential Load

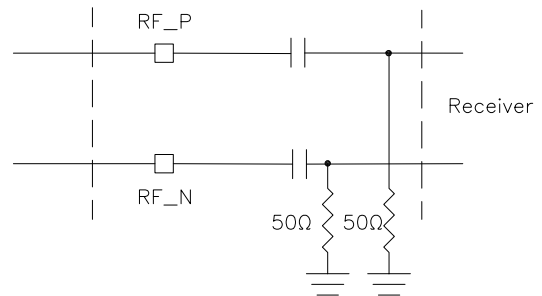


Figure 20. AC Coupling into a 50 Ohm Load

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**



Alternatively, the user can disable the internal bias, [VCO_Reg_03h\[4\]=0](#), and use a standard LVPECL termination scheme. One of the most common methods is shown in Figure 21, with the resistors being located near the receiver. AC coupling can be used after the DC biasing resistor network

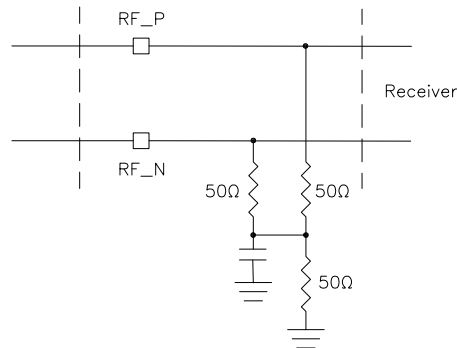


Figure 21. LVPECL Termination

The outputs can either be DC or AC coupled and the loads may be internal to the receiver or ADC etc - consult the manufacture for internal biasing and loading requirements. Selecting the AC coupling capacitors is a balance between impedance loading and rise and fall time versus signal loss and DC level drooping during the logic high and logic low levels - a low value such as 10 pF can be used for high frequency signals in the GHz range to ensure optimized rise and fall times, while a 100 nF capacitor can be used to insure low loss and minimal DC drooping when the output is a low value such as 25 MHz.

Waveform Diagrams

See Figure 22 which shows the definition for rise and fall time as well as VCM and VAMP. Figure 23 shows the Duty Cycle, which is defined as (On Time/Period) were On Time is positive going/logic high level . Measurements are made using the Internal Bias Setting.

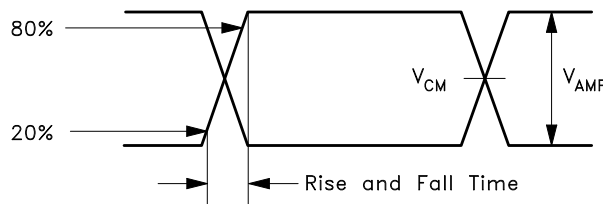


Figure 22. Rise and Fall Time, V_{CM} V_{AMP}

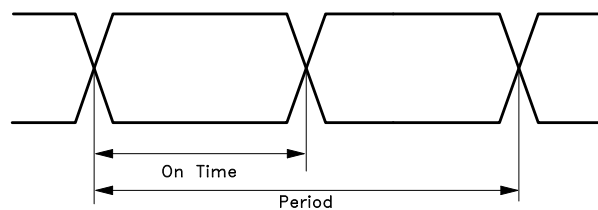


Figure 23. Duty Cycle



1.1 SERIAL PORT

1.1.1 Serial Port Modes of Operation

The HMC1035LP6GE serial port interface can operate in two different modes of operation.

- a. HMCSPi HMC Mode (HMC Legacy Mode) - Single slave per HMCSPi Bus
- b. HMCSPi Open Mode - Up to 8 slaves per HMCSPi Bus.

Both Modes support 5-bits of register address space. HMC Mode can support up to 6 bits of register address.

Register 0 has a dedicated function in each mode. Open Mode allows wider compatibility with other manufacturers SPI protocols.

Register 0 Comparison - Single vs Multi-User Modes

	Single User HMC Mode	Multi-User Open Mode
READ	Chip ID 24-bits	Chip ID 24-bits
WRITE	Soft Reset, General Strokes	Read Address [4:0] Soft reset [5] General Strokes [23:6]

1.1.2 HMCSPi Protocol Decision after Power-On Reset

On power up both types of modes are active and listening.

A decision to select the desired SPI protocol is made on the first occurrence of SEN or SCLK following a hard reset, after which the protocol is fixed and only changeable by cycling the power OFF and ON.

- a. If a rising edge on SEN is detected first HMC Mode is selected.
- b. If a rising edge on SCLK is detected first Open mode is selected.

1.1.3 Serial Port HMC Mode - Single PLL

HMC Mode (Legacy Mode) serial port operation can only address and talk to a single PLL, and is compatible with most Hittite PLLs and PLLs with Integrated VCOs.

The HMC Mode protocol, shown in [Figure 24](#) and, [Figure 25](#) is designed for a 4 wire interface with a fixed protocol featuring

- a. 1 Read/Write bit
- b. 6 Address bits
- c. 24 data bits
- d. 3 wire for Write only, 4 wire for Read/Write capability



1.1.3.1 HMC Mode - Serial Port WRITE Operation

AVDD = DVDD = 3.3V ±5%, AGND = DGND = 0V

SPI HMC Mode - Write Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			ns
t_2	SDI to SCLK setup time	3			ns
t_3	SCLK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
t_5	SCK to SEN fall	10			ns
	Max Serial port Clock Speed		50		MHz

A typical HMC Mode WRITE cycle is shown in Figure 24.

- The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.
- The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI low indicates a Write cycle (/WR).
- Host places the six address bits on the next six falling edges of SCK, MSB first.
- Slave shifts the address bits in the next six rising edges of SCK (2-7).
- Host places the 24 data bits on the next 24 falling edges of SCK, MSB first.
- Slave shifts the data bits on the next 24 rising edges of SCK (8-31).
- The data is registered into the chip on the 32nd rising edge of SCK.
- SEN is cleared after a minimum delay of t_5 . This completes the write cycle.

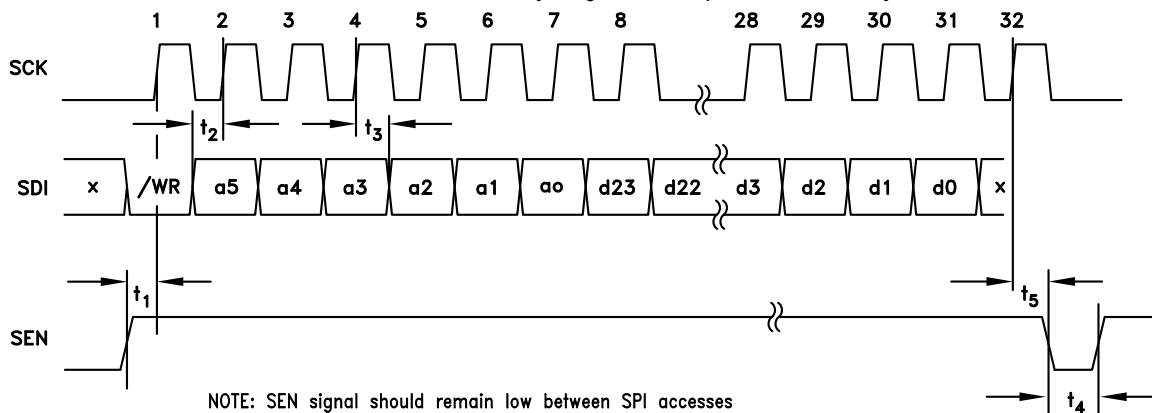


Figure 24. HMC Mode - Serial Port Timing Diagram Write

1.1.3.2 HMC Mode - Serial Port READ Operation

A typical HMC Mode READ cycle is shown in Figure 25.

- The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCLK. Note: The Lock Detect (LD) function is usually multiplexed onto the LD_SDO pin. It is suggested that LD only be considered valid when SEN is low. In fact LD will not toggle until the first active data bit toggles on LD_SDO, and will be restored immediately after the trailing edge of the LSB of serial data out as shown in Figure 25.
- The slave (HMC1035LP6GE) reads SDI on the 1st rising edge of SCLK after SEN. SDI high initiates the READ cycle (RD)



- c. Host places the six address bits on the next six falling edges of SCLK, MSB first.
- d. Slave registers the address bits on the next six rising edges of SCLK (2-7).
- e. Slave switches from Lock Detect and places the requested 24 data bits on SD_LDO on the next 24 rising edges of SCK (8-31), MSB first .
- f. Host registers the data bits on the next 24 falling edges of SCK (8-31).
- g. Slave restores Lock Detect on the 32nd rising edge of SCK.
- h. De-assertion of SEN completes the cycle

SPI HMC Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			ns
t_2	SDI to SCLK setup time	3			ns
t_3	SCLK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
t_5	SCLK to SDO delay			8.2ns+0.2ns/pF	ns
t_6	Recovery Time	10			ns

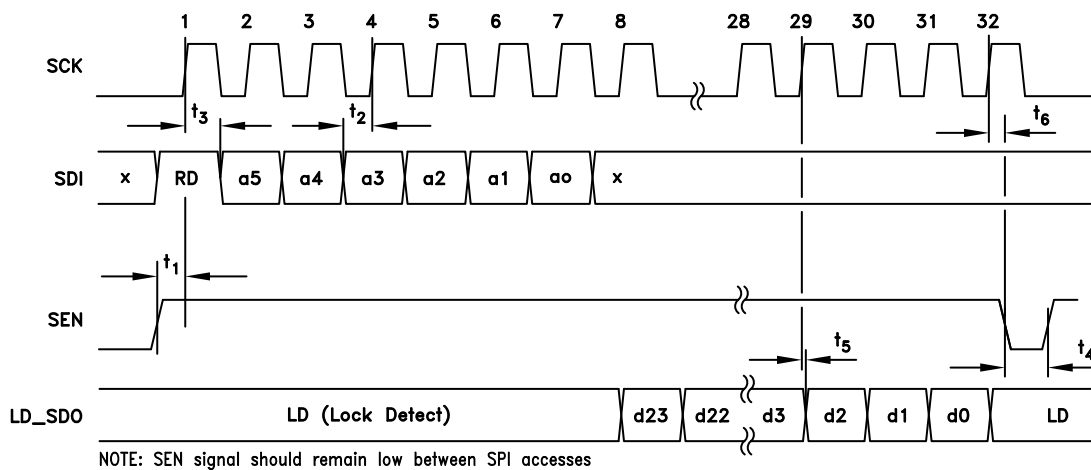


Figure 25. HMC Mode - Serial Port Timing Diagram - READ

1.1.4 Serial Port Open Mode

The Serial Port Open Mode, shown in [Figure 26](#) and [Figure 27](#), features:

- a. Compatibility with general serial port protocols that use shift and strobe approach to communication
- b. Compatible with Hittite PLL with Integrated VCO solutions, useful to address multiple chips of various types from a single serial port bus.

The Open Mode protocol has the following general features:

- a. 3-bit chip address , can address up to 8 devices connected to the serial bus
- b. Wide compatibility with multiple protocols from multiple vendors
- c. Simultaneous Write/Read during the SPI cycle

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**



- d. 5-bit address space
- e. 3 wire for Write Only capability, 4 wire for Read/Write capability

Hittite PLLs with integrated VCOs support Open Mode. Some legacy PLL and microwave PLLs with integrated VCOs only support HMC Mode. Consult the relevant data sheets for details.

Typical serial port operation can be run with SCLK at speeds up to 50 MHz.

1.1.4.1 Open Mode - Serial Port WRITE Operation

AVDD = DVDD = 3.V ±5%, AGND = DGND = 0V

SPI Open Mode - WRITE Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t ₁	SDI setup time to SCLK Rising Edge	3			ns
t ₂	SCLK Rising Edge to SDI hold time	3			ns
t ₃	SEN low duration	10			ns
t ₄	SEN high duration	10			ns
t ₅	SCLK 32 Rising Edge to SEN Rising Edge	10			ns
t ₆	Recovery Time	20			ns
	Max Serial port Clock Speed		50		MHz

A typical WRITE cycle is shown in Figure 26.

- a. The Master (host) places 24-bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCLK.
- b. the slave (HMC1035LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK
- c. Master places 5-bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCLK (25-29)
- d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).
- e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32). Hittite reserves chip address a2:a0 = 000 for all RF PLL with Integrated VCOs.
- f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).
- g. Master asserts SEN after the 32nd rising edge of SCLK.
- h. Slave registers the SDI data on the rising edge of SEN.

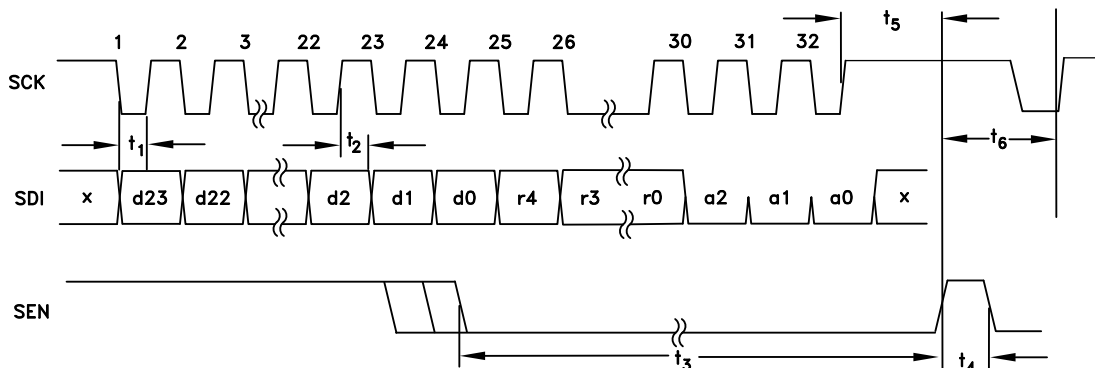


Figure 26. Open Mode - Serial Port Timing Diagram - WRITE



1.1.4.2 Open Mode - Serial Port READ Operation

A typical READ cycle is shown in Figure 27.

In general, in Open Mode the LD_SDO line is always active during the WRITE cycle. During any Open Mode SPI cycle LD_SDO will contain the data from the current address written in [Reg 00h\[4:0\]](#). If [Reg 00h\[4:0\]](#) is not changed then the same data will always be present on LD_SDO when an Open Mode cycle is in progress. If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to [Reg 00h\[4:0\]](#), then in the next SPI cycle the desired data will be available on LD_SDO.

An example of the Open Mode two cycle procedure to read from any random address is as follows:

- a. The Master (host), on the first 24 falling edges of SCLK places 24-bit data, d23:d0, MSB first, on SDI as shown in Figure 27. d23:d5 should be set to zero. d4:d0 = address of the register to be READ on the next cycle.
- b. the slave (HMC1035LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK
- c. Master places 5-bit register address , r4:r0, (the READ ADDRESS register), MSB first, on the next 5 falling edges of SCLK (25-29). r4:r0=00000.
- d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).
- e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32)..Chip address is always 000 for RF PLL with Integrated VCOs.
- f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).
- g. Master asserts SEN after the 32nd rising edge of SCLK.
- h. Slave registers the SDI data on the rising edge of SEN.
- i. Master clears SEN to complete the address transfer of the two part READ cycle.
- j. If one does not wish to write data to the chip at the same time as we do the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.
- k. Master places the same SDI data as the previous cycle on the next 32 falling edges of SCLK.
- l. Slave (HMC1035LP6GE) shifts the SDI data on the next 32 rising edges of SCLK.
- m. Slave places the desired read data (ie. data from the address specified in [Reg 00h\[7:3\]](#) of the first cycle) on LD_SDO which automatically switches to SDO mode from LD mode, disabling the LD output.
- n. Master asserts SEN after the 32nd rising edge of SCK to complete the cycle and revert back to Lock Detect on LD_SDO.

SPI Open Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t ₁	SDI setup time to SCLK Rising Edge	3			ns
t ₂	SCLK Rising Edge to SDI hold time	3			ns
t ₃	SEN low duration	10			ns
t ₄	SEN high duration	10			ns
t ₅	SCLK Rising Edge to SDO time			8.2ns+0.2ns/pF	ns
t ₆	Recovery Time	10			ns
t ₇	SCK 32 Rising Edge to SEN Rising Edge	10			ns



1.1.4.3 HMCSPi Open Mode READ Operation - 2 Cycles

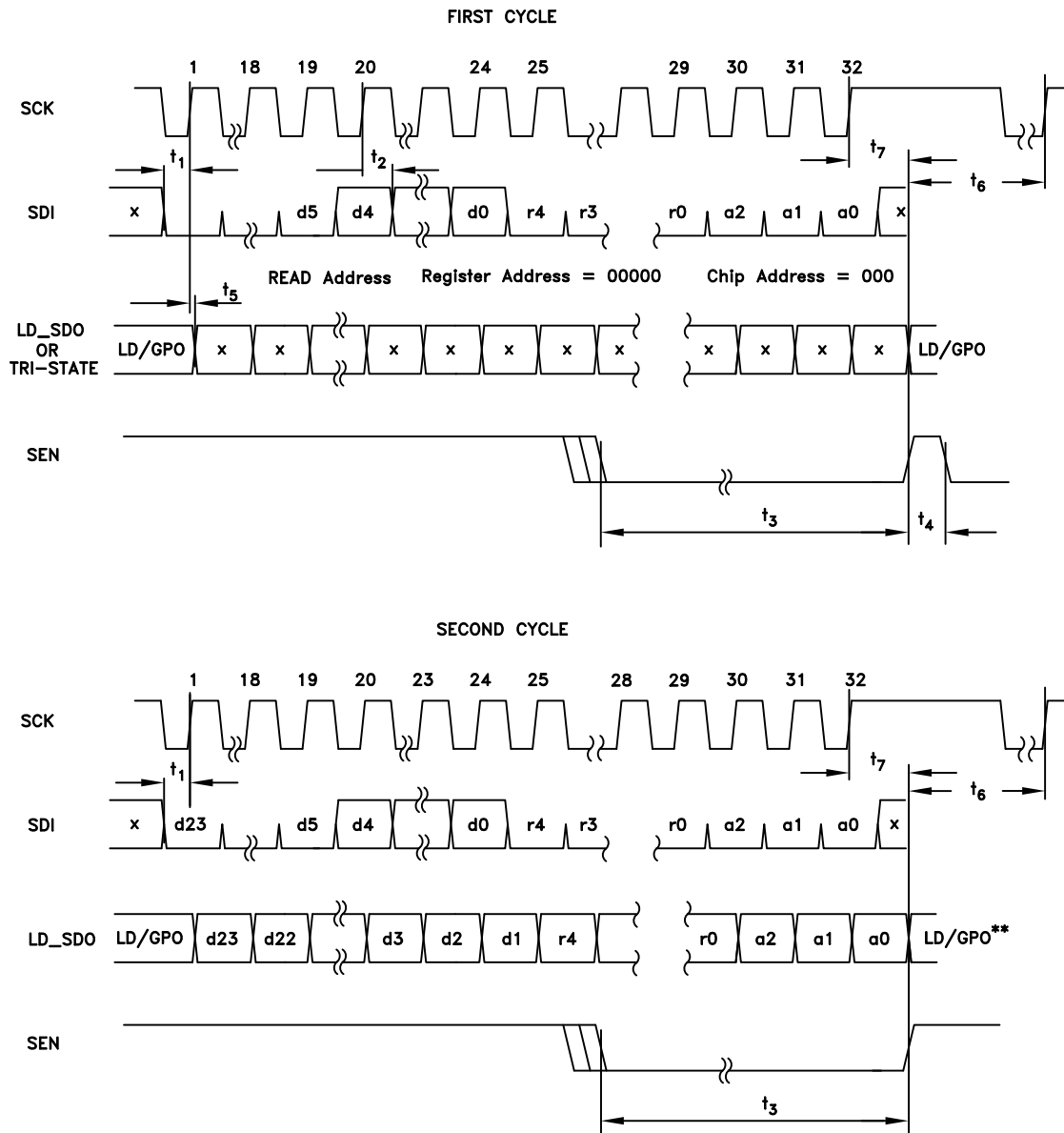


Figure 27. Serial Port Timing Diagram - READ

For more information on using the GPO pin while in SPI Open Mode please see section [1.15](#).

**HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR
25 - 2500 MHz**

1.2 Configuration at Start-Up

To configure the PLL after power up, follow the instructions below:

1. Configure the reference divider (write to [Reg 02h](#)), if required.
2. Configure the delta-sigma modulator (write to [Reg 06h](#)).
 - Configuration involves selecting the mode of the delta-sigma modulator (Mode A or Mode B), selection of the delta-sigma modulator seed value, and configuration of the delta-sigma modulator clock scheme. It is recommended to use the values found in the Hittite PLL evaluation board control software register files.
3. Configure the charge pump current and charge pump offset current (write to [Reg 09h](#))
4. Configure the VCO Subsystem (write to [Reg 05h](#), for more information see section [1.3.1](#), and "[VCO Subsystem Register Map](#)". Detailed writes to the VCO subsystem via PLL [Reg 05h](#) at start-up are available in the Register Setting Files found in the Hittite PLL Evaluation Software received with a product evaluation kit or downloaded from www.hittite.com.
5. Program the frequency of operation
 - Program the integer part (write to [Reg 03h](#))
 - Program the fractional part (write to [Reg 04h](#))
6. Configure the VCO output divider, if needed in the VCO subsystem via PLL [Reg 05h](#).

Once the HMC1035LP6GE is configured after startup, in most cases the user only needs to change frequencies by writing to [Reg 03h](#) integer register, [Reg 04h](#) fractional register, and [Reg 05h](#) to change the VCO output divider or doubler setting if needed, and possibly adjust the charge pump settings by writing to [Reg 09h](#)

For detailed and most up-to-date start-up configuration please refer to the appropriate Register Setting Files found in the Hittite PLL Evaluation Software received with a product evaluation kit or downloaded from www.hittite.com.

1.3 VCO Serial Port Interface (SPI)

The HMC1035LP6GE communicates with the internal VCO subsystem via an internal 16 bit VCO Serial Port, (e.g. see [Figure 25](#)). The internal serial port is used to control the step tuned VCO and other VCO subsystem functions, such as RF output divider / doubler control and RF buffer enable.

Note that the internal VCO subsystem SPI (VSPI) runs at the rate of the AutoCal FSM clock, T_{FSM} , where the FSM clock frequency cannot be greater than 50 MHz. The VSPI clock rate is set by [Reg 0Ah\[14:13\]](#) with a default setting = 1, or XREFP divided by 4.

Writes to the VCO's control registers are handled indirectly, via writes to [Reg 05h](#) of the PLL. A write to PLL [Reg 05h](#) causes the PLL subsystem to forward the packet, MSB first, across its internal serial link to the VCO subsystem, where it is interpreted.

The VCO serial port has the capability to communicate with multiple subsystems inside the IC. For this reason each subsystem has a subsystem ID, [Reg 05h\[2:0\]](#).

Each subsystem has multiple registers to control the functions internal to the subsystem, which may be different from one subsystem to the next. Hence each subsystem has internal register addresses bits ("[Reg 05h](#)"6:3))

Finally the data required to configure each register within the VCO subsystem is contained in [Reg 05h\[15:7\]](#).

HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR 25 - 2500 MHz



1.3.1 VSPI Use of Reg05h

The packet data written into, [Reg 05h](#) is sub-parsed by logic at the VCO subsystem into the following 3 fields:

1. [2:0] - 3 bits - VCO_ID, target subsystem address = 000b.
2. [6:3] - 4 bits - VCO_REGADDR, the internal register address inside the VCO subsystem.
3. [15:7] - 9- bits- VCO_DATA, data field to write into the VCO register.

For example, to write 0_0011_1110 into register 2 of the VCO subsystem (VCO_ID = '000'b), and set the VCO output divider to divide by 62, the following needs to be written to [Reg 05h](#) = '0_0011_1110, 0010, 000' b.

During AutoCal, the AutoCal controller only updates the data field of [Reg 05h](#). The VCO subsystem register address ([Reg 05h](#)[6:3]) must be set to 0000 for the AutoCal data to be sent to the correct address.

VCO subsystem ID and register address are not modified by the AutoCal state machine. Hence, if a manual access is done to a VCO Subsystem register the user must reset the register address to zero before a change of frequency which will re-run AutoCal.

Since every write to [Reg 05h](#) will result in a transfer of data to the VCO subsystem, if the VCO subsystem needs to be reset manually, it is important to make sure that the VCO switch settings are not changed. Hence the switch settings in [Reg 10h](#)[7:0] need to be read first, and then rewritten to [Reg 05h](#)[15:8].

In summary, first read "[Reg 10h](#)", then write to "[Reg 05h](#)" as follows:

Reg 10h [7:0]	= vv x yyyyy
Reg 05h	= vv x yyyyy 0 0000 iii
Reg 05h [2:0]	= iii, subsystem ID, 3 bits (000)
Reg 05h [6:3]	= 0000, subsystem register address
Reg 05h [7]	= 0 , calibration tune voltage off
Reg 05h [12:8]	= yyyyy, VCO caps
Reg 05h [13]	= x, don't care
Reg 05h [15:14]	= vv, VCO Select

1.0 PLL Register Map

1.1 Reg 00h ID Register (Read Only)

Bit	Type	Name	Width	Default	Description
[23:0]	RO	chip_ID	24	A7975	HMC1035LP6GE chip ID

1.2 Reg 00h Open Mode Read Address/RST Strobe Register (Write Only)

Bit	Type	Name	Width	Default	Description
[4:0]	WO	Read Address	5	-	(WRITE ONLY) Read Address for next cycle - Open Mode Only
[5]	WO	Soft Reset	1	-	Soft Reset - both SPI modes reset (set to 0 for proper operation)
[23:6]	WO	Not Defined	18	-	Not Defined (set to 0 for proper operation)



1.3 Reg 01h RST Register

(Default 000002h)

Bit	Type	Name	Width	Default	Description
[0]	R/W	Reserved	1	0	Reserved
[1]	R/W	Reserved	1	1	Reserved
[2]	R/W	Reserved	1	0	Reserved
[3]	R/W	Reserved	1	0	Reserved
[4]	R/W	Reserved	1	0	Reserved
[5]	R/W	Reserved	1	0	Reserved
[6]	R/W	Reserved	1	0	Reserved
[7]	R/W	Reserved	1	0	Reserved
[8]	R/W	Reserved	1	0	Reserved
[9]	R/W	Reserved	1	0	Reserved

1.4 Reg 02h REFDIV Register

(Default 000001h)

Bit	Type	Name	Width	Default	Description
[13:0]	R/W	rdiv	14	1	Reference Divider 'R' Value ⁴ Divider use also requires refBufEn Reg08[3]=1 and Divider min 1d max 16383d

1.5 Reg 03h Frequency Register - Integer Part

(Default 000019h)

Bit	Type	Name	Width	Default	Description
[18:0]	R/W	intg	19	25d	VCO Divider Integer part, used in all modes Fractional Mode min 20d max $2^{19} - 4 = 7FFFCh = 524,284d$ Integer Mode min 16d max $2^{19} - 1 = 7FFFFh = 524,287d$

1.6 Reg 04h Frequency Register - Fractional Part

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[23:0]	R/W	frac	24	0	VCO Divider Fractional part (24-bit unsigned) see Fractional Frequency Tuning Used in Fractional Mode only ($N_{frac} = \text{Reg 04h} / 2^{24}$) min 0d max $2^{24} - 1$



1.7 Reg 05h VCO SPI Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	VCO Subsystem_ID,	3	0	Internal VCO Subsystem ID
[6:3]	R/W	VCO Subsystem register address	4	0	For interfacing with the VCO please see section 1.3.1 .
[15:7]	R/W	VCO Subsystem data	9	0	Data

Note: [Reg 05h](#) is a special register used for indirect addressing of the VCO subsystem. Writes to [Reg 05h](#) are automatically forwarded to the VCO subsystem by the VCO SPI state machine controller.

Reg05h is a Read-Write register. However, Reg05h only holds the contents of the last transfer to the VCO subsystem. Hence it is not possible to read the full contents of the VCO subsystem. Only the content of the last transfer to the VCO subsystem can be read. Please take note special considerations for AutoCal related to [Reg 05h](#)

1.8 Reg 06h SD CFG Register

(Default 200B4Ah)

Bit	Type	Name	Width	Default	Description
[1:0]	R/W	seed	2	2	Selects the Seed in Fractional Mode 00: 0 seed 01: lsb seed 02: B29D08h seed 03: 50F1CDh seed Note: Writes to this register are stored in the HMC1035LP6GE and are only loaded into the modulator when a frequency change is executed and if AutoSeed $Reg06h[8] = 1$
[3:2]	R/W	Reserved	2	2	Reserved
[6:4]	R/W	Reserved	3	4	Reserved
[7]	R/W	frac_bypass	1	0	0: Use Modulator, Required for Fractional Mode, 1: Bypass Modulator, Required for Integer Mode Note: In bypass fractional modulator output is ignored, but fractional modulator continues to be clocked if $frac_rstb = 1$. Can be used to test the isolation of the digital fractional modulator from the VCO output in integer mode
[8]	R/W	Reserved	1	1	Reserved
[9]	R/W	Reserved	1	1	Reserved
[10]	R/W	Reserved	1	0	Program 1
[11]	R/W	SD Enable	1	1	0: disable frac core, use for Integer Mode or Integer Mode with CSP 1: Enable Frac Core, required for Fractional Mode, or Integer isolation testing This register controls whether AutoCal starts on an Integer or a Fractional write
[12]	R/W	Reserved	1	0	Reserved
[13]	R/W	Reserved	1	0	Reserved
[15:14]	R/W	Reserved	2	0	Reserved
[17:16]	R/W	Reserved	2	0	Reserved
[18]	R/W	Reserved	1	0	Reserved
[20:19]	R/W	Reserved	2	0	Reserved
[21]	R/W	Reserved	1	1	Program 0
[22]	R/W	Reserved	1	0	Reserved



1.9 Lock Detect:

HMC1035LP6GE features a robust digital lock detect function that provides faster and more accurate lock detect information compared to conventional analog lock detect schemes, and offers serial port monitoring of lock detect for visibility into device status from the host controller.

Lock Detect Enable Reg 07h[3]=1 is a global enable for all lock detect functions. The Lock Detect circuit effectively measures the difference between the arrival of the reference and the divided VCO signals at the Phase Detector. The arrival time difference must consistently be less than the Lock Detect window length, to declare lock. Either signal may arrive first, only the difference in arrival times is considered.

wincnt_max in Reg 07h[2:0] defines the number of consecutive counts of the divided VCO that must land inside the lock detect window to declare lock.

1.9.1 Analog or Digital Lock Detect

Analog Lock Detect

The lock detect window may be generated by either an analog one shot circuit or a digital one shot based upon an internal timer. Clearing [Reg 07h\[6\]=0](#) will result in a fixed, analog, nominal 10 ns window, as shown in Figure 28 below. The analog window cannot be used if the PD rate is above 50 MHz, or if the charge pump offset is too large. If charge pump offset or PD frequency are changed significantly then the lock detect window may need to be adjusted.

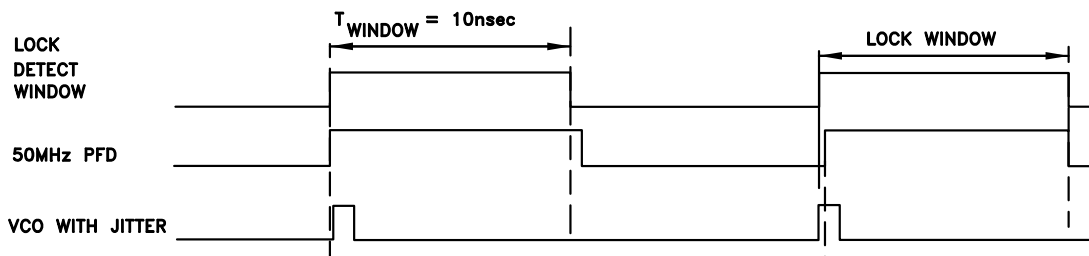


Figure 28. Lock Detect

1.9.2 Digital Lock Detect:

Setting [Reg 07h\[6\]=1](#) will result in a variable length lock detect window based upon an internal digital timer. The timer period is set by the number of cycles of the internal LD clock as programmed by [Reg 07h\[9:7\]](#). The LD clock frequency is adjustable by [Reg 07h\[11:10\]](#). The LD clock signal (Ring Osc) can be viewed via the GPO test pins.

Optimal spectral performance in fractional mode requires CP current and CP offset current configuration discussed in detail in section [1.11 Charge Pump Current Selection](#). These settings in [Reg 09h](#) impact the required LD window size in fractional mode of operation. To function, the required lock detect window size is provided by [\(EQ 1\)](#).

HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR 25 - 2500 MHz



$$\text{LD Window (seconds)} = \frac{\left(\frac{I_{CP\text{ Offset}} (A)}{F_{PD} (Hz) \times I_{CP} (A)} + 2.66 \times 10^{-9} (\text{sec}) + \frac{1}{F_{PD} (Hz)} \right)}{2} \text{ in Fractional Mode}$$

$$\text{LD Window (seconds)} = \frac{1}{2 \times F_{PD}} \text{ in Integer Mode} \quad (\text{EQ 1})$$

where:

F_{PD} : is the comparison frequency of the Phase Detector

$I_{CP\text{ Offset}}$: is the Charge Pump Offset Current [Reg 09h\[20:14\]](#)

I_{CP} : is the full scale current setting of the switching charge pump [Reg 09h\[6:0\]](#), or [Reg 09h\[13:7\]](#)

If the result provided by [\(EQ 1\)](#) is equal to 10 ns Analog LD can be used ([Reg 07h\[6\] = 0](#)). Otherwise Digital LD is necessary [Reg 07h\[6\] = 1](#).

[Table 17](#) provides the required [Reg 07h](#) settings to appropriately program the Digital LD window size. From [Table 17](#), simply select the closest value in the “Digital LD Window Size” columns to the one calculated in [\(EQ 1\)](#) and program [Reg 07h\[11:10\]](#) and [Reg 07h\[9:7\]](#) accordingly.

Table 17. Typical Digital Lock Detect Window

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Size Nominal Value (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	7.1	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Reg07[9:7]	000	001	010	011	100	101	110	111

1.9.2.1 Digital Window Configuration Example

Assuming, fractional mode, with a 50 MHz PD and

- Charge Pump gain of 2 mA ([Reg 09h\[13:7\] = 64h](#), [Reg 09h\[6:0\] = 64h](#)),
- Up Offset ([Reg 09h\[22:21\] = '01'b](#))
- and Offset current magnitude of +400 μA ([Reg 09h\[20:14\] = 50h](#))

Applying [\(EQ 1\)](#), the required LD window size is:

$$\text{LD Window (seconds)} = \frac{\left(\frac{0.4 \times 10^{-3} (A)}{50 \times 10^6 (Hz) \times 2 \times 10^{-3} (A)} + 2.66 \times 10^{-9} (\text{sec}) + \frac{1}{50 \times 10^6 (Hz)} \right)}{2} = 13.33 \text{ nsec} \quad (\text{EQ 2})$$

Locating the [Table 17](#) value that is closest to the [\(EQ 2\)](#) result, in this case $13.3 \approx 13.33$. To set the Digital LD window size, simply program [Reg 07h\[11:10\] = '10'b](#) and [Reg 07h\[9:7\] = '010'b](#) according to [Table 17](#).

There is always a good solution for the lock detect window for a given operating point. The user should understand however that one solution does not fit all operating points. As observed from [\(EQ 1\)](#), if charge pump offset or PD frequency are changed significantly then the lock detect window may need to be adjusted.