



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FEATURES

Attenuation range: 0.5 dB LSB steps to 31.5 dB

Low insertion loss

1.1 dB at 1 GHz

1.3 dB at 2 GHz

Typical step error: less than ± 0.1 dB

Excellent attenuation accuracy

Safe state transitions

High linearity

Input 0.1 dB compression (P0.1dB): 30 dBm typical

Input third-order intercept (IP3): 55 dBm typical

RF settling time (0.05 dB final RF output): 250 ns

Low phase shift error: 6° at 1 GHz

Single supply operation: 3.3 V to 5 V

ESD rating: Class 2 (2 kV HBM)

24-lead, 4 mm \times 4 mm LFCSP package: 16 mm²

Pin compatible to the [HMC624A](#)

APPLICATIONS

Cellular infrastructure

Microwave radios and very small aperture terminals (VSATs)

Test equipment and sensors

IF and RF designs

GENERAL DESCRIPTION

The [HMC1122](#) is a 6-bit digital attenuator operating from 0.1 GHz to 6 GHz with a 31.5 dB attenuation control range in 0.5 dB steps.

The [HMC1122](#) is implemented in a silicon process, offering very fast settling time, low power consumption, and high ESD robustness. The device features safe state transitions and optimized for excellent step accuracy and high linearity over frequency and temperature range. The RF input and output are internally matched to 50 Ω and do not require any external matching components. The design is bidirectional; therefore, the RF input and output are interchangeable.

FUNCTIONAL BLOCK DIAGRAM

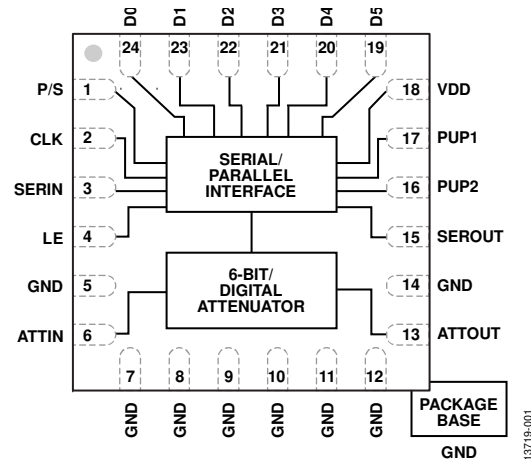


Figure 1.

The [HMC1122](#) operates on a single supply ranging from 3.3 V to 5 V with no performance change due to an on-chip regulator.

The device incorporates a driver that provides both serial and parallel control of the attenuator. The device also features a user-selectable power-up state and a serial output port for cascading other serial controlled components.

The [HMC1122](#) comes in a RoHS compliant, compact, 4 mm \times 4 mm LFCSP package, and is pin compatible to the [HMC624A](#).

A fully populated evaluation board is available.

HMC1122* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC1122 Evaluation Board

DOCUMENTATION

Data Sheet

- HMC1122: 0.1 GHz to 6.0 GHz, 0.5 dB LSB, 6-Bit, Silicon Digital Attenuator Data Sheet

TOOLS AND SIMULATIONS

- HMC1122LP4ME IBIS Model
- HMC1122 S-Parameters

DESIGN RESOURCES

- HMC1122 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC1122 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

| | | | |
|--|---|--|----|
| Features | 1 | Input Power Compression and Third-Order Intercept..... | 9 |
| Applications..... | 1 | Theory of Operation | 10 |
| Functional Block Diagram | 1 | Power Supply..... | 10 |
| General Description | 1 | RF Input and Output | 10 |
| Revision History | 2 | Serial or Parallel Mode Selection | 10 |
| Specifications..... | 3 | Serial Mode Interface..... | 10 |
| Absolute Maximum Ratings..... | 5 | Parallel Mode Interface..... | 11 |
| ESD Caution..... | 5 | Power-Up Interface | 11 |
| Pin Configuration and Function Descriptions..... | 6 | Applications Information | 12 |
| Interface Schematics..... | 6 | Evaluation Printed Circuit Board..... | 12 |
| Typical Performance Characteristics | 7 | Evaluation Board Schematic and Artwork | 13 |
| Insertion Loss, Return Loss, State Error, Step Error, and Relative Phase..... | 7 | Outline Dimensions | 15 |
| | | Ordering Guide | 15 |

REVISION HISTORY

4/16—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 3.3 \text{ V to } 5 \text{ V}$, $T_A = 25^\circ\text{C}$, 50Ω system, unless otherwise noted.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------------|-------------------------|---|----------------------------------|-------------|----------------------------------|---------|
| FREQUENCY RANGE | | | 0.1 | | 6.0 | GHz |
| INSERTION LOSS | | At 0.2 GHz to 1.0 GHz | | 1.1 | 1.8 | dB |
| | | At 1.0 GHz to 2.0 GHz | | 1.3 | 2.0 | dB |
| | | At 2.0 GHz to 4.0 GHz | | 1.7 | 2.4 | dB |
| | | At 4.0 GHz to 6.0 GHz | | 2.0 | 2.8 | dB |
| ATTENUATION | | At 0.2 GHz to 6 GHz | | | | |
| Range | | Between minimum and maximum attenuation states | | 31.5 | | dB |
| Step Size | | Between any successive attenuation states | | 0.5 | | dB |
| Step Error | | Between any successive attenuation states | | < ± 0.1 | | dB |
| Accuracy | | All attenuation states; referenced to insertion loss state | -(0.1 + 4% of attenuation state) | | +(0.1 + 4% of attenuation state) | dB |
| Overshoot | | Between all attenuation states | | <0.1 | | dB |
| RETURN LOSS (ATTIN and ATTOUT) | | At 1.0 GHz, minimum attenuation (worst case) | | 24 | | dB |
| | | At 2.0 GHz, minimum attenuation (worst case) | | 22 | | dB |
| | | At 4.0 GHz, minimum attenuation (worst case) | | 22 | | dB |
| | | At 6.0 GHz, maximum attenuation (worst case) | | 21 | | dB |
| RELATIVE PHASE | | Between minimum and maximum attenuation states | | | | |
| | | At 1.0 GHz | | 6 | | Degrees |
| | | At 2.0 GHz | | 18 | | Degrees |
| | | At 4.0 GHz | | 38 | | Degrees |
| | | At 6.0 GHz | | 58 | | Degrees |
| SWITCHING CHARACTERISTICS | | Between all attenuation states | | | | |
| Rise and Fall Time | t_{RISE} , t_{FALL} | 10% to 90% of RF output | | 60 | | ns |
| On and Off Time | t_{ON} , t_{OFF} | 50% V_{CTL} to 90% of RF output | | 150 | | ns |
| 0.1 dB Settling Time | | 50% V_{CTL} to 0.1 dB of final RF output | | 200 | | ns |
| 0.05 dB Settling Time | | 50% V_{CTL} to 0.05 dB of final RF output | | 250 | | ns |
| INPUT LINEARITY | | All attenuation states, 0.2 GHz to 6 GHz | | | | |
| Input 0.1 dB Compression | P0.1dB | | | 30 | | dBm |
| Input Third-Order Intercept | IP3 | Two-tone input power = 15 dBm each tone, $\Delta f = 1 \text{ MHz}$ | | 55 | | dBm |
| SUPPLY CURRENT | I_{DD} | $V_{DD} = 3.3 \text{ V}$ | | 0.3 | | mA |
| | | $V_{DD} = 5.0 \text{ V}$ | | 0.4 | | mA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|----------------------------------|----------------------|---|-----|------------------|----------|------------------|
| DIGITAL CONTROL INPUTS | | | | | | |
| Input Voltage | | P/S, CLK, SERIN, LE, D0 to D5, PUP1, and PUP2 pins | | | | |
| Low | V_{INL} | $V_{DD} = 3.3\text{ V}$ | 0 | | 0.5 | V |
| | | $V_{DD} = 5.0\text{ V}$ | 0 | | 0.8 | V |
| High | V_{INH} | $V_{DD} = 3.3\text{ V}$ | 2.0 | | 3.3 | V |
| | | $V_{DD} = 5.0\text{ V}$ | 3.5 | | 5.0 | V |
| Low and High Input Current | I_{INL}, I_{INH} | $V_{DD} = 3.3\text{ V to }5\text{ V}$ | | <1 | | μA |
| DIGITAL CONTROL OUTPUT | | | | | | |
| Output Voltage | | SEROUT | | | | |
| Low | V_{OUTL} | | | ± 0.1 | | V |
| High | V_{OUTH} | | | $V_{DD} \pm 0.1$ | | V |
| Low and High Output Current | I_{OUTL}, I_{OUTH} | | | | 1 | mA |
| RECOMMENDED OPERATING CONDITIONS | | | | | | |
| Supply Voltage | V_{DD} | | 3.0 | | 5.4 | V |
| Digital Control Voltage Range | V_{CTL} | | 0 | | V_{DD} | V |
| RF Input Power | P_{IN} | All attenuation states, $T_{CASE} = 85^\circ\text{C}$ | | | 24 | dBm |
| Case Temperature | T_{CASE} | | -40 | | +85 | $^\circ\text{C}$ |

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|--|----------------------------|
| RF Input Power, P_{IN} ($T_{CASE} = 85^{\circ}C$) | 25 dBm |
| Supply Voltage | -0.3 V to +5.5 V |
| Digital Control Input Voltage | -0.3 V to $V_{DD} + 0.5$ V |
| Continuous Power Dissipation, P_{DISS} | 0.31 W |
| Junction to Case Thermal Resistance, θ_{JC} (at Maximum Power Dissipation) | 156°C/W |
| Temperature | |
| Junction, T_J | 135°C |
| Storage | -65°C to +150°C |
| Reflow | 260°C (MSL3 Rating) |
| ESD Sensitivity | |
| Human Body Model (HBM) | 2 kV (Class 2) |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

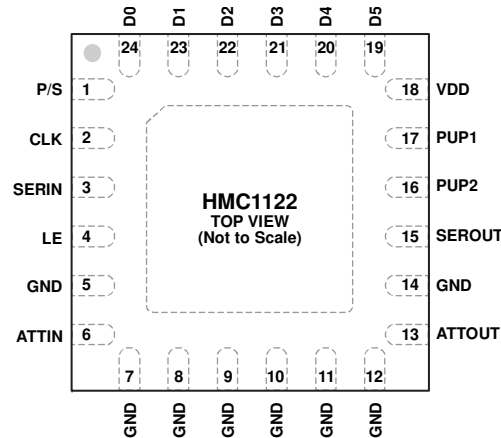
Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

13719-002

Figure 2. Pin Configuration (Top View)

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|----------------|------------|--|
| 1 | P/S | Parallel/Serial Mode Select. For parallel mode operation, set this pin to low. For serial mode operation, set this pin to high. |
| 2 | CLK | Serial Interface Clock Input. |
| 3 | SERIN | Serial Interface Data Input. |
| 4 | LE | Latch Enable Input. |
| 5, 7 to 12, 14 | GND | Ground. These pins must be connected to ground. |
| 6 | ATTIN | Attenuator RF Input. This pin can also be used as an output because the design is bidirectional. ATTIN is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required. |
| 13 | ATTOUT | Attenuator RF Output. This pin can also be used as an input because the design is bidirectional. ATTOUT is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required. |
| 15 | SEROUT | Serial Interface Data Output. Serial input data is delayed by six clock cycles. |
| 16, 17 | PUP2, PUP1 | Power-Up State Selection Bits. These pins set the attenuation value at power-up (see Table 7). There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (V_{IH} or V_{IL}) and not be left floating. |
| 18 | VDD | Power Supply. |
| 19 to 24 | D5 to D0 | Parallel Control Voltage Inputs. These pins select the required attenuation (see Table 5). There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (V_{IH} or V_{IL}) and not be left floating. |
| | EPAD | Exposed Pad. The exposed pad must be connected to ground for proper operation. |

INTERFACE SCHEMATICS

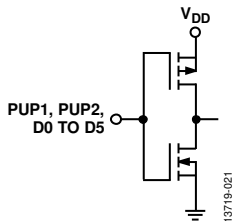


Figure 3. PUP1, PUP2, and D0 to D5 Interface Schematic

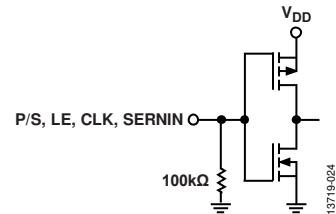


Figure 5. P/S, LE, CLK, and SERIN Interface Schematic

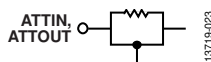


Figure 4. ATTIN, ATTOUT Interface Schematic



Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

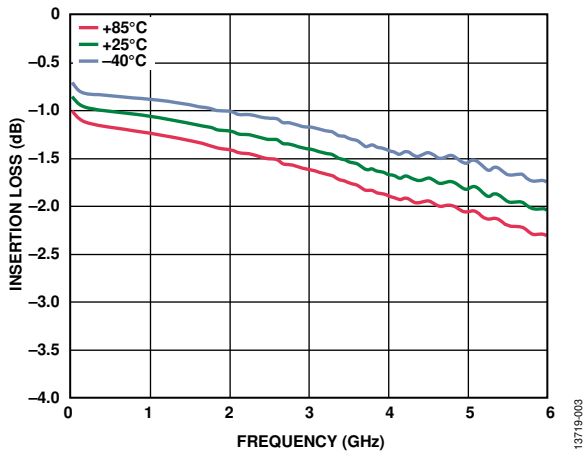


Figure 7. Insertion Loss vs. Frequency over Temperature

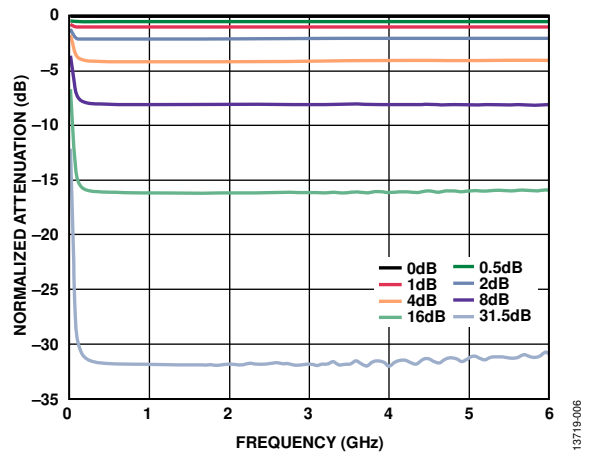


Figure 10. Normalized Attenuation vs. Frequency over Major Attenuation States

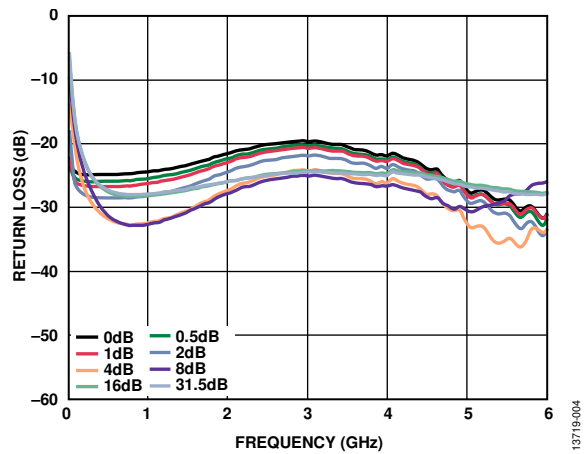


Figure 8. Input Return Loss vs. Frequency over Major Attenuation States

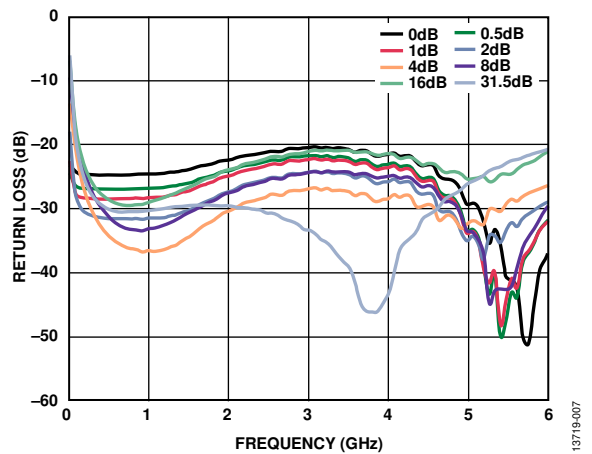


Figure 11. Output Return Loss vs. Frequency over Major Attenuation States

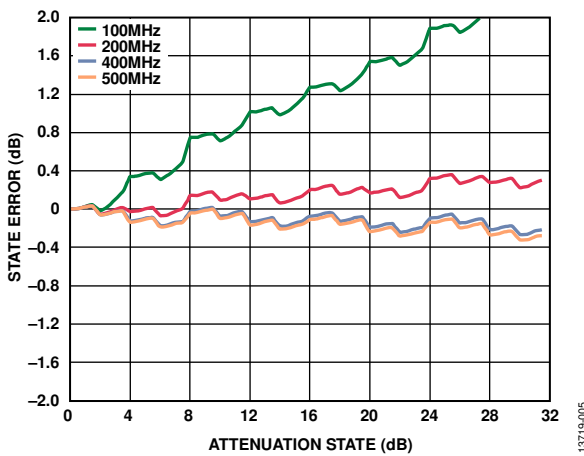


Figure 9. State Error vs. Attenuation State over Frequency (100 MHz to 500 MHz)

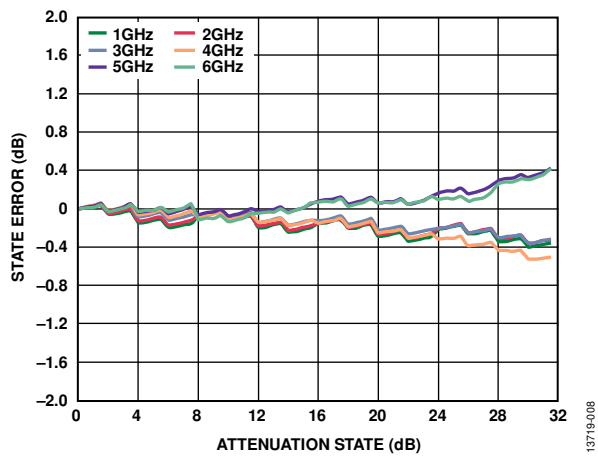


Figure 12. State Error vs. Attenuation State Over Frequency (1 GHz to 6 GHz)

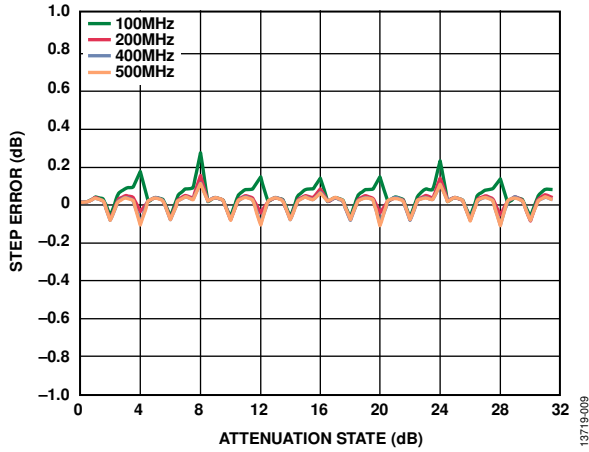


Figure 13. Step Error vs. Attenuation State over Frequency (100 MHz to 500 MHz)

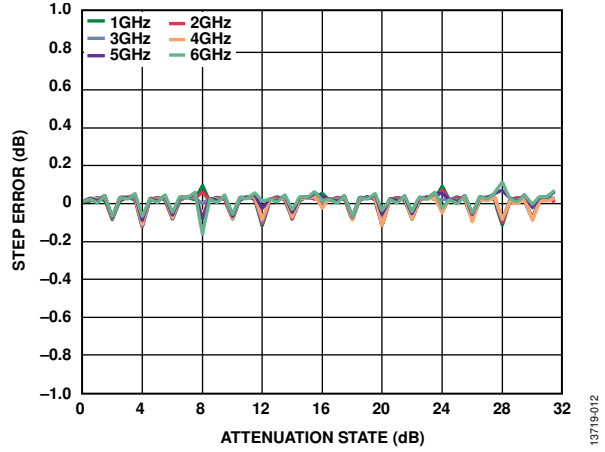


Figure 16. Step Error vs. Attenuation State over Frequency (1 GHz to 6 GHz)

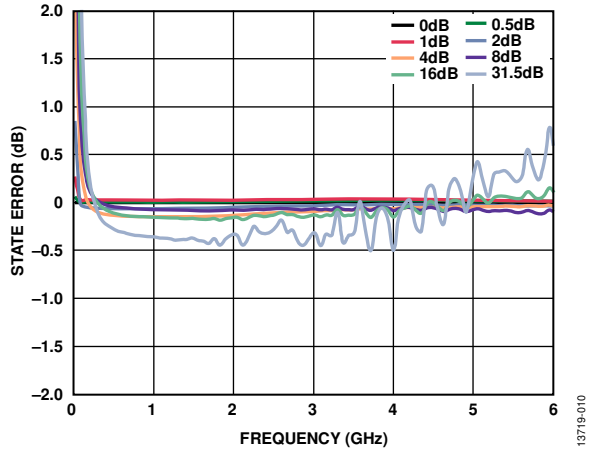


Figure 14. State Error vs. Frequency over Major Attenuation States

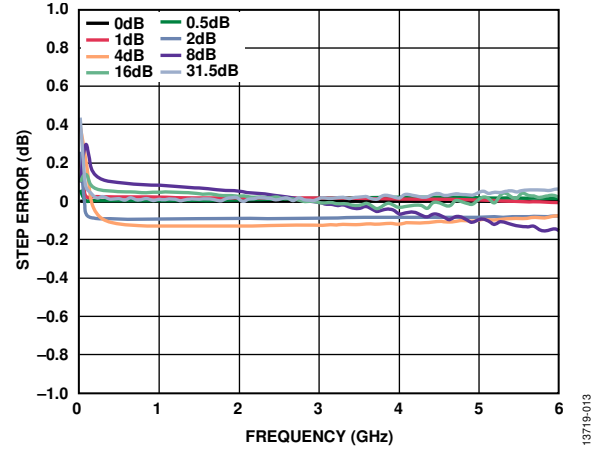


Figure 17. Step Error vs. Frequency over Major Attenuation States

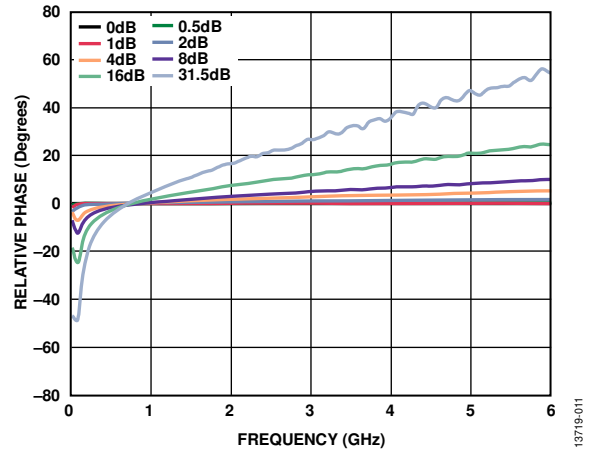


Figure 15. Relative Phase vs. Frequency over Major Attenuation States

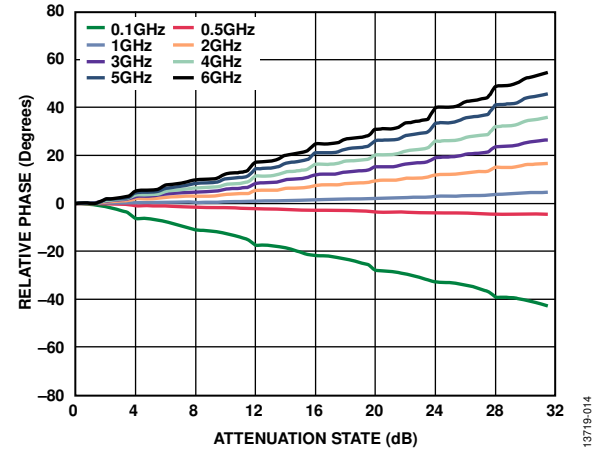


Figure 18. Relative Phase vs. Attenuation States over Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

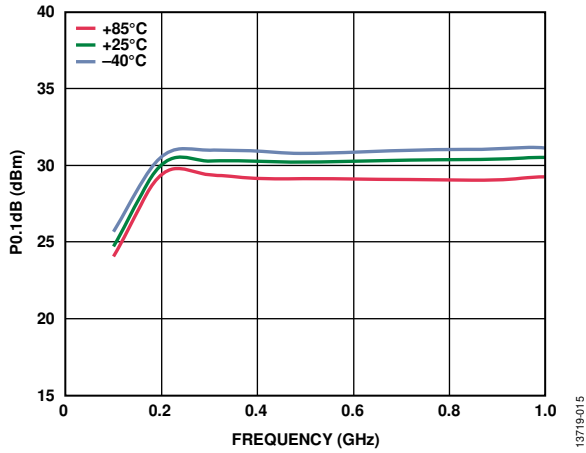


Figure 19. Input P0.1dB vs. Frequency (0.1 GHz to 1 GHz) at Minimum Attenuation State over Temperature

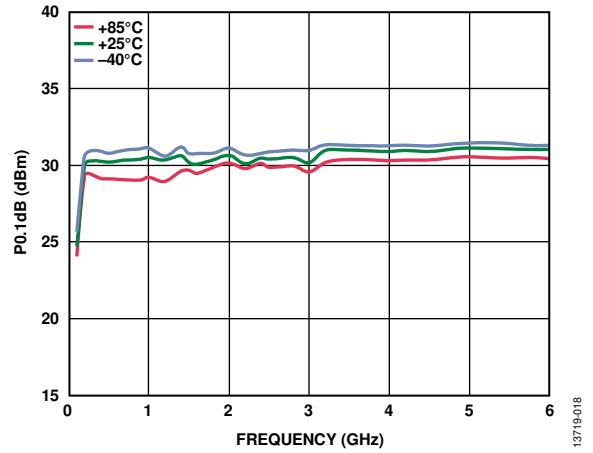


Figure 22. Input P0.1dB vs. Frequency (0.1 GHz to 6 GHz) at Minimum Attenuation State over Temperature

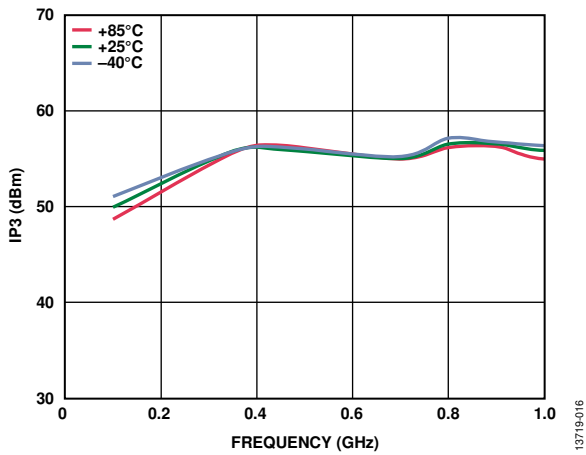


Figure 20. Input IP3 vs. Frequency (0.1 GHz to 1 GHz) at Minimum Attenuation State over Temperature

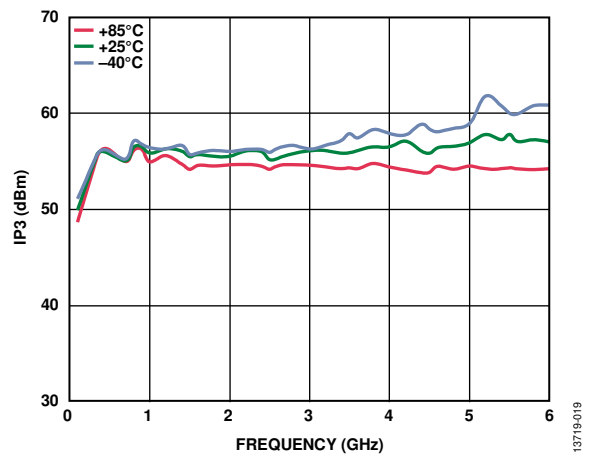


Figure 23. Input IP3 vs. Frequency (0.1 GHz to 6 GHz) at Minimum Attenuation State over Temperature

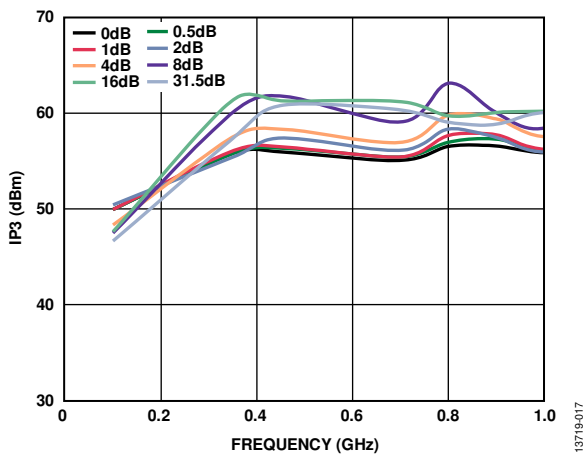


Figure 21. Input IP3 vs. Frequency (0.1 GHz to 1 GHz) over Major Attenuation States

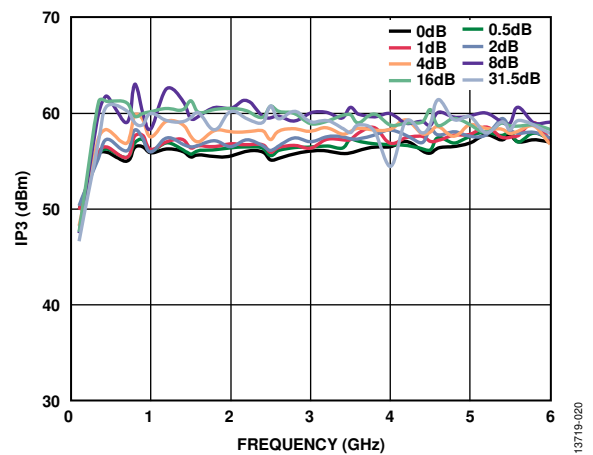


Figure 24. Input IP3 vs. Frequency (0.1 GHz to 6 GHz) over Major Attenuation States

THEORY OF OPERATION

The HMC1122 incorporates a 6-bit fixed attenuator array that offers an attenuation range of 31.5 dB in 0.5 dB steps. An integrated driver enables both serial and parallel mode control of the attenuator array (see Figure 25).

POWER SUPPLY

The HMC1122 requires a single dc voltage applied to the VDD pin. The ideal power-up sequence is as follows:

1. Connect the GND pin to a ground reference.
2. Apply a supply voltage to the VDD pin.
3. Power up the digital control inputs. The relative order of the digital control inputs is not important.
4. Apply an RF input signal to ATTIN or ATTOUT.

RF INPUT AND OUTPUT

The attenuator in the HMC1122 is bidirectional; ATTIN and ATTOUT pins are interchangeable as the RF input and output ports. The attenuator is internally matched to 50 Ω at both the input and the output; therefore, no external matching components are required. RF pins are dc-coupled; therefore, dc blocking capacitors are required on the RF lines.

SERIAL OR PARALLEL MODE SELECTION

The HMC1122 can be controlled in either serial or parallel mode by setting the P/S pin to high or low, respectively (see Table 4).

Table 4. Mode Selection

| P/S | Control Mode |
|------|--------------|
| Low | Parallel |
| High | Serial |

SERIAL MODE INTERFACE

The HMC1122 has a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to high.

In serial mode, the 6-bit SERIN data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 26 in conjunction with Table 5 and Table 6.

The HMC1122 also features a serial data output pin, SEROUT, that outputs serial input data delayed by six clock cycles to control the cascaded attenuator using a single SPI bus.

In serial mode operation, the parallel control inputs must always be kept at a valid logic level (V_{IH} or V_{IL}) and not be left floating. It is recommended to connect all parallel control inputs (D0 to D5) to ground.

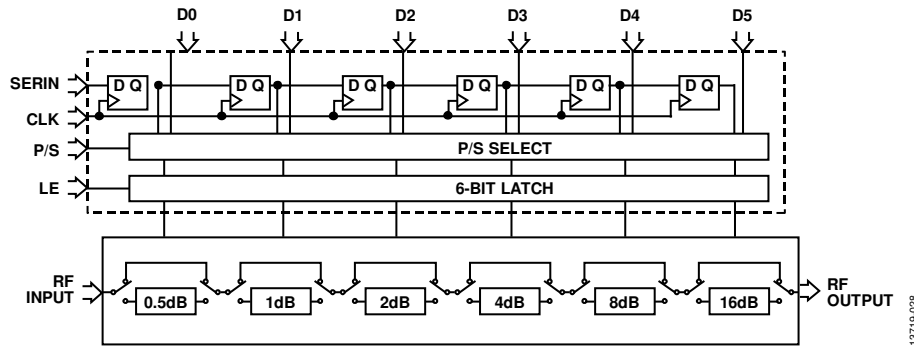


Figure 25. Functional Block Diagram

Table 5. D5 to D0 Truth Table

| Digital Control Input ¹ | | | | | | Attenuation State (dB) |
|------------------------------------|------|------|------|------|------|------------------------|
| D5 | D4 | D3 | D2 | D1 | D0 | |
| High | High | High | High | High | High | 0 (Reference) |
| High | High | High | High | High | Low | 0.5 |
| High | High | High | High | Low | High | 1.0 |
| High | High | High | Low | High | High | 2.0 |
| High | High | Low | High | High | High | 4.0 |
| High | Low | High | High | High | High | 8.0 |
| Low | High | High | High | High | High | 16.0 |
| Low | Low | Low | Low | Low | Low | 31.5 |

¹ Any combination of the control voltage input states shown in Table 5 provides an attenuation equal to the sum of the bits selected.

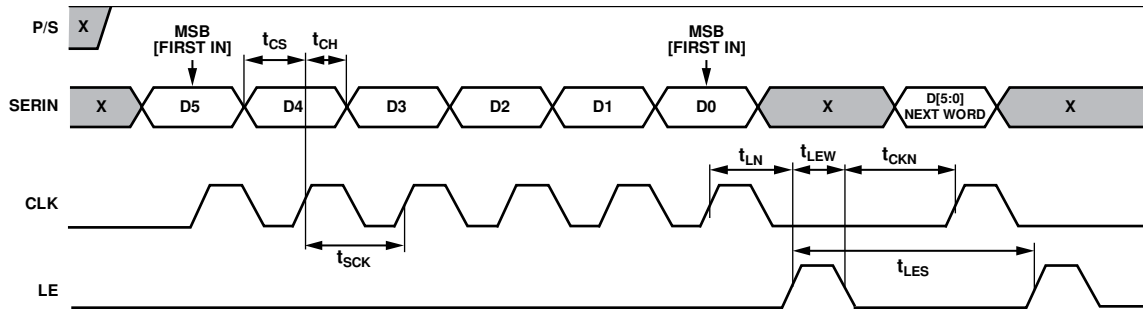


Figure 26. Serial Mode Timing Diagram

13719-029

Table 6. Timing Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|-----------|---|-----|-----|-----|------|
| t_{SCK} | Minimum serial period, see Figure 26 | 70 | | | ns |
| t_{CS} | Control setup time, see Figure 26 | 15 | | | ns |
| t_{CH} | Control hold time, see Figure 26 | | 20 | | ns |
| t_{LN} | LE setup time, see Figure 26 | 15 | | | ns |
| t_{LEW} | Minimum LE pulse width, see Figure 26 and Figure 27 | | 10 | | ns |
| t_{LES} | Minimum LE pulse spacing, see Figure 26 | | 630 | | ns |
| t_{CKN} | Serial clock hold time from LE, see Figure 26 | | 0 | | ns |
| t_{PH} | Hold time, see Figure 27 | | 10 | | ns |
| t_{PS} | Setup time, see Figure 27 | | 2 | | ns |

PARALLEL MODE INTERFACE

The HMC1122 has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 5. The parallel control interface is activated when P/S is set to low. In parallel mode operation, the parallel control inputs (D0 to D5) must always be kept at a valid logic level (V_{IH} or V_{IL}). It is recommended to use pull-down resistors on all parallel control input lines if the device driving them goes to a high impedance state during hibernation.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

The LE pin must be kept high. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

The LE pin must be kept low when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled high to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled low to latch the change into the device until the next desired attenuation change (see Figure 27 in conjunction with Table 6).

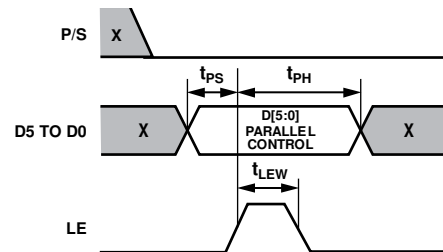


Figure 27. Latched Parallel Mode Timing Diagram

13719-030

POWER-UP INTERFACE

The HMC1122 uses the PUP1 and PUP2 control voltage inputs to set the attenuation value to a known value at power-up before the initial control data word is provided in either serial or parallel mode. When the attenuator powers up with LE = low, the state of PUP1 and PUP2 determines the power-up state of the device per the truth table shown in Table 7. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Table 7. PUPx Truth Table¹

| Attenuation State | LE | PUP1 | PUP2 |
|------------------------|------|------------|------------|
| 31.5 dB | Low | Low | Low |
| 24.0 dB | Low | High | Low |
| 16.0 dB | Low | Low | High |
| 0 dB (Reference) | Low | High | High |
| Determined by D0 to D5 | High | Don't care | Don't care |

¹ The PUPx pins must always be kept at a valid logic level (V_{IH} or V_{IL}) and not be left floating.

APPLICATIONS INFORMATION

EVALUATION PRINTED CIRCUIT BOARD

The schematic of the [HMC1122](#) evaluation board is shown in Figure 28. The [HMC1122](#) evaluation board is constructed of a 4-layer material with a copper thickness of 0.7 mil on each layer. Every copper layer is separated with a dielectric material. The top dielectric material is 10 mil RO4350. The middle and bottom dielectric materials are FR-4, used for mechanical strength and overall board thickness of approximately 62 mil, which allows SMA connectors to be slipped in at the board edges.

All RF and dc traces are routed on the top copper layer. The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a width of 18 mil, spacing of 13 mil, and dielectric thickness of 10 mil, to have a characteristic impedance of 50 Ω . The inner and bottom layers are grounded planes to provide a solid ground for the RF transmission lines. For optimal electrical and thermal performance, as many vias as possible are arranged around transmission lines and under the package exposed pad. The evaluation board layout shown in Figure 29 serves as a recommendation for optimal and stable performance, as well as for improvement of thermal efficiency.

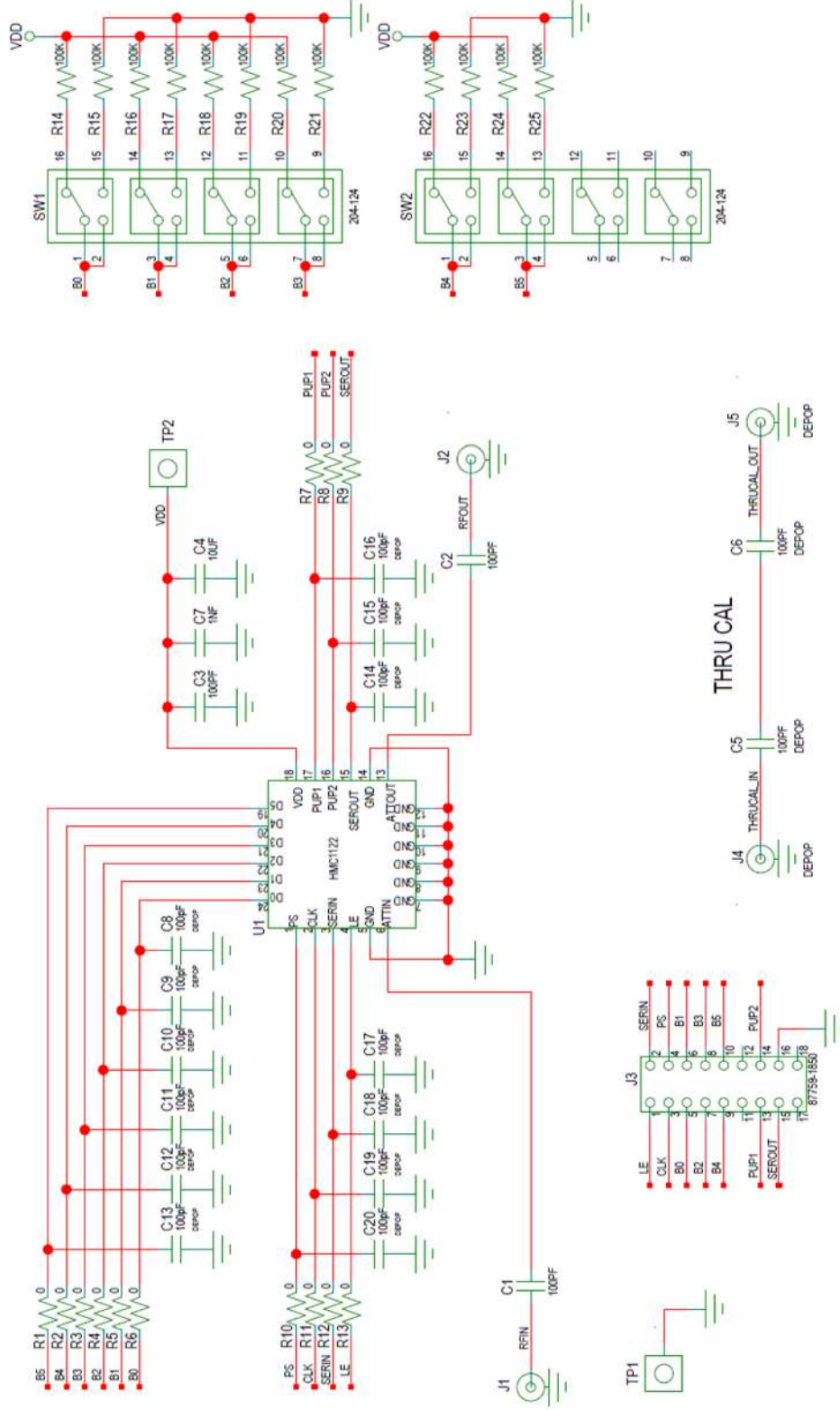
The evaluation board is grounded from the dc test point, TP1. The dc supply must be connected to the dc test point, TP2, of the evaluation board. Three decoupling capacitors are populated on the supply trace to filter high frequency noise.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines to the SMA connectors, J1 and J2, respectively. The ATTIN and ATTOUT ports are ac-coupled with capacitors of an appropriate value to ensure broadband performance. A thru calibration line connects J4 and J5; this transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

All the digital control pins are connected through digital signal traces to the 2 \times 9-pin header, J3. On the digital signal traces, provisions for an RC filter are made to clean any potential coupled noise. In normal operation, series resistors are 0 Ω and shunt capacitors are open.

The [HMC1122](#) evaluation board also uses two dual inline package (DIP), four-position single-pole dual-throw (SPDT) switches for the manual control of the device in direct parallel mode.

EVALUATION BOARD SCHEMATIC AND ARTWORK



13719-025

Figure 28. Evaluation Board Schematic

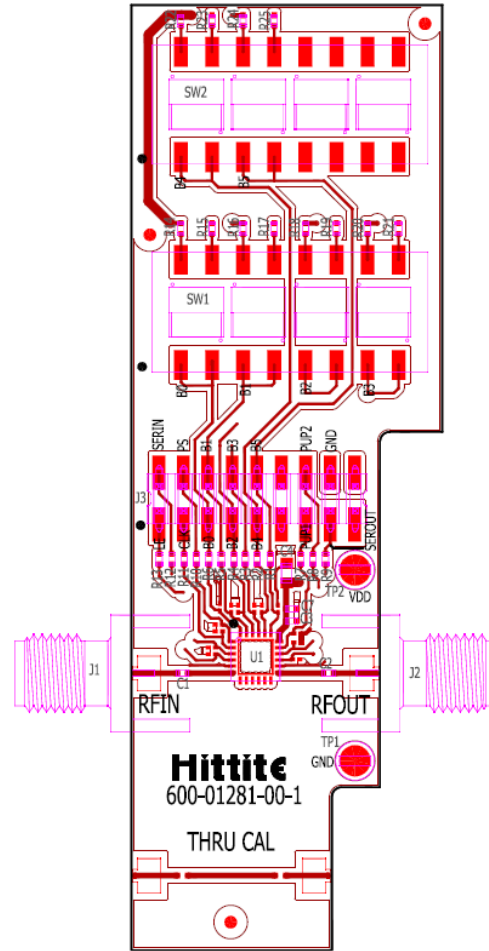


Figure 29. Evaluation Board Layout—Top View

Table 8. Evaluation Board Components

| Component | Default Value | Description |
|------------|--------------------------------|--|
| J1, J2 | Not applicable | SMA connector |
| J3 | Not applicable | 2 × 9-pin header |
| J4, J5 | Do not insert | SMA connector |
| TP1, TP2 | Not applicable | Through hole mount test point |
| C1, C2 | 100 pF | Capacitor, 0402 package |
| C3 | 100 pF | Capacitor, 0402 package |
| C4 | 10 μF | Capacitor, 0603 package |
| C7 | 1 nF | Capacitor, 0402 package |
| C5, C6 | Do not insert | Capacitor, 0402 package |
| C8 to C20 | Do not insert | Capacitor, 0402 package |
| SW1, SW2 | Not applicable | SPDT four-position DIP switch |
| R1 to R13 | 0 Ω | Resistor, 0402 package |
| R14 to R25 | 100 kΩ | Resistor, 0402 package |
| U1 | HMC1122 | HMC1122 digital attenuator, Analog Devices, Inc. |
| PCB | EV2HMC1122LP4M | 600-01281-00-1 evaluation PCB, Analog Devices |

OUTLINE DIMENSIONS

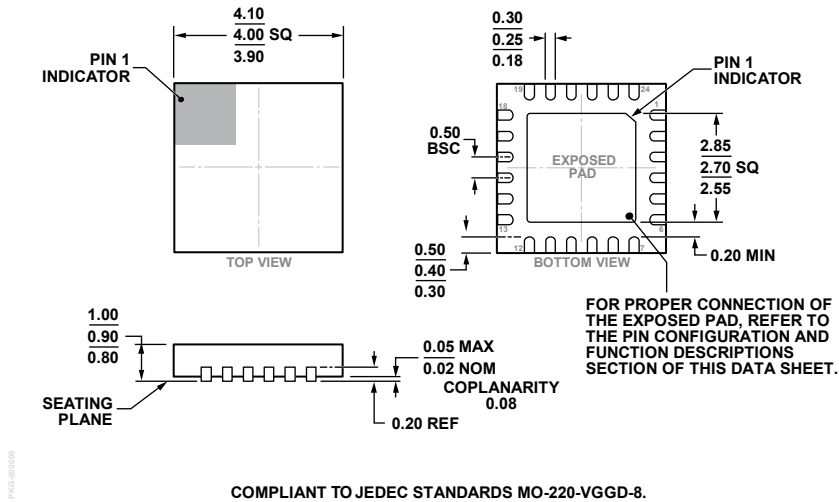


Figure 30. 24-Lead Lead Frame Chip Scale Package [LFCSP]
 4 mm × 4 mm Body and 0.90 mm Package Height
 (CP-24-16)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | MSL Rating ² | Package Description | Package Option | Branding ³ |
|--------------------|-------------------|-------------------------|---|----------------|-----------------------|
| HMC1122LP4ME | -40°C to +85°C | MSL3 | 24-Lead Lead Frame Chip Scale Package [LFCSP] | CP-24-16 | H1122 XXXX |
| HMC1122LP4METR | -40°C to +85°C | MSL3 | 24-Lead Lead Frame Chip Scale Package [LFCSP] | CP-24-16 | H1122 XXXX |
| EV2HMC1122LP4M | | | Evaluation Board | | |

¹ HMC1122LP4ME and HMC1122LP4METR are RoHS compliant parts.

² See the Absolute Maximum Ratings section.

³ XXXX is the 4-digit lot number.