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HMC1190ALP6NE

v01.0116

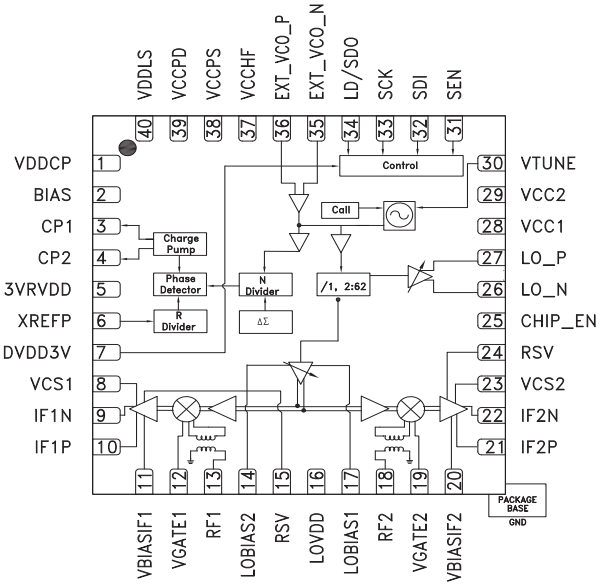
BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.8 GHz

Typical Applications

The HMC1190ALP6NE is Ideal for:

- Multiband/Multi-standard Cellular BTS Diversity Receivers
- GSM & 3G & LTE/WiMAX/4G
- MIMO Infrastructure Receivers
- Wideband Radio Receivers
- Multiband Basestations & Repeaters

Functional Diagram



Features

Broadband Operation with no external matching

High-side and Low-side LO injection Operation

High Input IP3 of +24 dBm

Power Conversion Gain of 8.9 dB

Input P1dB of 11 dBm

SSB Noise Figure of 9 dB

55 dBc Channel-to-Channel Isolation

Enable/Disable Mixer and PLLVCO independently

Single-ended RF input ports

Maximum Phase Detector Rate: 100 MHz

Low Phase Noise: -110 dBc/Hz in Band Typical

PLL FOM:

-230 dBc/Hz Integer Mode, -227 dBc/Hz Fractional Mode

< 180 fs Integrated RMS Jitter (1 kHz to 20 MHz)

LO Low Noise Floor: -165 dBc/Hz

Mixer Low Noise Floor: -161 dBc/Hz

Integrated VCO

External VCO Input, differential LO output

Exact Frequency Mode:
0 Hz Fractional Frequency Error

Programmable RF Output Phase

Output Phase Synchronous Frequency Changes

Output Phase Synchronization

LO Output Mute Function

Compact Solution, 6x6 mm Leadless QFN Package

General Description

The HMC1190ALP6NE is a high linearity broadband dual channel downconverting mixer with integrated PLL and VCO optimized for multi-standard receiver applications that require a compact, low power design. Integrated wideband limiting LO amplifiers enable the HMC1190ALP6NE to achieve an unprecedented RF bandwidth of 700 MHz to 3800 MHz for applications including Cellular/3G, LTE/WiMAX/4G. Unlike conventional narrow-band downconverters, the HMC1190ALP6NE supports both high-side and low-side LO injection over all RF frequencies. The RF and LO input ports are internally matched to 50 Ohms.

The HMC1190ALP6NE features an integrated LO and RF baluns, enable control of IF and LO amplifiers and bias control interface to high linearity passive mixer cores. Balanced passive mixer combined with high-linearity IF amplifier architecture provides excellent LO-to-RF, LO-to-IF, and RF-to-IF isolations. Low noise figure of 9 dB, and high IIP3 of +24 dBm allow the HMC1190ALP6NE to be used in most demanding applications. External bias control pins enable optimization of already low power dissipation of 2.34 W (typical). Fast enable control interface reduces power consumption further in TDD applications.

External VCO input allows the HMC1190ALP6NE to lock external VCOs, and enables cascaded LO architectures for MIMO applications. Two separate Charge Pump (CP) outputs enable separate loop filters optimized for both integrated and external VCOs, and seamless switching between integrated or external VCOs during operation. Programmable RF output phase features can further phase adjust and synchronize multiple HMC1190ALP6NE's enabling scalable MIMO and beam-forming radio architectures.

Additional features include configurable LO output mute function, Exact Frequency Mode that enables the HMC1190ALP6NE to generate fractional frequencies with 0 Hz frequency error, and the ability to synchronously change frequencies without changing phase of the output signal that increases efficiency of digital pre-distortion loops. The HMC1190ALP6NE is housed in RoHS compliant compact 6x6 mm leadless QFN package.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.8 GHz

Table 1. Electrical Specifications

T_A = +25°C, IF Frequency = 150 MHz, LO Power is set to '3' [1], RF Input Power = -5 dBm, LOVDD=3VRVDD=DVDD3V=CHIPEN= 3.3V, VDDCP=VCS1=VCS2=VBIASIF1=VBIASIF2=LOBIAS1=LOBIAS2=VCC1=VCC2=VGATE1=VGATE2=5V unless otherwise noted.

Parameter	Typical												Units
Mixer Core RF Input Frequency Range	700 - 3800												MHz
Mixer Core IF Output Frequency Range	50 - 350												MHz
RF Frequency	900		1900		2200		2700		3500		3800		MHz
Side Band[2]	LSB	USB	LSB	USB	LSB	USB	LSB	USB	LSB	USB	LSB	USB	
Conversion Gain[3]	9	8.9	8.3	8.5	7.9	8.1	7.1	7.6	6 [4]	6.2 [4]	4.7 [4]	4.7 [4]	dB
IIP3	24.5	22.7	26.5	25.5	26.9	26.2	27.1	27.5	27	27.9	27.1	28.3	dB
Noise Figure (SSB)	9.6	9.3	9.9	9.3	10.7	10.1	11.5	11	14	13.1	15.7	13.7	dB
Input 1 dB Compression	10.6	10.4	12.3	11.8	12.8	12.2	13.9	13.2	15.7	14.7	17.3	16.3	dBm
LO Leakage at RF Port	-47.6	-44.8	-49.2	-49.5	-50.4	-48.8	-44.2	-50.1	-48.8	-48.7	-51.1	-48.1	dBm
RF to IF Isolation	41.5	43.1	39.2	46.7	39.9	41.5	46.1	44.8	54.1	51	52	52.8	dBc
Channel to Channel Isolation[5]	56.1	55.9	52.6	53.5	51.4	51	49.4	49.8	43.5	44	43.5	44.3	dBc
+2RF-2LO Response	83	71.6	75.7	73.9	81.5	82.2	67.3	76.1	68.5	68	68.7	69.1	dBc
+3RF-3LO Response	89	73	75.3	74.8	86.7	74.1	79.7	73.6	75.2	71.8	75.5	69.9	dBc

[1] LO Power Level can be adjusted using Reg 16h

[2] LSB stands for lower side band and refers to RF<LO. USB stands for upper side band and refers to RF>LO.

[3] Balun losses at IF output ports are de-embedded.

[4] VGATE1 = VGATE2 = 4.9V

[5] RF1 input power= -5 dBm, measurement taken from IF2 output. RF2 and IF1 ports are terminated with 50 Ohms

Table 2. DC Power Supply Specifications

Parameter	Min.	Typ.	Max.	Units
5V Supply Rails (VDDCP, VCS1, VCS2, VDDLS, VBIASIF1, VBIASIF2, LOBIAS1, LOBIAS2, VCC1, VCC2)	4.5	5	5.5	V
	200 [1]	330	556 [2]	mA
3.3V Supply Voltage (LOVDD, 3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF)	3	3.3	3.6	V
	142 [1]	193	246 [2]	mA
VGATE1, VGATE2[3]	VDDIF-0.2	5	VDDIF	V
5V Supply Rails [4] (VDDCP, VCS1, VCS2, VDDLS, VBIASIF1, VBIASIF2, LOBIAS1, LOBIAS2, VCC1, VCC2) (5V)	324	330	338	mA
3.3V Supply Voltage [4] (LOVDD, 3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF) (3.3V)	185	193	200	mA

[1] LO Frequency=2400 MHz, LO_MIX is enabled in single ended mode, LO_OUT is disabled. LO_MIX power setting = 0, divide ratio = 1, divider stage high gain = 0

[2] LO Frequency=2400 MHz, LO_MIX and LO_OUT are both enabled in differential mode. LO_MIX and LO_OUT power setting = 3, divide ratio = 62, divider stage high gain = 1

[3] VGATE1 and VGATE2 are obtained through resistors which are connected to VDDIF

[4] LO Frequency=2400 MHz, LO_MIX is enabled in differential mode, LO_OUT is disabled. LO_MIX power setting = 3. When LO_OUT is enabled in differential mode the bias current increases by 34 mA (Typ.).

Table 2. DC Power Supply Specifications *(Continued)*

Parameter		Min.	Typ.	Max.	Units
Mixer Core Supply Currents when IF1EN and IF2EN are Enabled	VDDIF (5V)	139	146	152	mA
	VCS1 + VCS2 (5V)	2.7	3	3.1	mA
	VBIASIF1 + VBIASIF2 (5V)	20	21.5	23	mA
	VGATE1 + VGATE2	3	3	3	mA
	LOBIAS1 + LOBIAS2 (5V)	4	4	4	mA
	LOVDD (3.3V)	136	143	150	mA
Mixer Core Supply Currents when IF1EN and IF2EN are Disabled	VDDIF (5V)	0	0	0	mA
	VCS1 + VCS2 (5V)	3.2	3.45	3.6	mA
	VBIASIF1 + VBIASIF2 (5V)	1.3	1.6	1.9	mA
	VGATE1 + VGATE2 (5V)	0	0	0	mA
	LOBIAS1 + LOBIAS2 (5V)	4.5	4.9	5.2	mA
	LOVDD (3.3V)	3.2	3.45	3.6	mA
PLL/VCO Core Supply Currents when CHIPEN is Enabled	LO_OUT differential, LO_MIXER off [1] 5V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)	 144 44.5	 149 47	 154 49.5	 mA mA
	LO_OUT single-ended, LO_MIXER off [1] 5V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)	 126 44.5	 130 47	 133 49.5	 mA mA
	LO_OUT off, LO_MIXER differential [1] 5V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)	 144 44.5	 149 47	 154 49.5	 mA mA
	LO_OUT off, LO_MIXER single-ended [1] 5V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)	 127 44.5	 130 47	 132.5 49.5	 mA mA
	LO_OUT differential, LO_MIXER differential [1] 5V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)	 179 44.5	 184 47	 189 49.5	 mA mA
	LO_OUT single-ended, LO_MIXER single-ended [1] 5V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)	 146 44.5	 150 47	 154 49.5	 mA mA
	VCCPD, VCCPS, VCCHF, DVDD3V, 3VRVDD (+3.3V)	44.5	47	49.5	mA
PLL/VCO Core Supply Currents when CHIPEN is Disabled	VDDCP, VCC1, VCC2, VDDLS (5V) [1]	1	1	1	mA
	3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF (3.3V) [1]	5	5	5	mA

[1] LO Frequency=2400 MHz, LO_MIX and LO_OUT outputs set to maximum gain.

Table 3. PLL & VCO Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Logic Inputs					
Logic High		1.2			V
Logic Low				0.6	V
Input Current				±1	uA
Input Capacitance			2		pF
LO Output Characteristics					
LO Output Frequency		50		4100	MHz
VCO Frequency at PLL Input		2000		4100	MHz
VCO Fundamental Frequency		2000		4100	MHz
VCO Output Divider					
VCO Output Divider Range	1, 2, 4, ... 60, 62	1		62	
PLL RF Divider Characteristics					
19-Bit N Divider Range	Integer	16		524287	
	Fractional	20		524283	
Phase Detector (PD)					
PD Frequency	Fractional Mode	DC		100	MHz
	Integer Mode	DC		100	MHz
Harmonics					
fo Mode at 4000 MHz	2nd / 3rd / 4th		-30/-22/-32		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,... 62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled	1	2	3.3	Vpp
Ref Input Capacitance				5	pF
14-\Bit R-Divider Range		1		16,383	
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-167		dBc/Hz

Table 3. PLL & VCO Specifications *(Continued)*

Parameter	Conditions	Min.	Typ.	Max.	Units
VCO Open Loop Phase Noise at fo @ 3 GHz/2 = 1.5 GHz					
10 kHz Offset			-83		dBc/Hz
100 kHz Offset			-113		dBc/Hz
1 MHz Offset			-139.5		dBc/Hz
10 MHz Offset			-165.5		dBc/Hz
100 MHz Offset			-167		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 3862 MHz	Measured at 2.5 V		15		MHz/V
VCO Tuning Sensitivity at 3643 MHz	Measured at 2.5 V		14.5		MHz/V
VCO Tuning Sensitivity at 3491 MHz	Measured at 2.5 V		16.2		MHz/V
VCO Tuning Sensitivity at 3044 MHz	Measured at 2.5 V		14.6		MHz/V
VCO Tuning Sensitivity at 2558 MHz	Measured at 2.5 V		15.4		MHz/V
VCO Tuning Sensitivity at 2129 MHz	Measured at 2.5 V		14.8		MHz/V
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

Table 4. Enable/Disable Settling Time Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Enable Settling Time	Mixer Core Enabled		140		ns
Disable Settling Time	Mixer Core Disabled		110		ns

Figure 1. Low Side LO Conversion Gain vs. VGATE [1] [2]

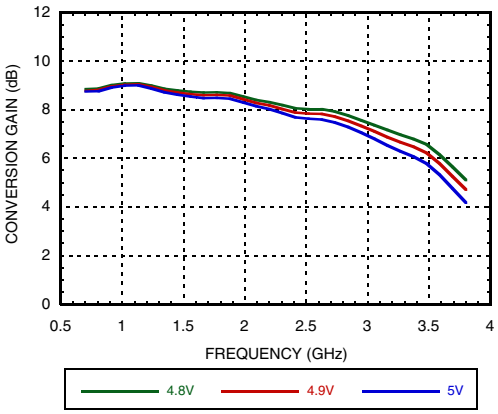


Figure 2. Low Side LO Input IP3 vs. VGATE [1]

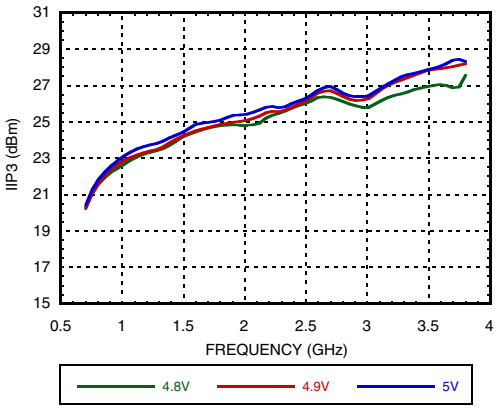


Figure 3. High Side LO Conversion Gain vs. VGATE [1] [2]

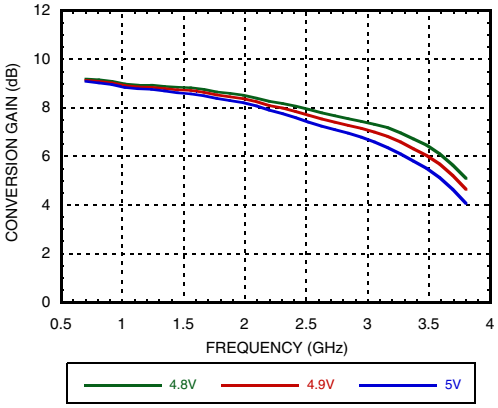


Figure 4. High Side LO Input IP3 vs. VGATE [1]

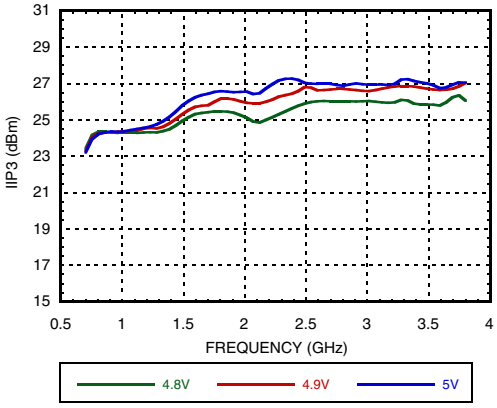


Figure 5. Low Side LO Noise Figure vs. VGATE [1]

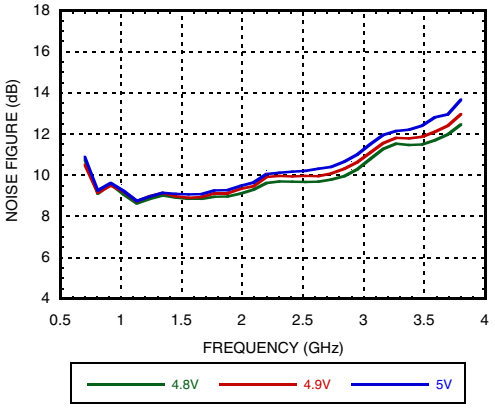
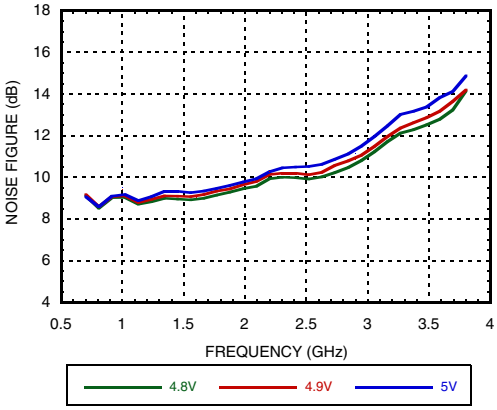


Figure 6. High Side LO Noise Figure vs. VGATE [1]



[1] VGATE is bias voltage for passive mixer cores (VGATE1 and VGATE2 pins). Refer to pin description table.

[2] Balun losses at IF output ports are de-embedded.

Figure 7. Conversion Gain vs. High Side LO & Low Side LO [1][2]

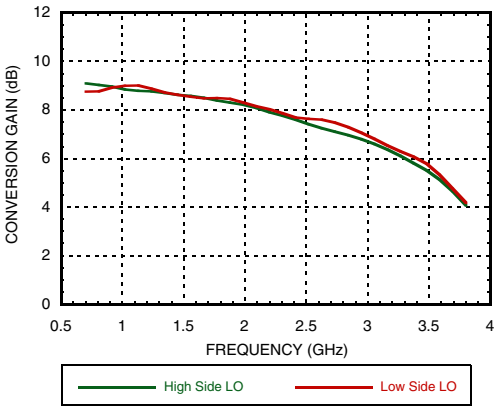


Figure 8. Input IP3 vs. High Side LO & Low Side LO[2]

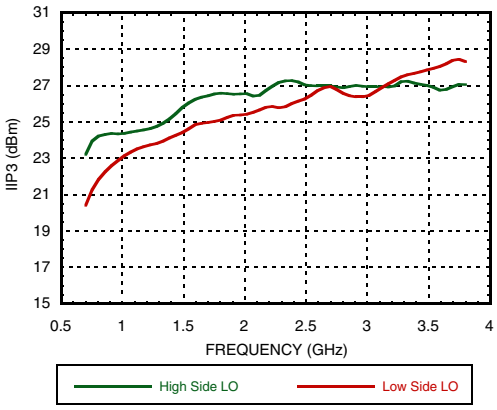


Figure 9. RF/IF Isolation vs. Temperature[2][3]

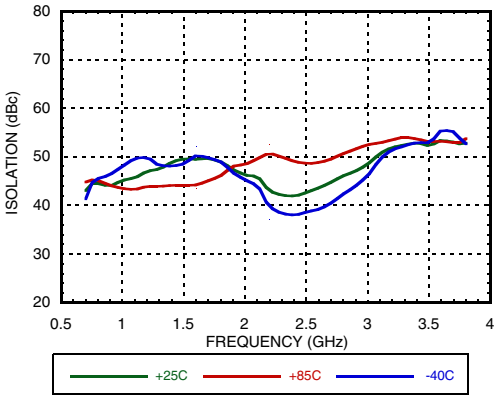


Figure 10. LO Leakage vs. Frequency[2][3]

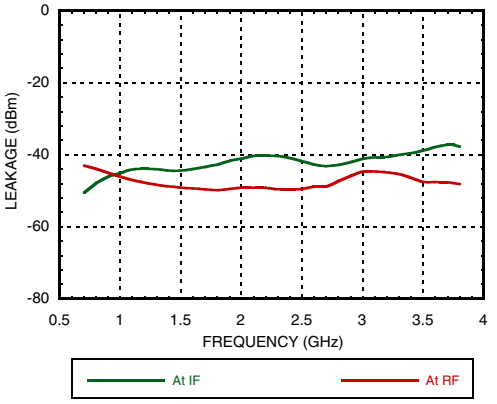


Figure 11. Low Side LO Conversion Gain vs. LO Drive [1][2]

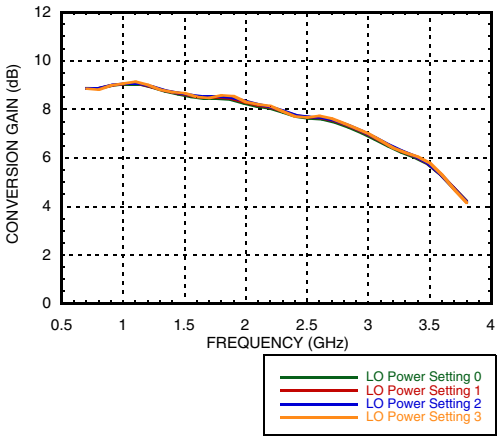
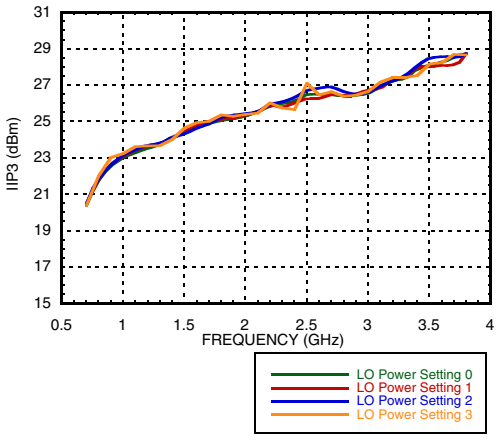


Figure 12. Low Side LO Input IP3 vs. LO Drive[2]



[1] Balun losses at IF output ports are de-embedded.

[2] VGATE=5V

[3] For low side LO

Figure 13. +2RF -2LO Response vs. Frequency over Temperature[1][2][3]

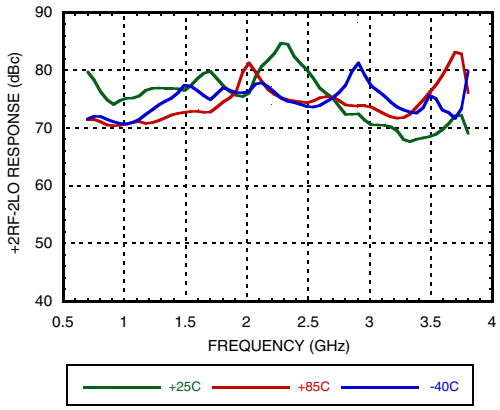


Figure 14. +3RF -3LO Response vs. Frequency over Temperature[1][2][3]

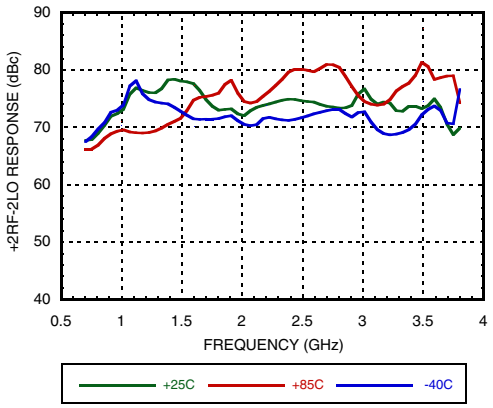


Figure 15. RF Input Return Loss vs. Frequency over Temperature[3][4]

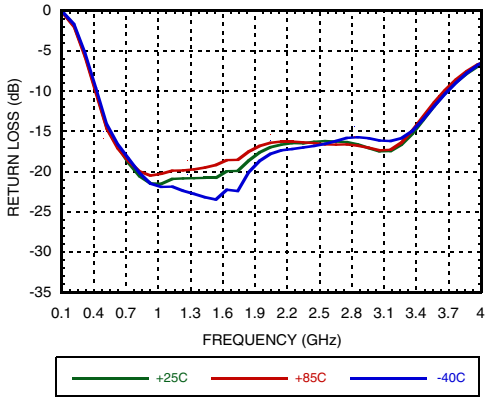


Figure 16. IF Output Return Loss vs. Frequency over Temperature [3][4]

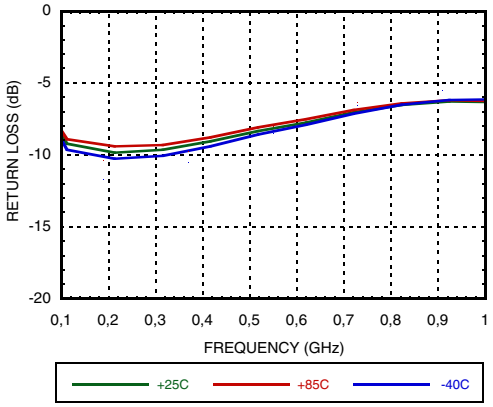


Figure 17. High Side LO Input P1dB vs. Frequency over Temperature[3]

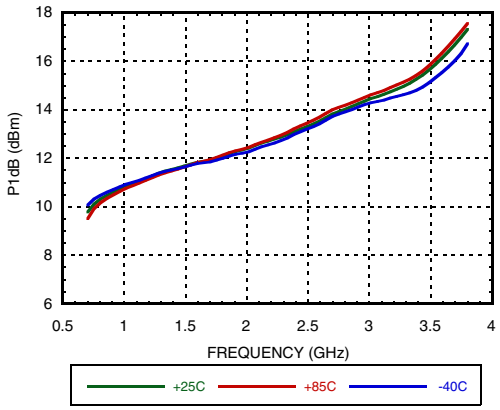
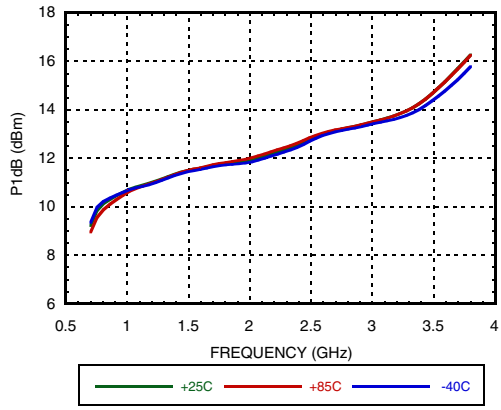


Figure 18. Low Side LO Input P1dB vs. Frequency over Temperature[3]



[1] Balun losses at IF output ports are de-embedded.

[2] Low side LO

[3] VGATE=5V

[4] LO input Frequency = 1900MHz, LO power setting is 3.

Figure 19. Low Side LO Conversion Gain vs. Frequency at VGATE=5V [1][2]

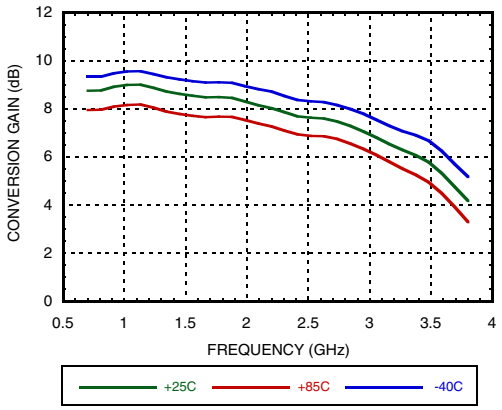


Figure 20. Low Side LO Input IP3 vs. Frequency at VGATE=5V[2]

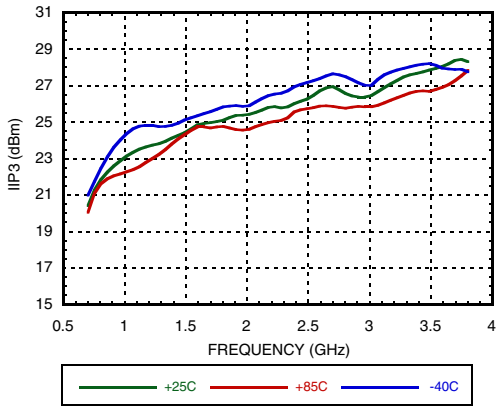


Figure 21. High Side LO Conversion Gain vs. Frequency at VGATE=5V [1][2]

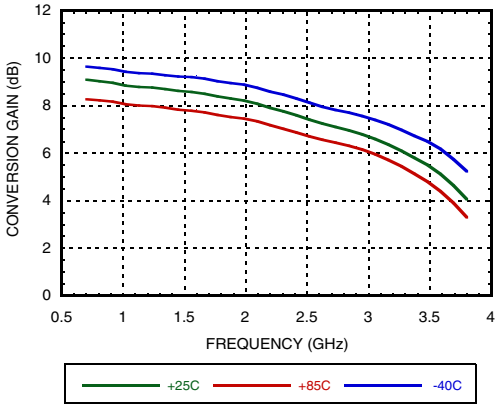


Figure 22. High Side LO Input IP3 vs. Frequency at VGATE=5V[2]

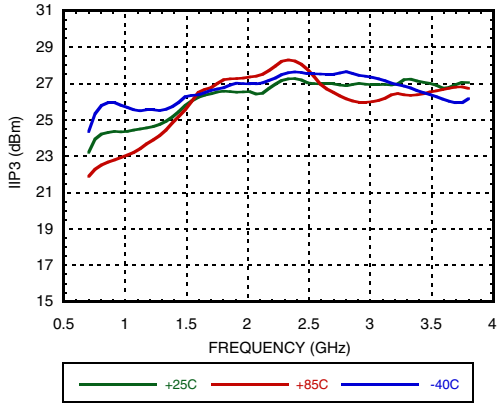


Figure 23. Low Side LO Noise Figure vs. Temperature at VGATE=5V

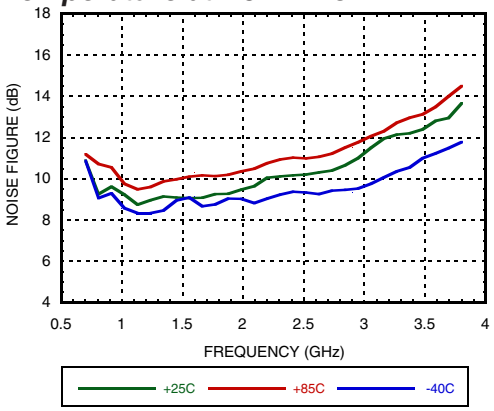
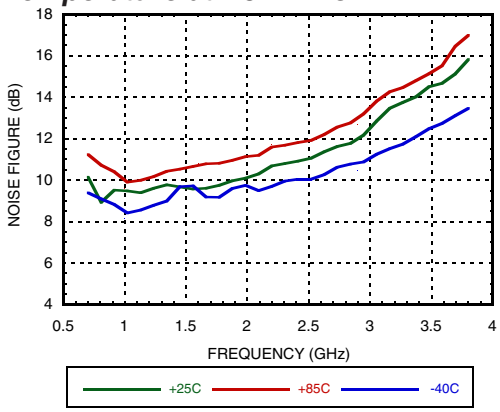


Figure 24. High Side LO Noise Figure vs. Temperature at VGATE=5V



[1] Balun losses at IF output ports are de-embedded.

[2] At room temperature

Figure 25. Low Side LO Conversion Gain vs. Frequency at VGATE=4.9V [1][2]

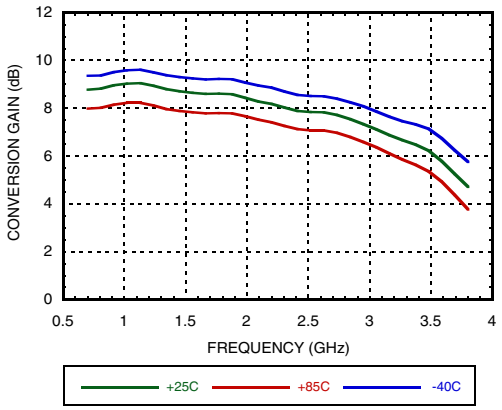


Figure 26. Low Side LO Input IP3 vs. Frequency at VGATE=4.9V[2]

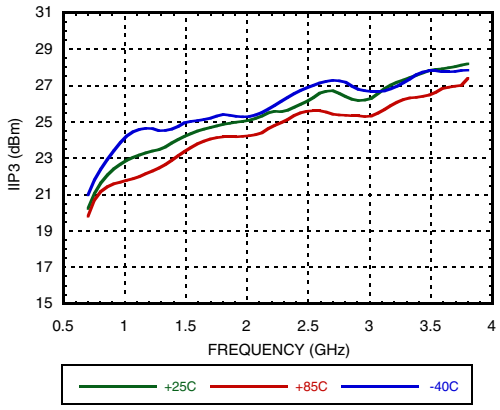


Figure 27. High Side LO Conversion Gain vs. Frequency at VGATE=4.9V [1][2]

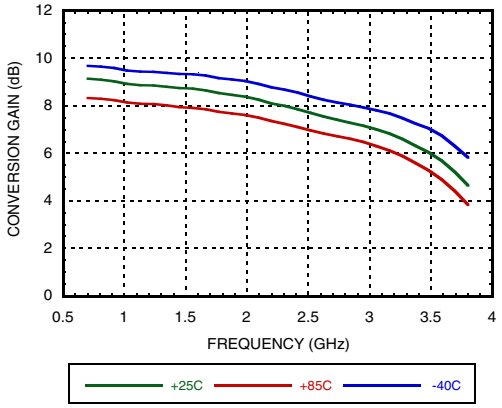


Figure 28. High Side LO Input IP3 vs. Frequency at VGATE=4.9V[2]

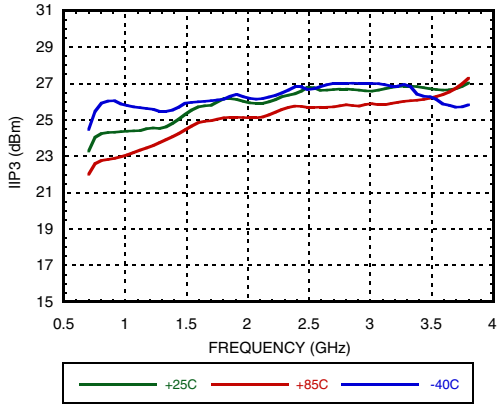


Figure 29. Low Side LO Noise Figure vs. Temperature at VGATE=4.9V

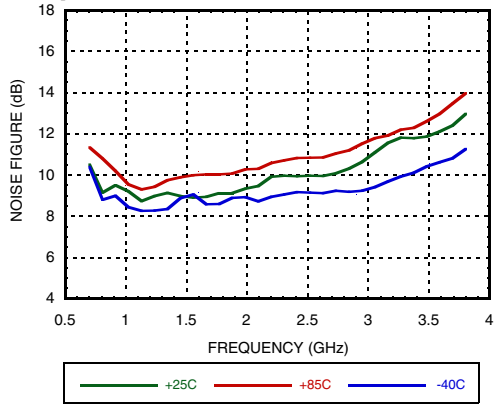
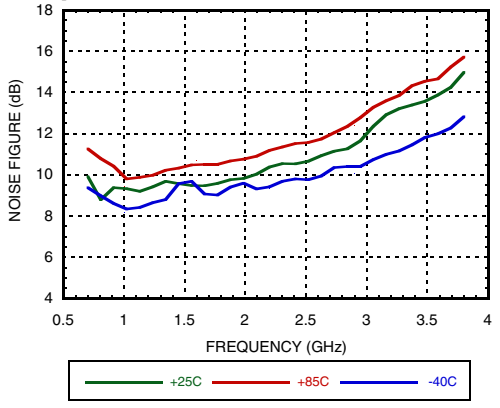


Figure 30. High Side LO Noise Figure vs. Temperature at VGATE=4.9V



[1] Balun losses at IF output ports are de-embedded.

[2] At room temperature

Figure 31. Low Side LO Conversion Gain vs. Frequency at VGATE=4.8V [1][2]

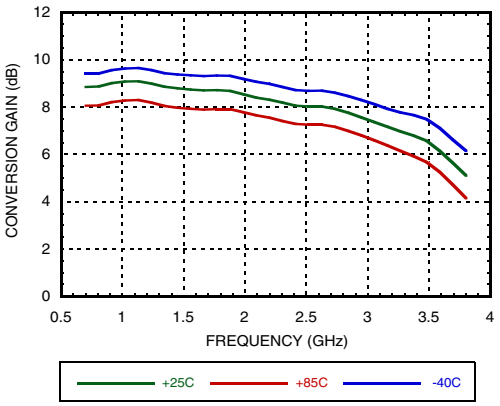


Figure 32. Low Side LO Input IP3 vs. Frequency at VGATE=4.8V[2]

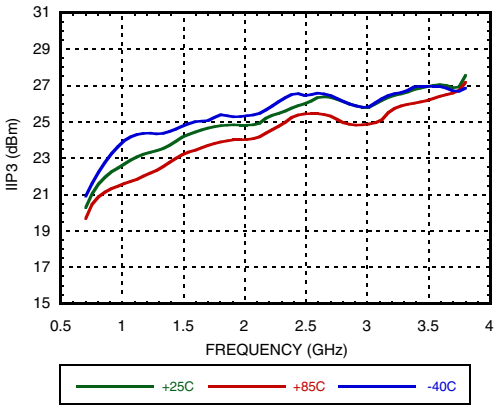


Figure 33. High Side LO Conversion Gain vs. Frequency at VGATE=4.8V [1][2]

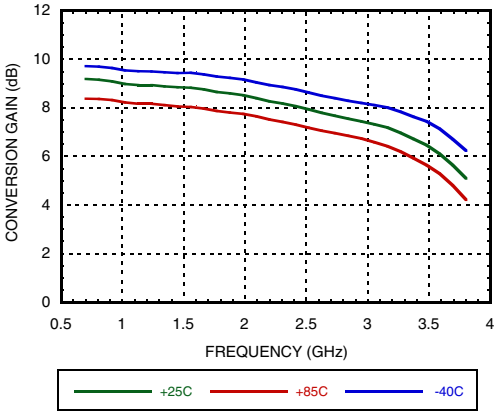


Figure 34. High Side LO Input IP3 vs. Frequency at VGATE=4.8V[2]

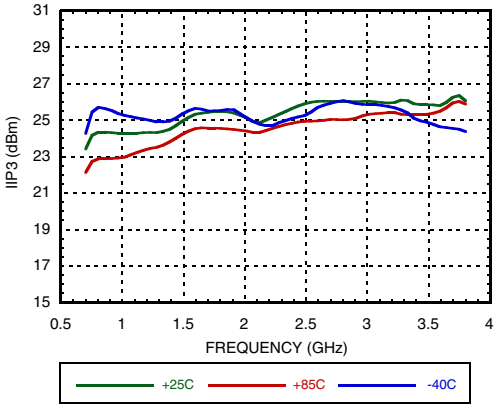


Figure 35. Low Side LO Noise Figure vs. Temperature at VGATE=4.8V

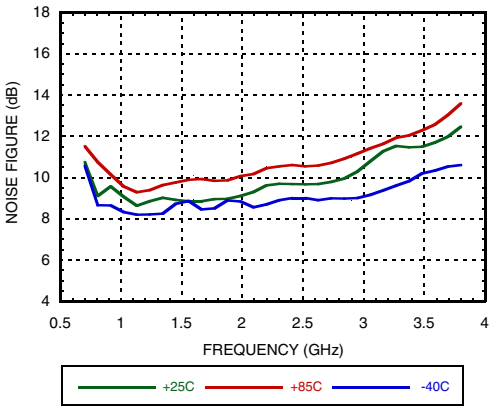
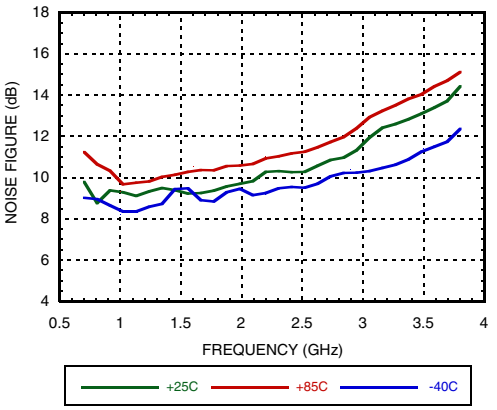


Figure 36. High Side LO Noise Figure vs. Temperature at VGATE=4.8V



[1] Balun losses at IF output ports are de-embedded.

[2] At room temperature

Figure 37. Channel to Channel Isolation vs. Frequency

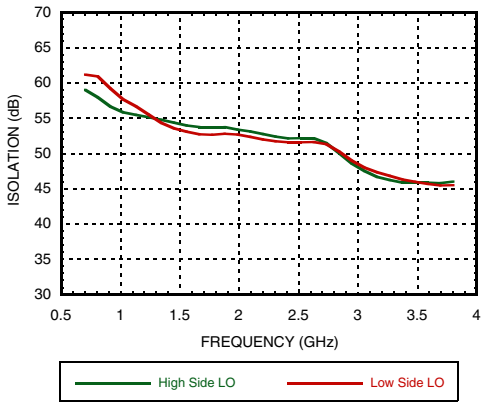


Figure 38. Channel to Channel Isolation vs. IF Frequency

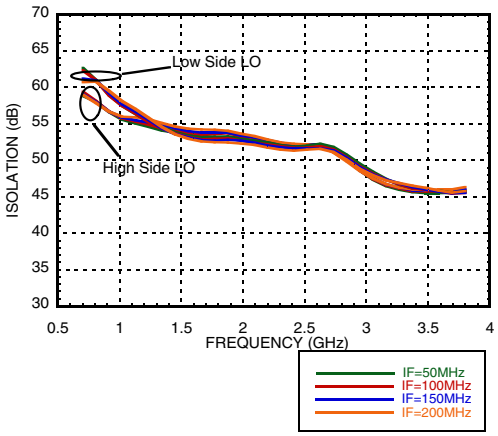


Figure 39. Low Side LO Conversion Gain Mismatch at VGATE=5V [1]

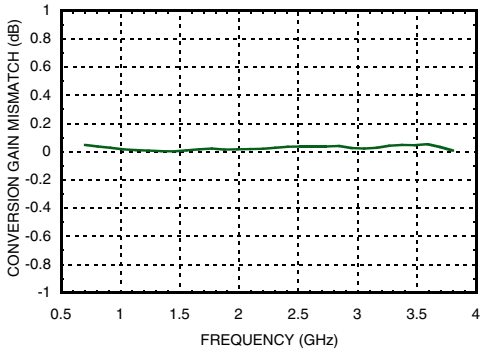


Figure 40. Low Side LO Input IP3 Mismatch at VGATE=5V

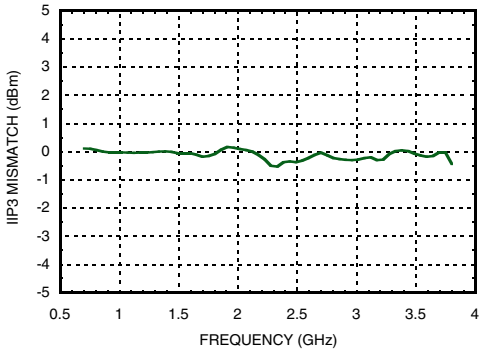


Figure 41. Low Side LO Conversion Gain vs. VGATE=VDDIF[1]

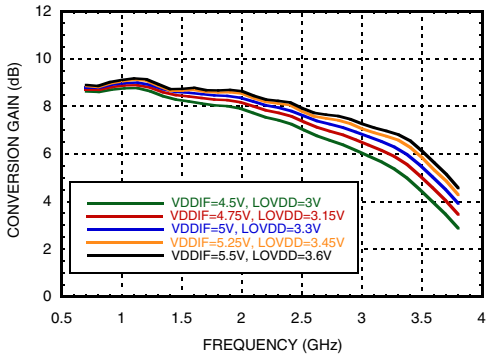
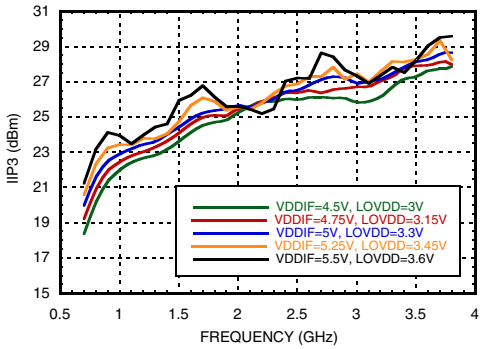


Figure 42. Low Side LO Input IP3 vs. VGATE=VDDIF



[1] Balun losses at IF output ports are de-embedded.

Figure 43. Conversion Gain vs. IF Frequency at RF=900 MHz, VGATE=5V [1]

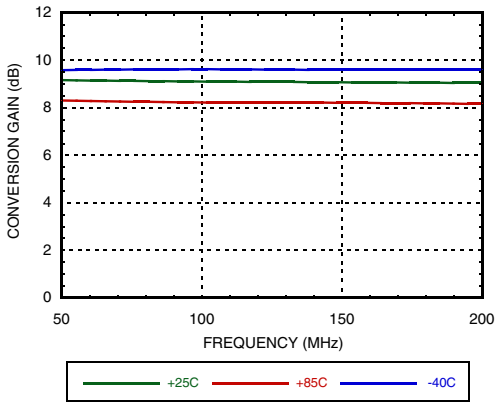


Figure 44. IIP3 vs. IF Frequency at RF=900 MHz, VGATE=5V

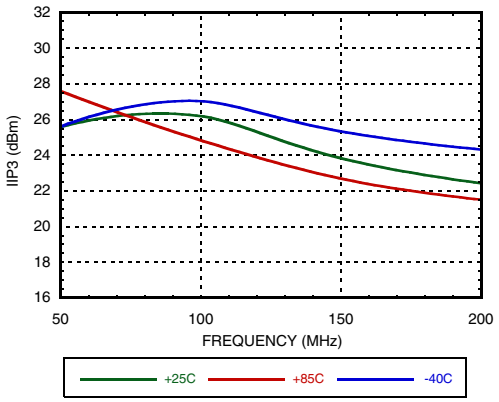


Figure 45. Conversion Gain vs. IF Frequency at RF=1900 MHz, VGATE=5V [1]

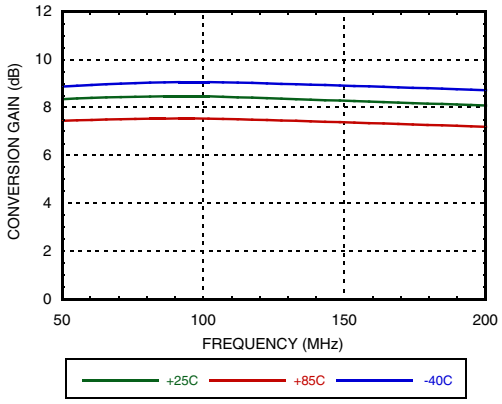


Figure 46. IIP3 vs. IF Frequency at RF=1900 MHz, VGATE=5V

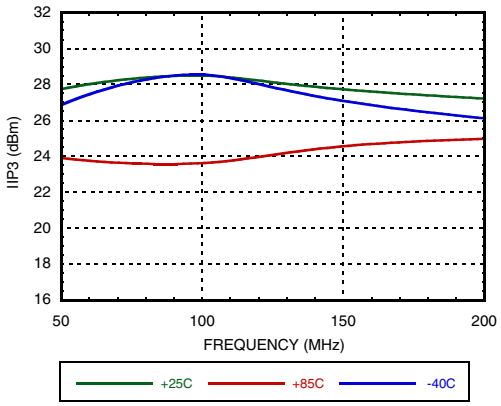


Figure 47. Conversion Gain vs. IF Frequency at RF=2400 MHz, VGATE=5V [1]

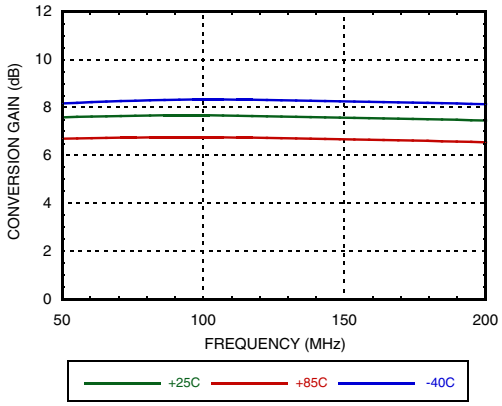
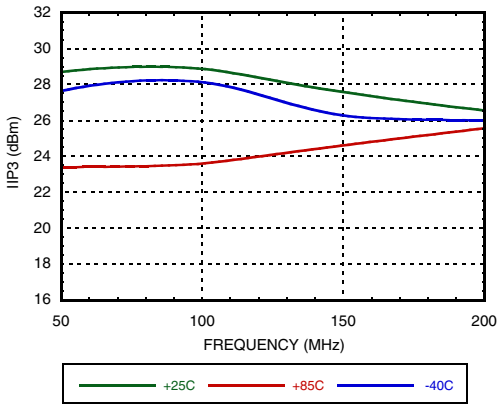


Figure 48. IP3 vs. IF Frequency at RF=2400 MHz, VGATE=5V



[1] Balun losses at IF output ports are de-embedded.

Figure 49. Auxiliary LO Output, Open Loop Phase Noise at 3600 MHz

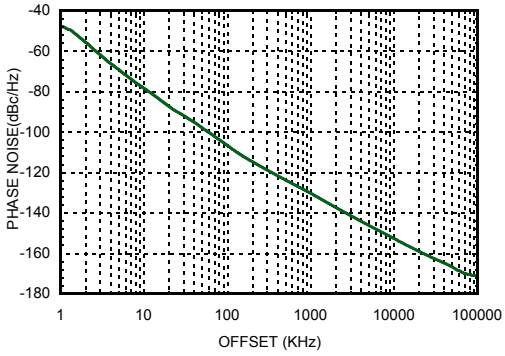


Figure 50. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise at 3600 MHz with various divider ratios [1]

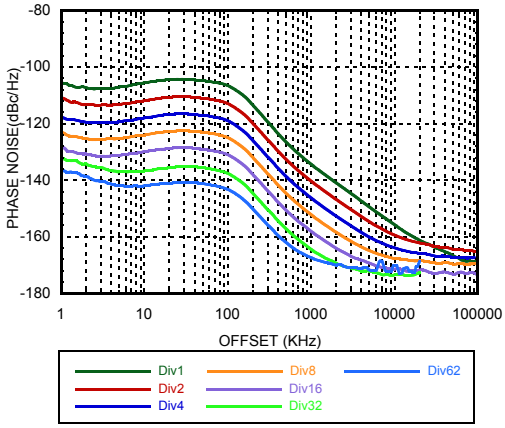


Figure 51. Auxiliary LO Output, Open Loop Phase Noise at 4100 MHz

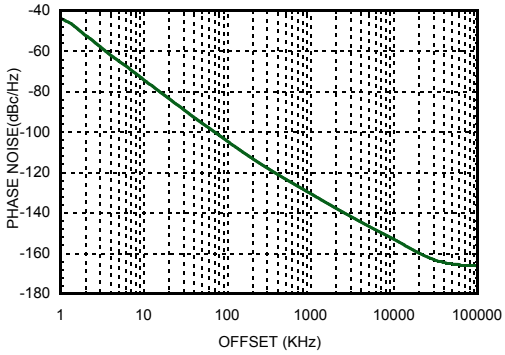


Figure 52. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise at 4100 MHz with various divider ratios [1]

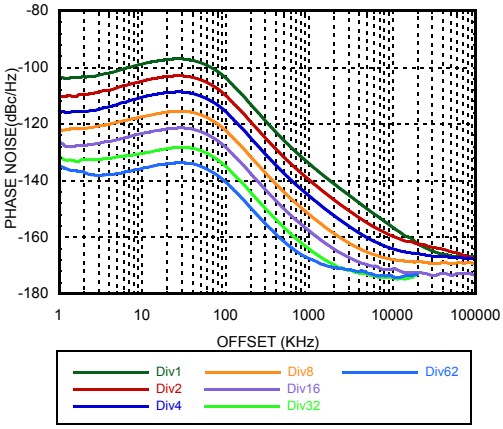
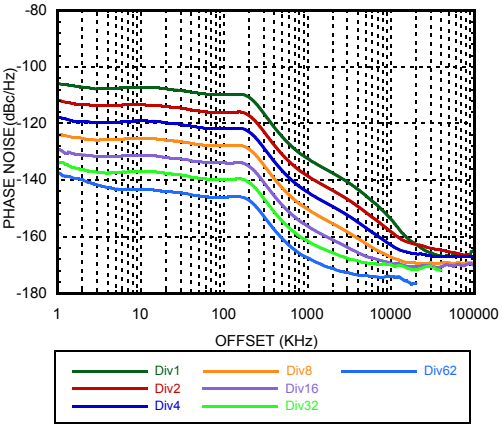


Figure 53. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise at 3300 MHz with various divider ratios [2]



[1] Using 122.88 MHz clock input, 61.44 MHz PFD, 2.5 mA CP, 174 µA Leakage.

[2] Using 100 MHz clock input, 50MHz PFD, 2.5 mA CP, 174 µA Leakage

Figure 54. Auxiliary LO Output, Open Loop Phase Noise vs. Frequency

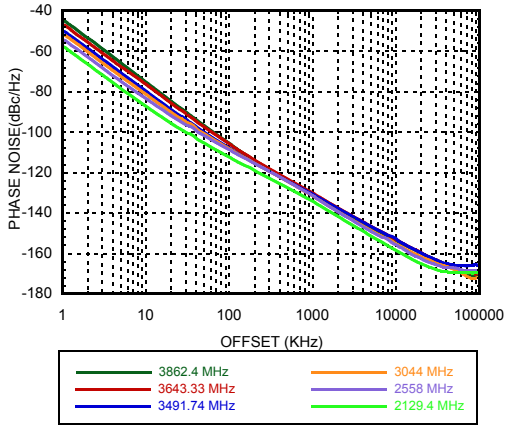


Figure 55. Auxiliary LO Output, Open Loop Phase Noise vs. Temperature

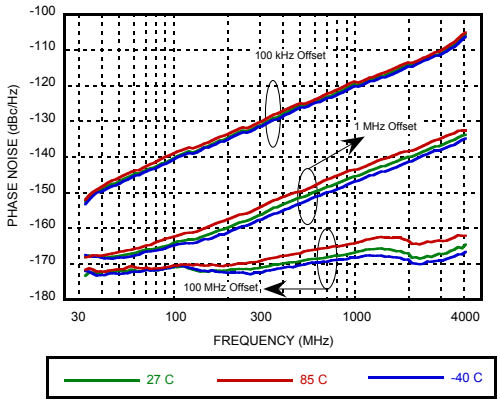


Figure 56. Auxiliary LO Output Power vs. Temperature [1]

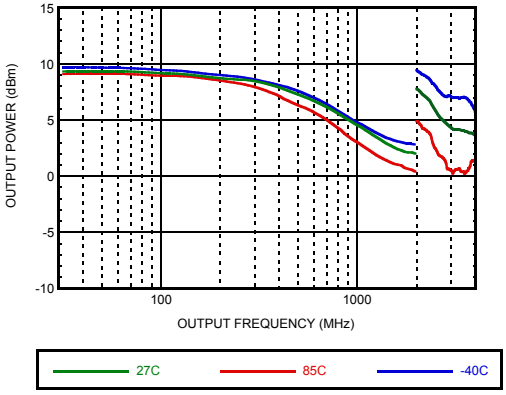


Figure 57. Integrated RMS Jitter [2]

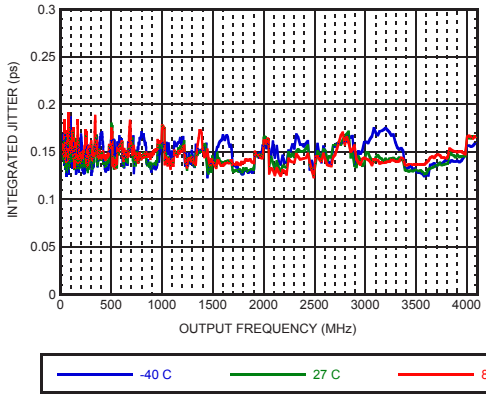


Figure 58. Typical VCO Sensitivity

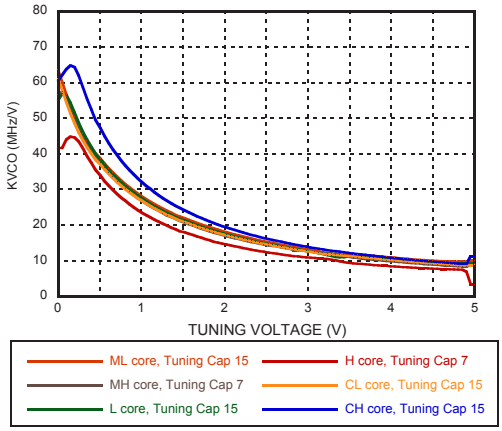
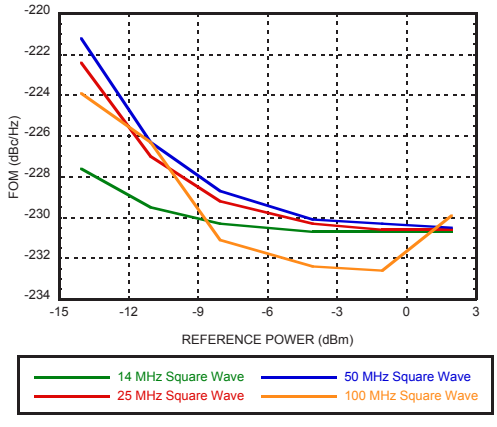


Figure 59. Reference Input Sensitivity, Square Wave, 50 Ω [3]



[1] Both Aux. LO and MOD LO Gain Set to '3' (Max Level), both Aux. LO and MOD LO Buffer Enabled, measured from Auxiliary LO Port.
[2] RMS Jitter data is measured in fractional mode using 50 MHz reference frequency, from 1 kHz to 100 MHz integration bandwidth.
[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

Figure 60. Reference Input Sensitivity, Sinusoid Wave, 50 Ω [1]

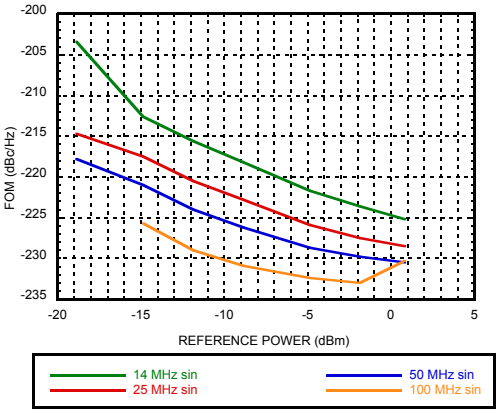


Figure 61. Figure of Merit for PLL/VCO

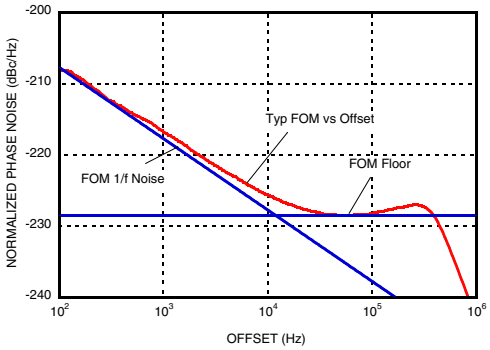


Figure 62. Fractional-N Spurious Performance at 2646.96 MHz Exact Frequency Mode ON [2]

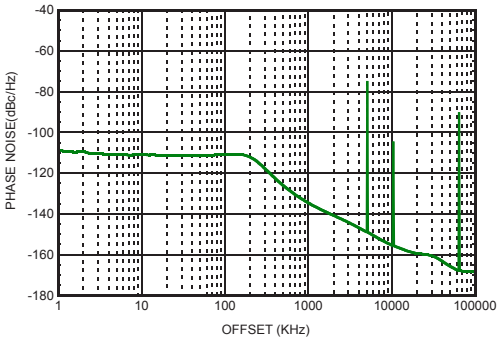


Figure 63. Fractional-N Spurious Performance at 2646.96 MHz Exact Frequency Mode OFF [2]

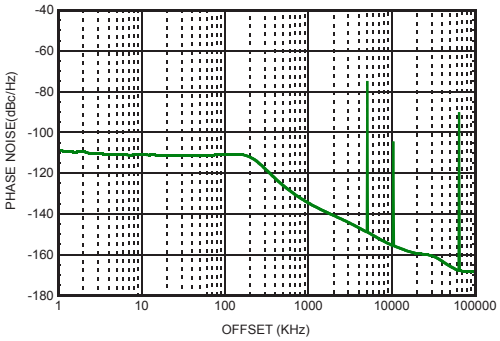


Figure 64. Forward Transmission Gain [3]

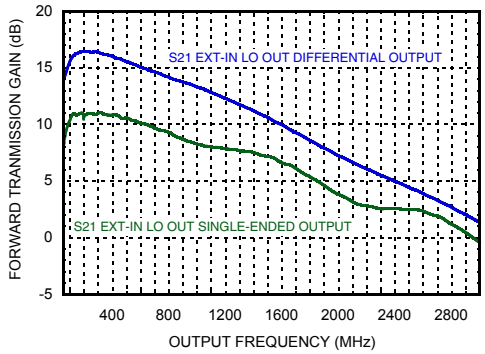
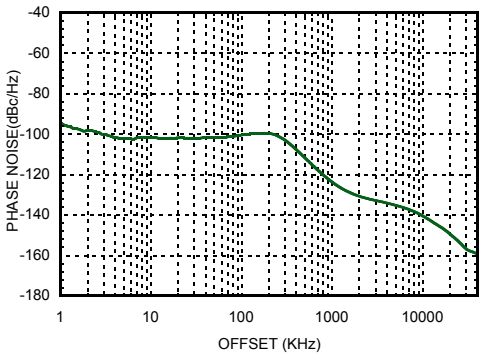


Figure 65. Closed Loop Phase Noise With External VCO HMC384LP4E at 2200 MHz



[1] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[2] 122.88 MHz clock input, PFD = 61.44 MHz, Channel Spacing = 240 kHz.

[3] S21 from Ext_VCO (pin 43, 44) in and LO (pin32, 33) out.

Figure 66. Auxiliary LO Differential Output Return Loss

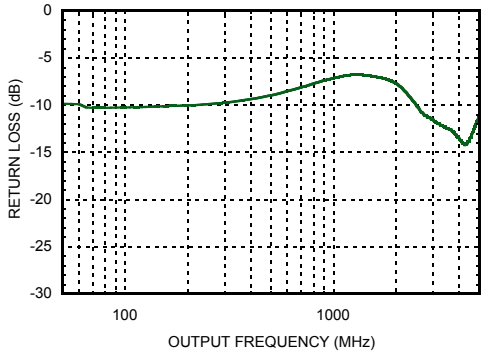


Figure 67. Auxiliary LO Single Ended Output Return Loss

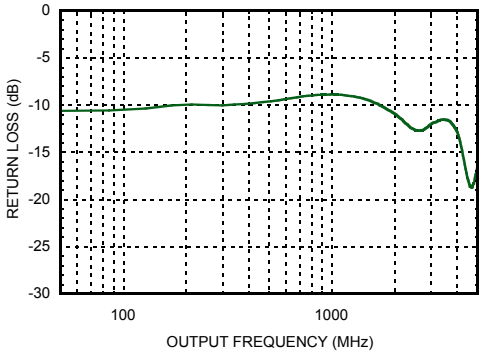


Table 5. Loop Filter Configuration

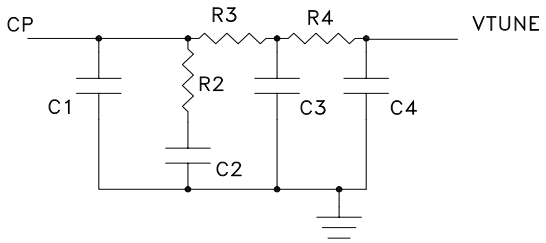
Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
156	180	6.8	47	47	2.2	1	1	

Table 6. Harmonics of LO

	nLO Spur at RF Port			
LO Frequency (GHz)	1	2	3	4
0.7	-65	-45	-67	-63
1.1	-80	-55	-64	-67
1.5	-59	-58	-65	-62
1.9	-59	-54	-72	-64
2.3	-60	-59	-73	-63
2.7	-59	-58	-82	-55
3.1	-60	-58	-77	-48
3.5	-53	-63	-73	-48

LO = Maximum level
All values in dBm measured at RF port.

Table 7. MxN Spurious at IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	-44	-52	-52	-55
1	-49	0	-44	-17	-52
2	-87	-45	-72	-50	-80
3	-88	-62	-88	-71	-87
4	-85	-85	-88	-88	-87

RF Frequency = 0.9 GHz at-5 dBm
LO Frequency = 0.8 GHz at maximum level
All values in dBc below IF power level (1RF - 1LO).

Table 8. MxN Spurious at IF Port

	nLO				
mRF	0	1	2	3	4
0	xxx	-44	-49	-64	-49
1	-54	0	-43	-28	-65
2	-83	-49	-76	-57	-84
3	-87	-72	-86	-88	-85
4	-83	-83	-85	-85	-87

RF Frequency = 1.9 GHz at-5 dBm
LO Frequency = 1.8 GHz at maximum level
All values in dBc below IF power level (1RF - 1LO).

Table 9. MxN Spurious at IF Port

	nLO				
mRF	0	1	2	3	4
0	xxx	-44	-47	-65	-53
1	-58	0	-46	-40	-68
2	-80	-60	-75	-67	-85
3	-82	-82	-86	-83	-85
4	-84	-82	-85	-85	-87

RF Frequency = 2.5 GHz at -5 dBm
LO Frequency = 2.4 GHz at maximum level
All values in dBc below IF power level (1RF - 1LO).

Table 10. Truth Table [1]

CHIPEN (V)	PLL/VCO
LOW	OFF
HIGH	ON

[1] IF and LO amplifiers can be disabled through SPI bus. See `Enabling/Disabling Mixer Features` application section.

Absolute Maximum Ratings

RF Input Power (VBIASIF1,2= 5V, LOVDD=3.3V)	20 dBm
VBIASIF1,2, LOVDD	6V
VGATE1,2, VDDCP, VCS1, VCS2, LOVDD	-0.3V to 5.5V
3VRVDD, DVDD3V	-0.3V to 3.6V
Max. Channel Temperature	150°C
Thermal Resistance (channel to ground paddle)	3.3°C/W
Storage Temperature	-65°C to 150°C
Operating Temperature	-40°C to 85°C
ESD Sensitivity (HBM)	Class 1B
ESD Sensitivity (FICDM)	Class IV

Recommended Operating Conditions

VDDCP, VCS1, VCS2, VBIASIF1, VBIASIF2,LOBIAS1,LOBIAS2,VCC1,VCC2,VGATE1,VGATE2,VDDLS	5 V
LOVDD, 3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF	3.3 V
Operating Temperature	-40°C to +85°C

Outline Drawing

NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: NiPdAu.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

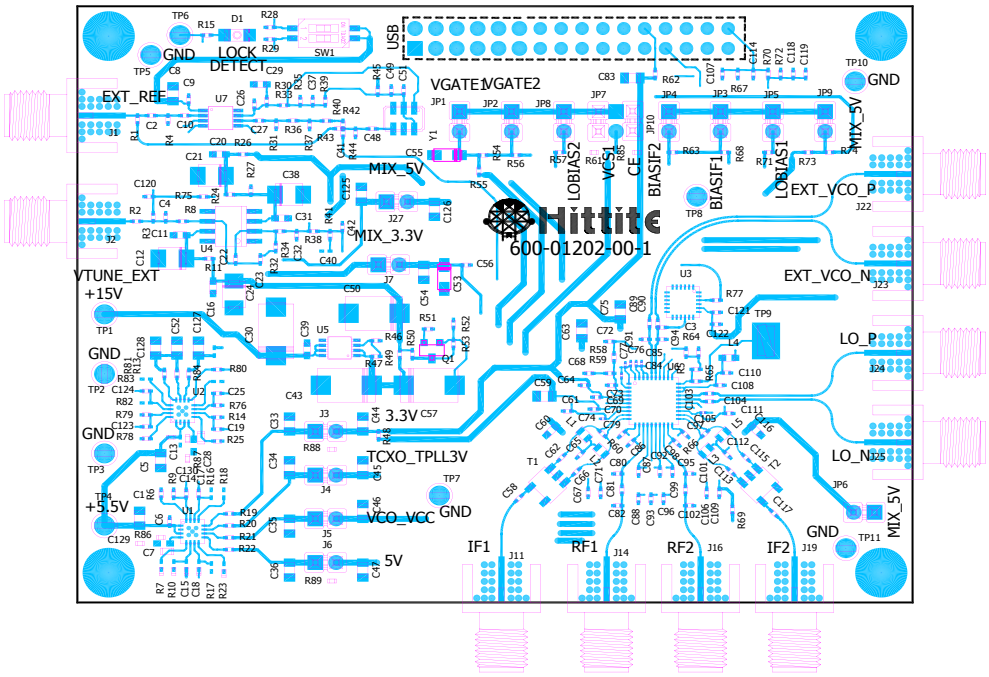
Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC1190ALP6NE	RoHS-compliant Low Stress Injection Molded Plastic	NiPdAu	MSL3	H1190A XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description
1	VDDCP	Power Supply for Charge Pump Analog Section.
2	BIAS	External Bypass Decoupling for Precision Bias Circuits.
3,4	CP1,CP2	Charge Pump Outputs.
5	3VRVDD	Reference supply, 3.3 V nominal.
6	XREFP	Reference Input. The DC bias is generated internally. Normally, it is AC coupled externally.
7	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry, 3.3 V nominal.
8,23	VCS1, VCS2	Bias Control for IF Amplifiers. Connect these pins to a 5V supply through 590 Ohms resistors. Refer to application section for proper values of resistors to adjust IF amplifier current.
9	IF1N	Differential IF outputs. Connect these pins to a 5V supply through choke inductors. See the evaluation board schematic available on the HMC1190A product page.
10	IF1P	
21	IF2P	
22	IF2N	
11, 20	VBIASIF1, VBIASIF2	Supply voltage pin for IF amplifier's bias circuits. Connect to 5V supply through filtering.
12, 19	VGATE1, VGATE2	Bias pins for mixer cores. Set from 4.8V to 5V for operating frequency band.
13, 18	RF1, RF2	RF Input Pins of the Mixer. These pins are internally matched to 50 Ohms. RF input pins require off chip DC blocking capacitors. See the evaluation board schematic available on the HMC1190A product page.
14, 17	LOBIAS2, LOBIAS1	Bias control pins for Local Oscillator Amplifiers. Connect these pins to a 5V supply through 270 Ohms resistors. Refer to application section for proper values of resistors to adjust LO amplifier current.
15,24	RSV	Reserved. These pins are reserved for internal use; leave them floating.
16	LOVDD	3.3V Bias Supply for LO Drive Stages. Refer to application circuit for appropriate filtering and bias generation information.
25	CHIP_EN	Chip Enable. Connect to logic high for normal operation.
26	LO_N	Negative Local Oscillator output. This pin is used for single-ended, differential, or dual output mode.
27	LO_P	Positive Local Oscillator output. This pin is used for differential or dual output mode only. Whereas it can drive a separate load from LO_N, it cannot be used when LO_N is disabled.
28	VCC1	VCO Analog Supply1, 5V nominal.
29	VCC2	VCO Analog Supply 2, 5V nominal.
30	VTUNE	VCO Varactor. VTUNE is the tuning port input.
31	SEN	PLL Serial Port Enable (CMOS) Logic Input.
32	SDI	PLL Serial Port Data (CMOS) Logic Input.
33	SCK	PLL Serial Port Clock (CMOS) Logic Input.
34	LD/SDO	Lock Detect/Serial Data or General Purpose (CMOS) Logic Output (GPO). This is a multifunction pin.
35	EXT_VCO_N	External VCO negative input
36	EXT_VCO_P	External VCO positive input.
37	VCCHF	Analog supply, 3.3 V nominal
38	VCCPS	Analog supply, Prescaler, 3.3 V nominal
39	VCCPD	Analog supply, Phase Detector, 3.3 V nominal
40	VDDLS	Analog supply, Charge Pump, 5 V nominal

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. All evaluation board related drawings are available under Evaluation Kits tab of product page www.analog.com/HMC1190A

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1190ALP6NE Evaluation PCB	EV1HMC1190ALP6N [1]
Evaluation Kit	HMC1190ALP6NE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable	EK1HMC1190ALP6N [2]

[1] Reference this number when ordering Evaluation PCB Only
[2] Reference this number when ordering an HMC1190ALP6NE Evaluation KIt

1.0 Theory of Operation

The block diagram of HMC1190ALP6NE PLL with Integrated VCO is shown in Figure 66

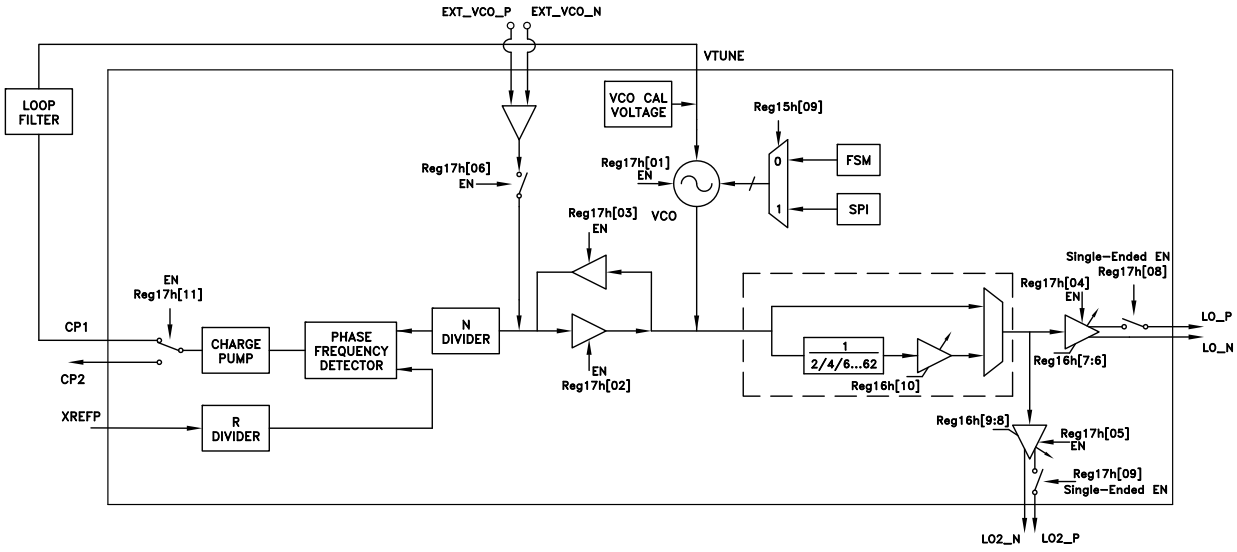


Figure 66. HMC1190ALP6NE PLL VCO Block Diagram

1.1 VCO Overview

The VCO consists of a capacitor switched step tuned VCO and an output stage. In typical operation, the VCO is programmed with the appropriate capacitor switch setting which is executed automatically by the PLL AutoCal state machine if AutoCal is enabled (Reg 0Ah[11] = 0, see section VCO Calibration for more information). The VCO tunes to the fundamental frequency (2050 MHz to 4100 MHz), and is locked by the CP output from the PLL subsystem. The VCO controls the output stage of the HMC1190ALP6NE enabling configuration of:

- VCO Output divider settings configured in Reg 16h (divide by 2/4/6...60/62 to generate frequencies from 33 MHz to 2050 MHz, or divide by 1 to generate fundamental frequencies between 2050 MHz and 4100 MHz)
- Output gain settings (Reg 16h[7:6], Reg 16h[9:8])
- Single-ended or differential output operation (Reg 17h[9:8])
- Always Mute (Reg 16h[5:0])
- Mute when unlock (Reg 17h[7])

1.1.1 VCO Calibration

1.1.1.1 VCO Auto-Calibration (AutoCal)

The HMC1190ALP6NE uses a step tuned type VCO. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or 'stepped' by switching in/out VCO tank capacitors. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the HMC1190ALP6NE's charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (kvco).

The VCO switches are normally controlled automatically by the HMC1190ALP6NE using the Auto-Calibration feature. The Auto-Calibration feature is implemented in the internal state machine. It manages the selection of the VCO sub-band (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via register Reg 15h for testing or for other special purpose operation.

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC1190ALP6NE knows which switch position on the VCO is optimum for the desired output frequency. The HMC1190ALP6NE supports Auto-Calibration (AutoCal) of the step tuned VCO. The AutoCal fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 67.Note how the tuning voltage stays in a narrow range over a wide range of output frequencies such as fast frequency hopping.

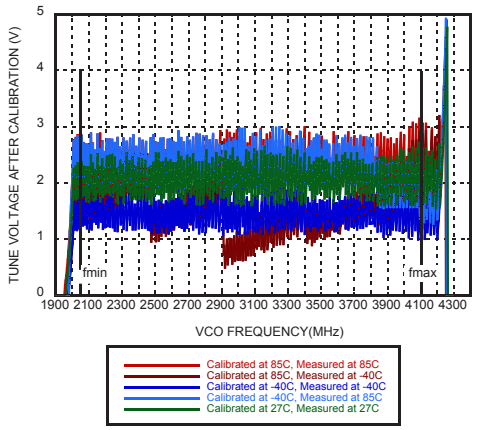


Figure 67.Typical VCO Tuning Voltage After Calibration

The calibration is normally run automatically once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally have to be concerned about which switch setting is used for a given frequency as this is handled by the AutoCal routine. The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration

routine searches for the best step setting that locks the VCO at the current programmed frequency, and ensures that the VCO will stay locked and perform well over it's full temperature range without additional calibration, regardless of the temperature that the VCO was calibrated at.

Auto-Calibration can also be disabled allowing manual VCO tuning. Refer to section Manual VCO Calibration for Fast Frequency Hopping for a description of manual tuning.

1.1.1.1.1 Auto-reLock on Lock Detect Failure

It is possible by setting Reg 0Ah[17] to have the VCO subsystem automatically re-run the calibration routine and re-lock itself if Lock Detect indicates an unlocked condition for any reason. With this option the system will attempt to re-Lock only once.

1.1.1.1.2 VCO AutoCal on Frequency Change

Assuming Reg 0Ah[11]=*0*, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the AutoCal routine for any reason, at the same frequency, simply rewrite the frequency change with the same value and the AutoCal routine will execute again without changing final frequency.

1.1.1.1.3 VCO AutoCal Time & Accuracy

The VCO frequency is counted for T_{mmt}, the period of a single AutoCal measurement cycle.

$$T_{mmt} = T_{xtal} \cdot R \cdot 2^n \quad \text{(EQ 1)}$$

n — is set by Reg 0Ah[2:0] and results in measurement periods which are multiples of the PD period, $T_{xtal}R$.

R — is the reference path division ratio currently in use, Reg 02h

T_{xtal} — is the period of the external reference (crystal) oscillator.

The VCO AutoCal counter will, on average, expect to register N counts, rounded down (floor) to the nearest integer, every PD cycle.

N — is the ratio of the target VCO frequency, f_{vco}, to the frequency of the PD, f_{pd}, where N can be any rational number supported by the N divider.

N is set by the integer (N_{int} = Reg 03h) and fractional (N_{frac} = Reg 04h) register contents

$$N = N_{int} + N_{frac} / 2^{24} \quad \text{(EQ 2)}$$

The AutoCal state machine runs at the rate of the FSM clock, T_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$T_{FSM} = T_{xtal} \cdot 2^m \quad \text{(EQ 3)}$$

m — is 0, 2, 4 or 5 as determined by Reg 0Ah[14:13]

The expected number of VCO counts, V, is given by

$$V = floor\ (N \cdot 2^n) \quad \text{(EQ 4)}$$

The nominal VCO frequency measured, f_{vcom}, is given by

$$f_{vcom} = V \cdot f_{xtal} / (2^n \cdot R) \quad \text{(EQ 5)}$$

where the worst case measurement error, f_{err} , is:

$$f_{err} \approx \pm f_{pd} / 2^{n+1} \quad \text{(EQ 6)}$$

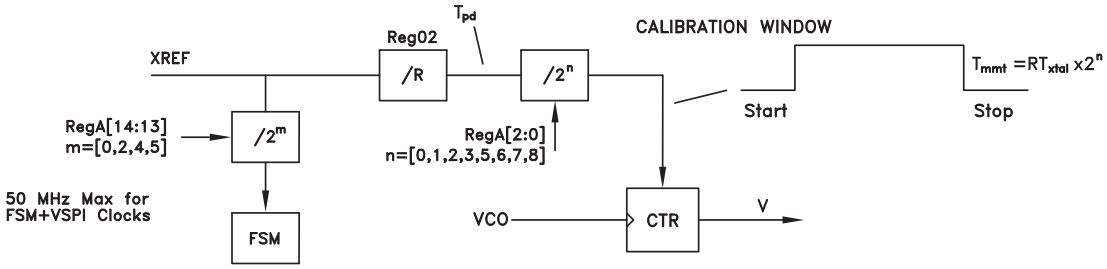


Figure 68. VCO Calibration

A 5-bit step tuned VCO, for example, nominally requires 5 measurements for calibration, worst case 6 measurements, and hence 7 VSPI data transfers of 20 clock cycles each. Total calibration time, worst case, is given by:

$$T_{cal} = k128T_{FSM} + 6T_{PD}\,2^{n} + 7 \cdot 20T_{FSM} \quad \text{(EQ 7)}$$

or equivalently

$$T_{cal} = T_{xtal}\,(6R \cdot 2^{n} + (140+(3 \cdot 128)) \cdot 2^{m}) \quad \text{(EQ 8)}$$

For guaranteed hold of lock, across temperature extremes, the resolution should be better than 1/8th the frequency step caused by a VCO sub-band switch change. Better resolution settings will show no improvement.

1.1.1.1.4 VCO AutoCal Example

The HMC1190ALP6NE must satisfy the maximum f_{pd} limited by the two following conditions:

a. N ≥ 16 (f_{int}), N ≥ 20.0 (f_{frac}), where N = f_{VCO} / f_{pd}

b. f_{pd} ≤ 100 MHz

Suppose the HMC1190ALP6NE output frequency is to operate at 2.01 GHz. Our example crystal frequency is f_{xtal} = *50 MHz, R=1, and m=0 (*Figure 68*)*, hence T_{FSM} = 20 ns (50 MHz). Note, when using AutoCal, the maximum AutoCal Finite State Machine (FSM) clock cannot exceed 50 MHz (see Reg 0Ah[14:13]). The FSM clock does not affect the accuracy of the measurement, it only affects the time to produce the result. This same clock is used to clock the 16 bit VCO serial port.

If time to change frequencies is not a concern, then one may set the calibration time for maximum accuracy, and therefore not be concerned with measurement resolution.

Using an input crystal of 50 MHz (R=1 and f_{pd}=50 MHz) the times and accuracies for calibration using EQ 6 and EQ 8 are shown in Table 11 Where minimal tuning time is 1/8th of the VCO band spacing.

Across all VCOs, a measurement resolution better than 800 kHz will produce correct results. Setting m = 0, n = 5, provides 781 kHz of resolution and adds 8.6 µs of AutoCal time to a normal frequency hop. Once the AutoCal sets the final switch value, 8.64 µs after the frequency change command, the fractional register will be loaded, and the loop will lock with a normal transient predicted by the loop dynamics. Hence as shown in this example that AutoCal typically adds about 8.6 µs to the normal time to achieve frequency lock. Hence, AutoCal should be used for all but the most extreme frequency hopping requirements.