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HMC1190LP6GE

v06.1113

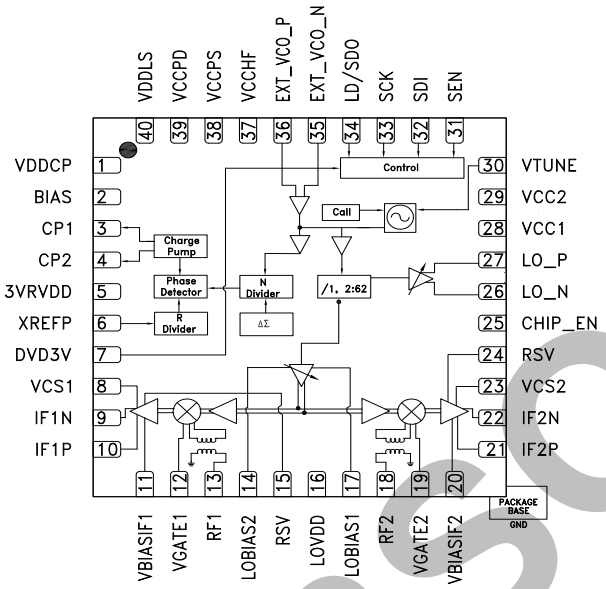
BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

Typical Applications

The HMC1190LP6GE is Ideal for:

- Multiband/Multi-standard Cellular BTS Diversity Receivers
- GSM & 3G & LTE/WiMAX/4G
- MIMO Infrastructure Receivers
- Wideband Radio Receivers
- Multiband Basestations & Repeaters

Functional Diagram



Features

Broadband Operation with no external matching

High-side and Low-side LO injection Operation

High Input IP3 of +24 dBm

Power Conversion Gain of 8.9 dB

Input P1dB of 11 dBm

SSB Noise Figure of 9 dB

55 dBc Channel-to-Channel Isolation

Enable/Disable Mixer and PLLVCO independently

Single-ended RF input ports

Maximum Phase Detector Rate: 100 MHz

Low Phase Noise: -110 dBc/Hz in Band Typical

PLL FOM:

-230 dBc/Hz Integer Mode, -227 dBc/Hz Fractional Mode

< 180 fs Integrated RMS Jitter (1 kHz to 20 MHz)

LO Low Noise Floor: -165 dBc/Hz

Mixer Low Noise Floor: -161 dBc/Hz

Integrated VCO

External VCO Input, differential LO output

Exact Frequency Mode:
0 Hz Fractional Frequency Error

Programmable RF Output Phase

Output Phase Synchronous Frequency Changes

Output Phase Synchronization

LO Output Mute Function

Compact Solution, 6x6 mm Leadless QFN Package

General Description

The HMC1190LP6GE is a high linearity broadband dual channel downconverting mixer with integrated PLL and VCO optimized for multi-standard receiver applications that require a compact, low power design. Integrated wideband limiting LO amplifiers enable the HMC1190LP6GE to achieve an unprecedented RF bandwidth of 700 MHz to 3500 MHz for applications including Cellular/3G, LTE/WiMAX/4G. Unlike conventional narrow-band downconverters, the HMC1190LP6GE supports both high-side and low-side LO injection over all RF frequencies. The RF and LO input ports are internally matched to 50 Ohms.

The HMC1190LP6GE features an integrated LO and RF baluns, enable control of IF and LO amplifiers and bias control interface to high linearity passive mixer cores. Balanced passive mixer combined with high-linearity IF amplifier architecture provides excellent LO-to-RF, LO-to-IF, and RF-to-IF isolations. Low noise figure of 9 dB, and high IIP3 of +24 dBm allow the HMC1190LP6GE to be used in most demanding applications. External bias control pins enable optimization of already low power dissipation of 2.34 W (typical). Fast enable control interface reduces power consumption further in TDD applications.

External VCO input allows the HMC1190LP6GE to lock external VCOs, and enables cascaded LO architectures for MIMO applications. Two separate Charge Pump (CP) outputs enable separate loop filters optimized for both integrated and external VCOs, and seamless switching between integrated or external VCOs during operation. Programmable RF output phase features can further phase adjust and synchronize multiple HMC1190LP6GE's enabling scalable MIMO and beam-forming radio architectures.

Additional features include configurable LO output mute function, Exact Frequency Mode that enables the HMC1190LP6GE to generate fractional frequencies with 0 Hz frequency error, and the ability to synchronously change frequencies without changing phase of the output signal that increases efficiency of digital pre-distortion loops. The HMC1190LP6GE is housed in RoHS compliant compact 6x6 mm leadless QFN package.

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Table 1. Electrical Specifications, (Unless Otherwise Specified, the Following Test Conditions Were Used) T_A = +25°C, IF Frequency = 150 MHz, LO Power is set to '3' [1], RF Input Power = -5 dBm (-5 dBm / tone for 2-tone IP3 tests, Δf = 1MHz), LOVDD=3VR-VDD=DVDD3V=CHIPEN= 3V, VDDCP=VCS1=VCS2=VBIASIF1=VBIASIF2=LOBIAS1=LO-BIAS2=VCC1=VCC2=VGATE1=VGATE2=5V, VGATE = 4.8V.

Parameter	Typical				Units
Mixer Core RF Input Frequency Range	700 - 3500				MHz
Mixer Core IF Output Frequency Range	50 - 350				MHz
	RF=900 MHz[2]	RF=1900 MHz[3]	RF=2200 MHz [3]	RF=2700 MHz [3]	
Conversion Gain	9.3 [5]	8.4 [5]	8.1 [5]	7.1 [5]	dB
IP3 (Input)	24.5	24	23.5	23.5	dBm
Noise Figure (SSB)	8.5	9.2	9.5	10	dB
1 dB Compression (Input)	10.7	11.4	11.2	12	dBm
LO leakage @ RF port	-67	-58	-59	-58	dBm
RF to IF Isolation	40	46	45	52	dB
Channel to Channel Isolation [4]	53	49	48	48	dBc
+2RF-2LO Response	68	67	70	72	dBc
+3RF-3LO Response	69	68	74	78	dBc

[1] LO Power Level can be adjusted using Reg 16h.

[2] High Side LO injection, VGATE1,2 = 5V

[3] Low Side LO injection, VGATE1,2 = 4.8V

[4] RF1 input power= -5 dBm, measurement taken from IF2 output. RF2 and IF1 ports are terminated with 50 Ohms.

[5] Balun losses at IF output ports are de-embedded.

Table 2. DC Power Supply Specifications

Parameter		Min.	Typ.	Max.	Units.
5 V Supply Rails (VDDCP, VCS1, VCS2, VDDLS, VBIASIF1, VBIASIF2, LOBIAS1, LOBIAS2, VCC1, VCC2)		+4.8	+5	+5.2	V
			348 [1]		mA
VGATE1, VGATE2		+4.5	+5	+5.2	V
3.3 V Supply Voltage (LOVDD, 3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF)		+3.1	+3.3	+3.5	V
			198		mA
Mixer Core Supply Currents when IF1EN and IF2EN are Enabled	VDDIF (5 V)		160		mA
	VCS1 + VCS2 (5 V)		3.3	4.2	mA
	VBIASIF1 + VBIASIF2 (5 V)		24	28	mA
	VGATE1, VGATE2		8	9.2	mA
	LOBIAS1 + LOBIAS2 (5 V)		4.6	5.6	mA
	LOVDD (3.3 V)		140	148	mA

[1] LO Frequency=2400 MHz, LO_MIX Power and LO_OUT Power set to '3', LO_MIX and LO_OUT is differential and LO_OUT is off. When LO_OUT enabled in differential mode the bias current increases by 34 mA (Typ.)

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Table 2. DC Power Supply Specifications

Parameter		Min.	Typ.	Max.	Units.
PLL/VCO Core Supply Currents when CHIPEN is Enabled	Charge Pump (VDDCP, +5 V) +VCCLS		6		mA
	LO_OUT differential, LO_MIXER off [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 148 58		 mA mA
	LO_OUT single-ended, LO_MIXER off [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 131 58		 mA mA
	LO_OUT off, LO_MIXER differential [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 148 58		 mA mA
	LO_OUT off, LO_MIXER single-ended [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 131 58		 mA mA
	LO_OUT differential, LO_MIXER differential [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 182 58		 mA mA
	LO_OUT single-ended, LO_MIXER single-ended [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 150 58		 mA mA
	VCCPD, VCCPS, VCCHF, DVDD3V, 3VRVDD (+3.3V)		58	64	mA
Mixer Core Supply Currents when IF1EN and IF2EN are Disabled	VDDIF (5V)		0		mA
	VCS1 + VCS2 (5V)		4		mA
	VBIASIF1 + VBIASIF2 (5V)		3.5		mA
	VGATE1 + VGATE2 (5V)		4		mA
	LOBIAS1 + LOBIAS2 (5V)		5.5		mA
	LOVDD (3.3 V)		4		mA
PLL/VCO Core Supply Currents when CHIPEN is Disabled	VDDCP, VCC1, VCC2, VDDLS (5V) [1]		3		mA
	3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF (3.3V) [1]		1		mA

[1] LO Frequency=2400 MHz, LO_MIX and LO_OUT outputs set to maximum gain.

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Table 3. PLL & VCO Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Logic Inputs					
Logic High		1.2			V
Logic Low				0.6	V
Input Current				+/- 1	uA
Input Capacitance			2		pF
LO Output Characteristics					
LO Output Frequency		50		4100	MHz
VCO Frequency at PLL Input		2000		4100	MHz
VCO Fundamental Frequency		2000		4100	MHz
VCO Output Divider					
VCO Output Divider Range	1, 2, 4, ... 60, 62	1		62	
PLL RF Divider Characteristics					
19-Bit N Divider Range	Integer	16		524287	
	Fractional	20		524283	
Phase Detector (PD)					
PD Frequency	Fractional Mode	DC		100	MHz
	Integer Mode	DC		100	MHz
Harmonics					
fo Mode at 4000 MHz	2nd / 3rd / 4th		-30/-22/-32		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,... 62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled	1	2	3.3	Vpp
Ref Input Capacitance				5	pF
14-\Bit R-Divider Range		1		16,383	
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-167		dBc/Hz

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Table 3. PLL & VCO Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
VCO Open Loop Phase Noise at fo @ 3 GHz/2 = 1.5 GHz					
10 kHz Offset			-83		dBc/Hz
100 kHz Offset			-113		dBc/Hz
1 MHz Offset			-139.5		dBc/Hz
10 MHz Offset			-165.5		dBc/Hz
100 MHz Offset			-167		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 3862 MHz	Measured at 2.5 V		15		MHz/V
VCO Tuning Sensitivity at 3643 MHz	Measured at 2.5 V		14.5		MHz/V
VCO Tuning Sensitivity at 3491 MHz	Measured at 2.5 V		16.2		MHz/V
VCO Tuning Sensitivity at 3044 MHz	Measured at 2.5 V		14.6		MHz/V
VCO Tuning Sensitivity at 2558 MHz	Measured at 2.5 V		15.4		MHz/V
VCO Tuning Sensitivity at 2129 MHz	Measured at 2.5 V		14.8		MHz/V
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

Table 4. Enable/Disable Settling Time Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Enable Settling Time	Mixer Core Enabled		140		ns
Disable Settling Time	Mixer Core Disabled		110		ns

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Figure 1. Conversion Gain vs. VGATE [1] [2]

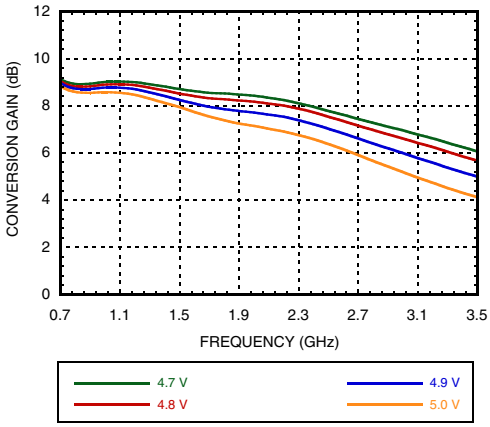


Figure 2. Input IP3 vs. VGATE [1]

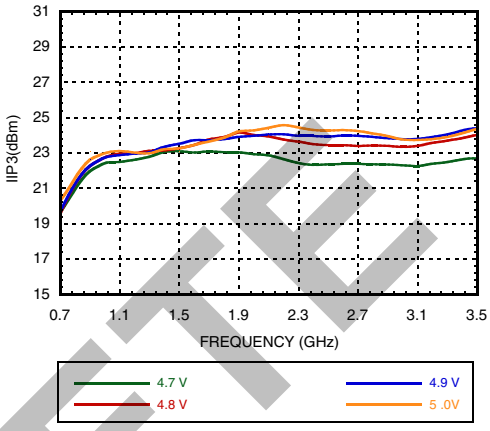


Figure 3. +2RF -2LO Response vs. VGATE[1]

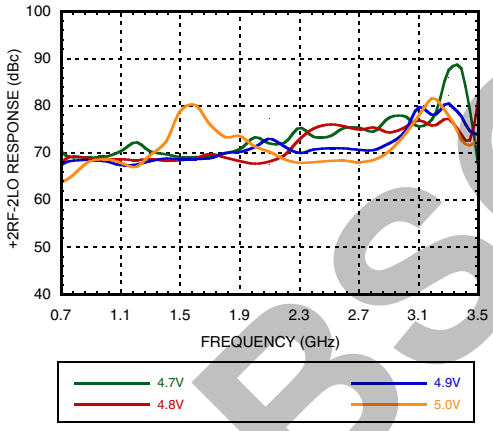


Figure 4. +3RF -3LO Response vs. VGATE[1]

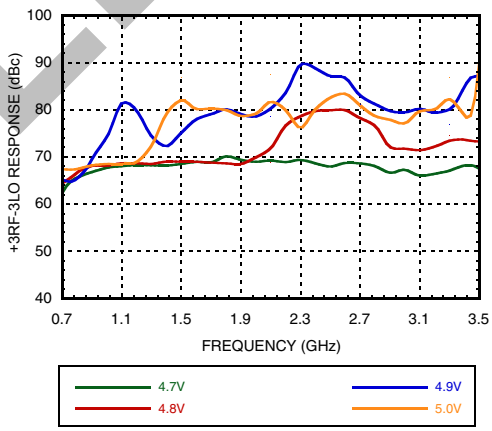
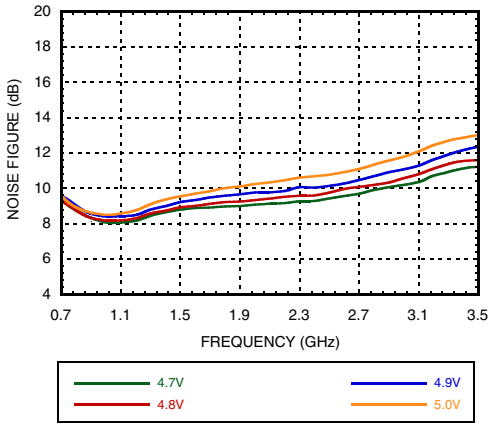


Figure 5. Noise Figure vs. VGATE [1]



[1] VGATE is bias voltage for passive mixer cores (VGATE1 and VGATE2 pins). Refer to pin description table.

[2] Balun losses at IF output ports are de-embedded.

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Figure 6. Conversion Gain vs. High Side LO & Low Side LO @ VGATE=4.8V [1]

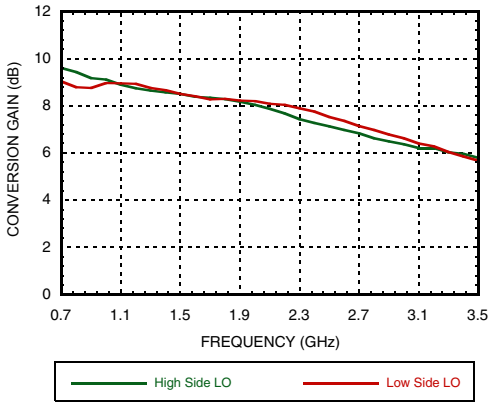


Figure 7. Input IP3 vs. High Side LO & Low Side LO @ VGATE=4.8V

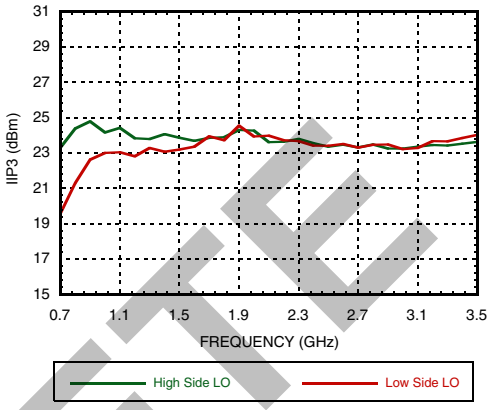


Figure 8. RF/IF Isolation vs. Temperature @ VGATE=4.8V

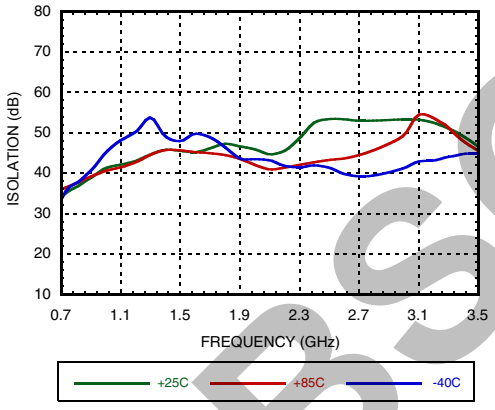


Figure 9. LO Leakage @ VGATE=4.8V

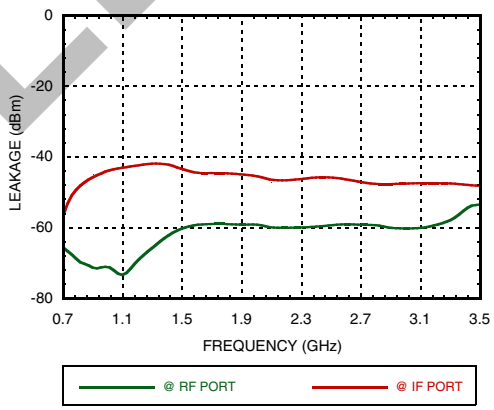


Figure 10. Conversion Gain vs. LO Drive @ VGATE=4.8V [1]

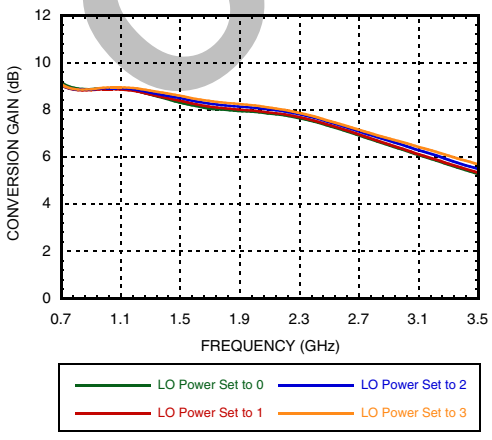
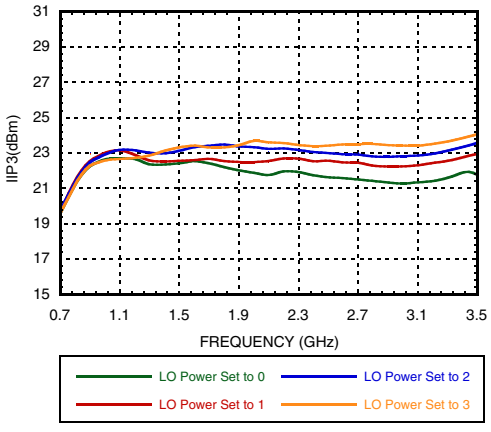


Figure 11. LO Drive @ VGATE=4.8V



[1] Balun losses at IF output ports are de-embedded.

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Figure 12. +2RF -2LO Response vs. LO Drive @ VGATE=4.8V

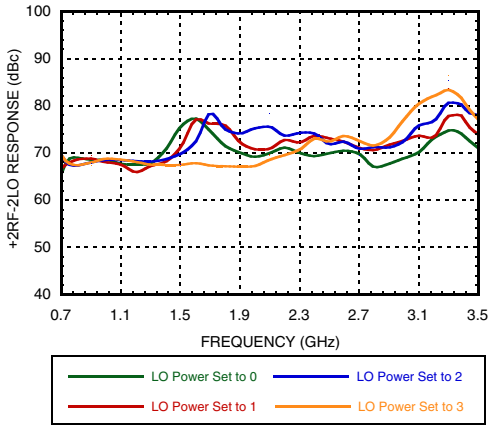


Figure 13. +3RF -3LO Response vs. LO Drive @ VGATE=4.8V

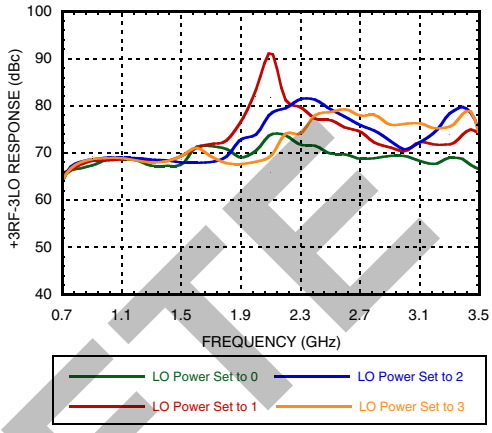


Figure 14. RF Input Return Loss @ VGATE=4.8V [1]

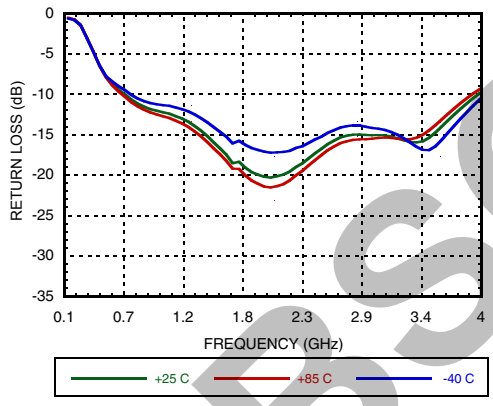


Figure 15. IF Output Return Loss @ VGATE=4.8V [1]

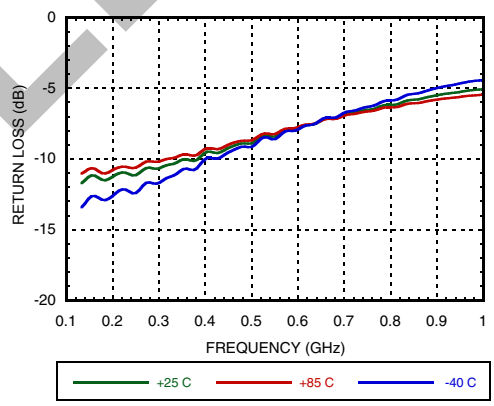
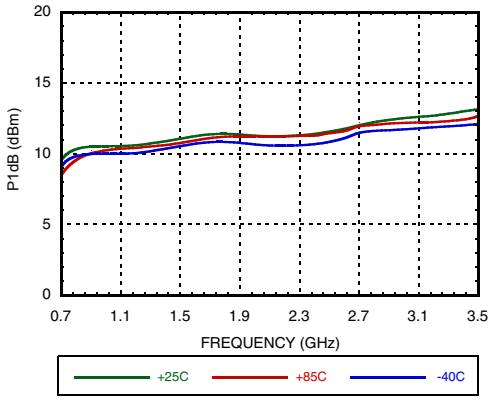


Figure 16. Input P1dB vs. Temperature @ VGATE=4.8V



[1] LO input Frequency = 1700MHz, LO power = 0 dBm.

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Figure 17. Conversion Gain vs. Temperature @ VGATE=5.0V [1]

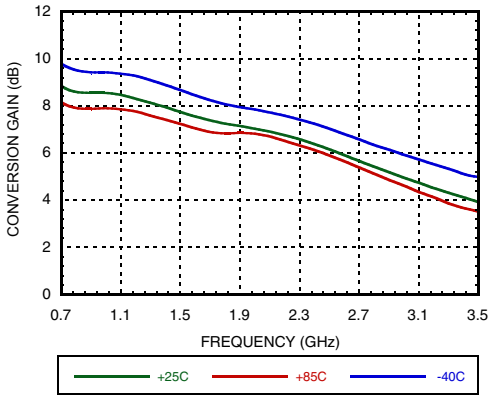


Figure 18. Input IP3 vs. Temperature @ VGATE=5.0V

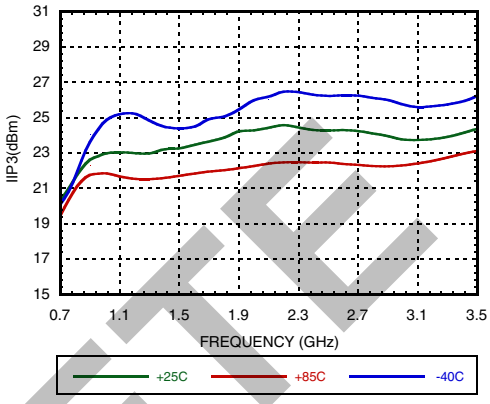


Figure 19. +2RF -2LO Response vs. Temperature @ VGATE=5.0V

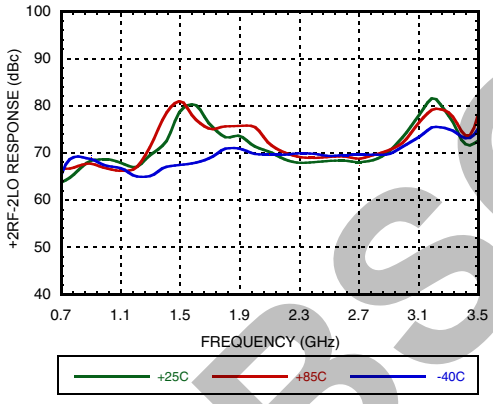


Figure 20. +3RF -3LO Response vs. Temperature @ VGATE=5.0V

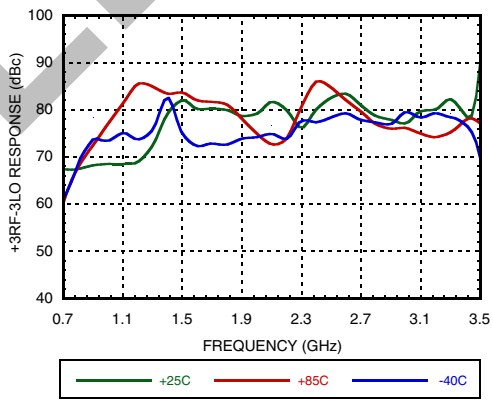
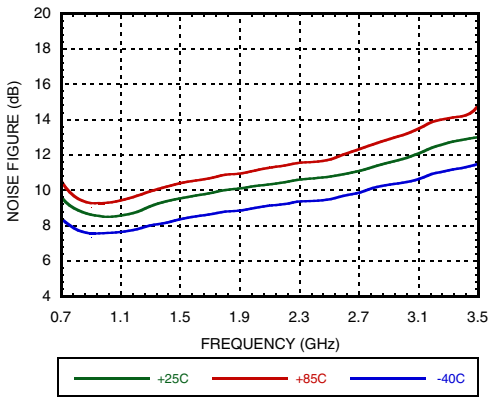


Figure 21. Noise Figure vs. Temperature @ VGATE=5.0V



[1] Balun losses at IF output ports are de-embedded.

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Figure 22. Conversion Gain vs. Temperature @ VGATE=4.9V [1]

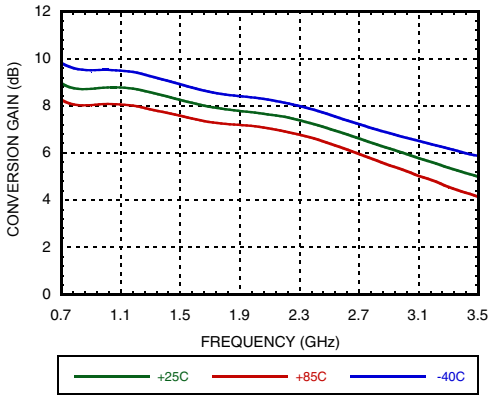


Figure 23. Input IP3 vs. Temperature @ VGATE=4.9V

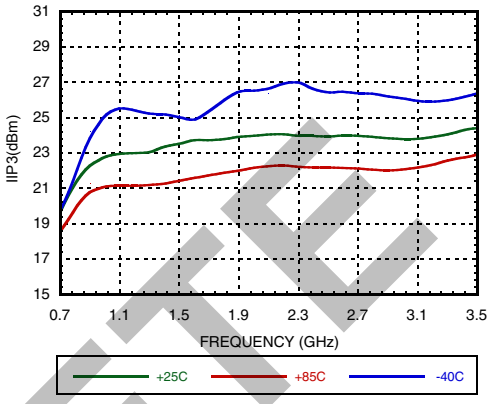


Figure 24. +2RF -2LO Response vs. Temperature @ VGATE=4.9V

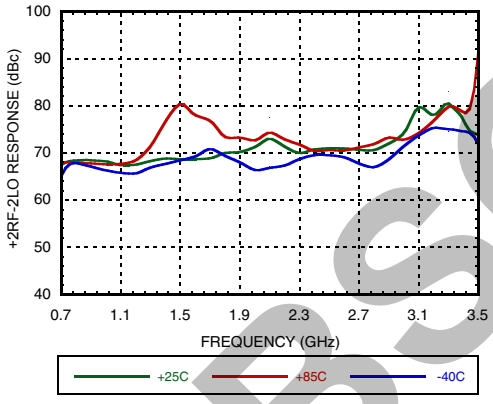


Figure 25. +3RF -3LO Response vs. Temperature @ VGATE=4.9V

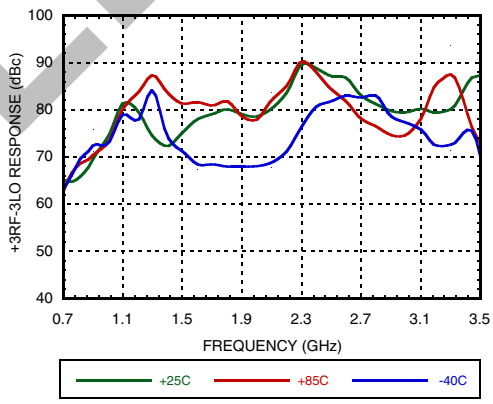
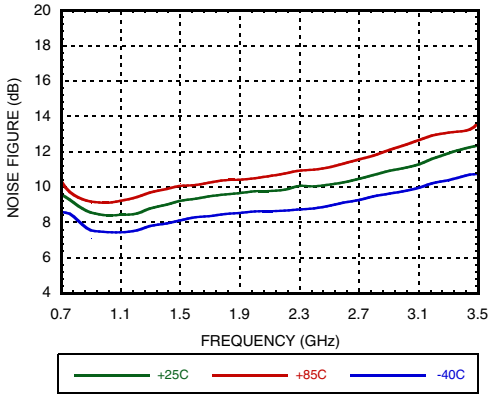


Figure 26. Noise Figure vs. Temperature @ VGATE=4.9V



[1] Balun losses at IF output ports are de-embedded.

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Figure 27. Conversion Gain vs. Temperature @ VGATE=4.8V [1]

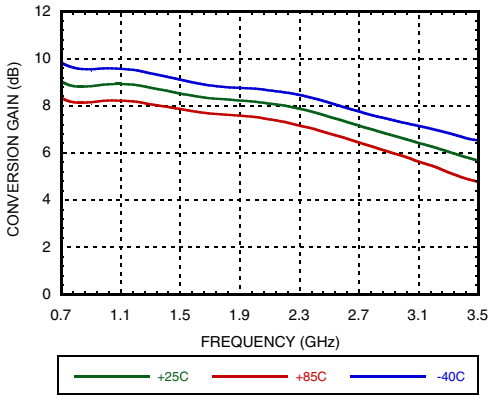


Figure 28. Input IP3 vs. Temperature @ VGATE=4.8V

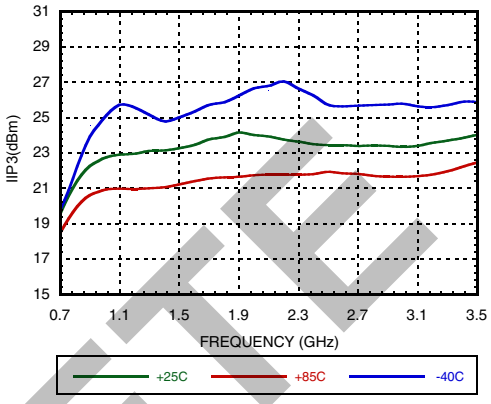


Figure 29. +2RF -2LO Response vs. Temperature @ VGATE=4.8V

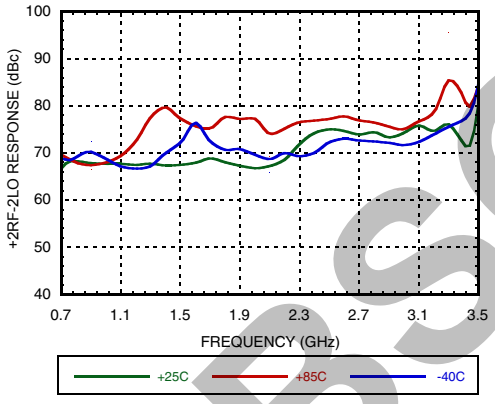


Figure 30. +3RF -3LO Response vs. Temperature @ VGATE=4.8V

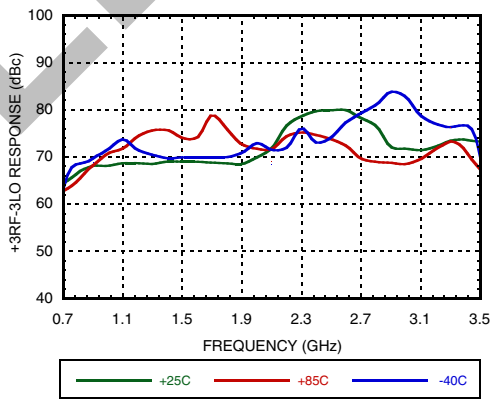
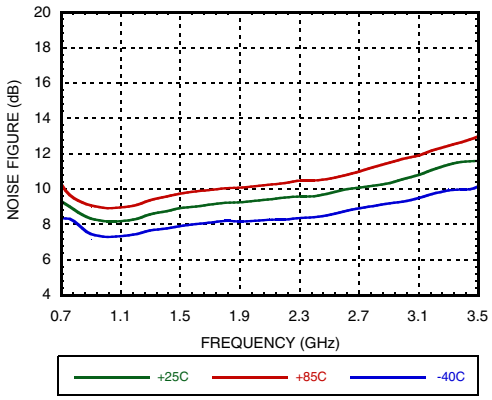


Figure 31. Noise Figure vs. Temperature @ VGATE=4.8V



[1] Balun losses at IF output ports are de-embedded.

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Figure 32. Conversion Gain vs. Temperature @ VGATE=4.7V [1]

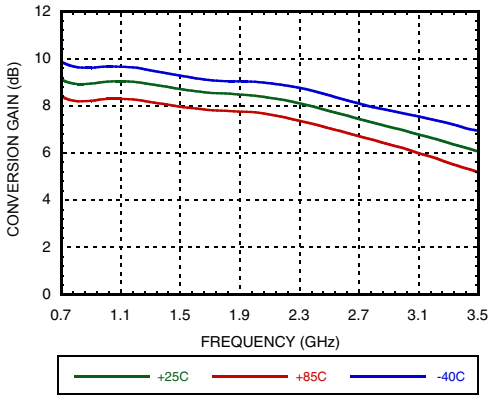


Figure 33. Input IP3 vs. Temperature @ VGATE=4.7V

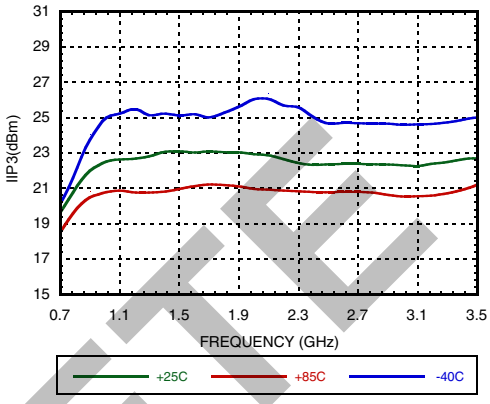


Figure 34. +2RF -2LO Response vs. Temperature @ VGATE=4.7V

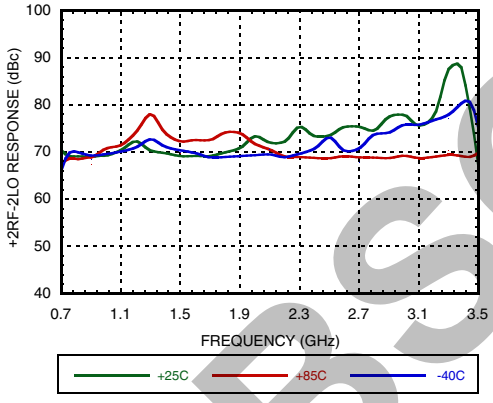


Figure 35. +3RF -3LO Response vs. Temperature @ VGATE=4.7V

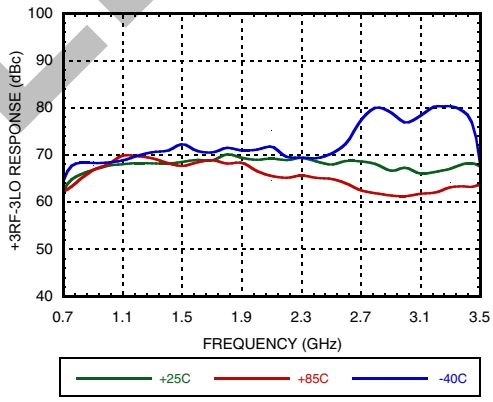
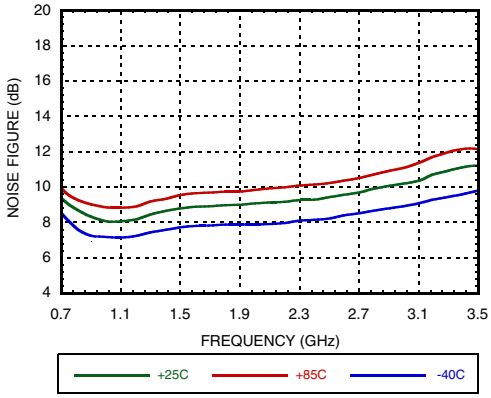


Figure 36. Noise Figure vs. Temperature @ VGATE=4.7V



[1] Balun losses at IF output ports are de-embedded.

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Figure 37. Channel to Channel Isolation vs. VGATE

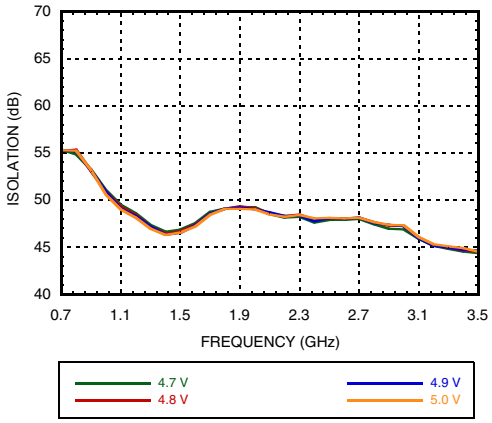


Figure 38. Channel to Channel Isolation vs. IF Frequency

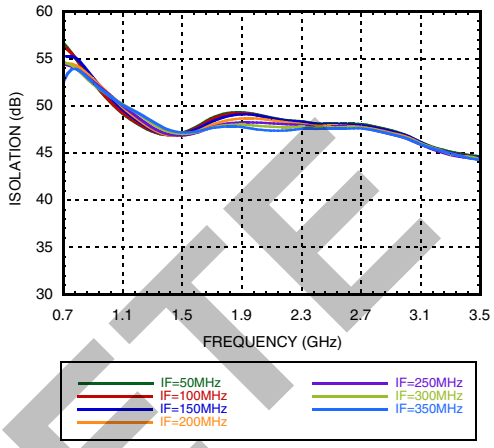


Figure 39. Conversion Gain, Channel Matching @ VGATE=4.8V [1]

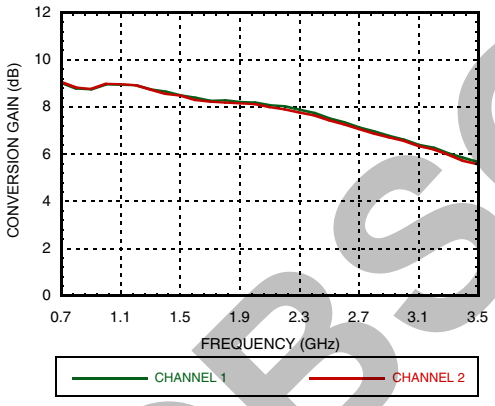


Figure 40. Input IP3, Channel Matching @ VGATE=4.8V

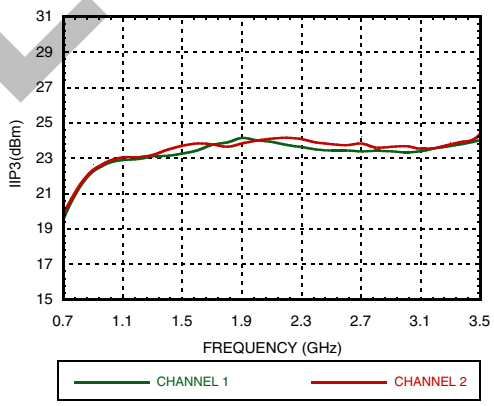


Figure 41. Conversion Gain vs. Vdd @ VGATE=4.8V [1]

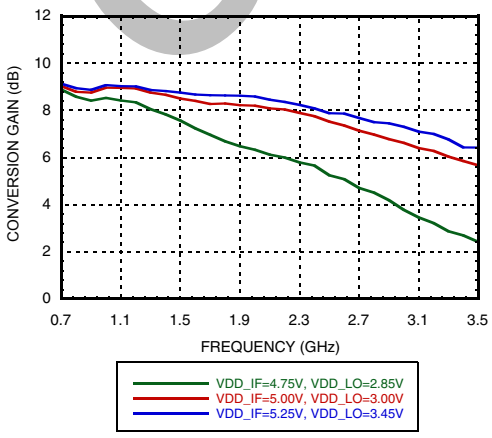
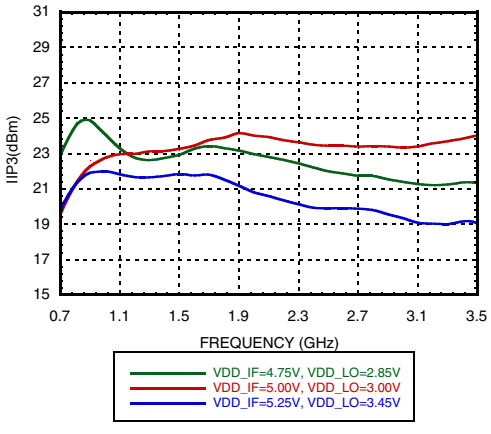


Figure 42. Input IP3 vs. Vdd @ VGATE=4.8V



[1] Balun losses at IF output ports are de-embedded.

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Figure 43. Conversion Gain vs. IF Frequency @ LO=850 MHz, VGATE=4.8V [1]

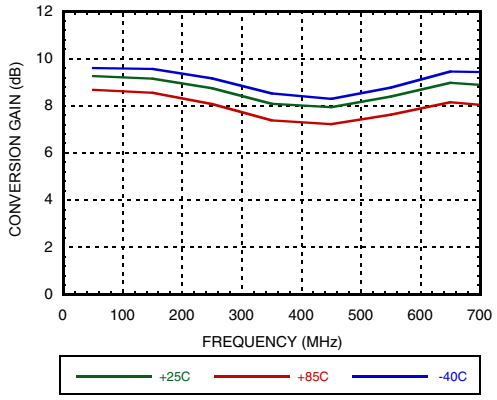


Figure 44. IIP3 vs. IF Frequency @ LO=850 MHz, VGATE=4.8V

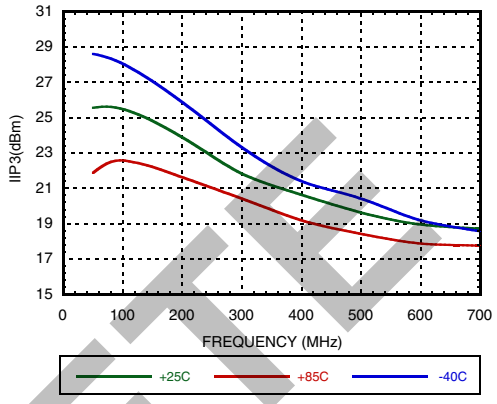


Figure 45. Conversion Gain vs. IF Frequency @ LO=1800 MHz, VGATE=4.8V [1]

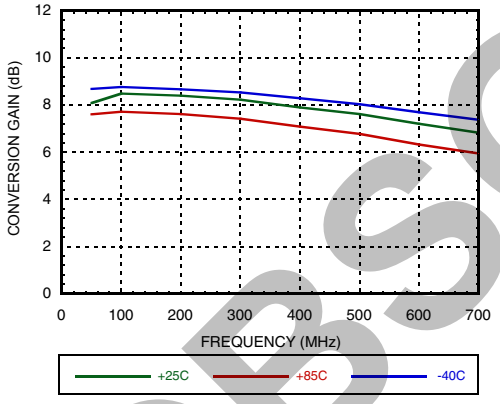
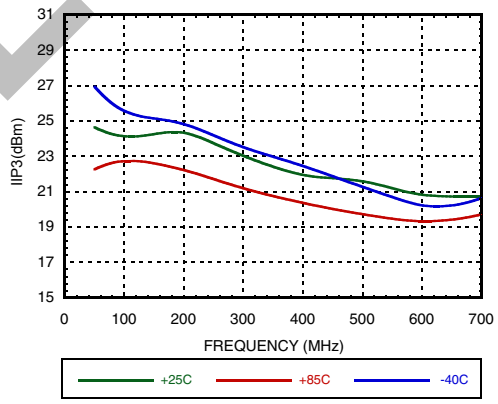


Figure 46. IIP3 vs. IF Frequency @ LO=1800 MHz, VGATE=4.8V



[1] Balun losses at IF output ports are de-embedded.

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Figure 47. Auxiliary LO Output, Open Loop Phase Noise @ 3600 MHz

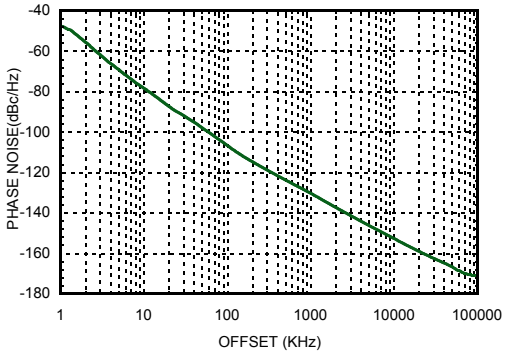


Figure 48. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @3600 MHz with various divider ratios [1]

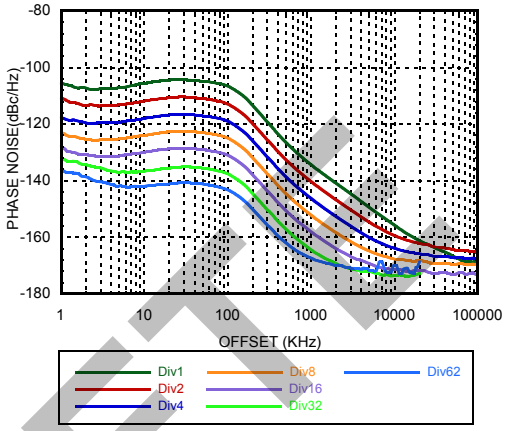


Figure 49. Auxiliary LO Output, Open Loop Phase Noise @ 4100 MHz

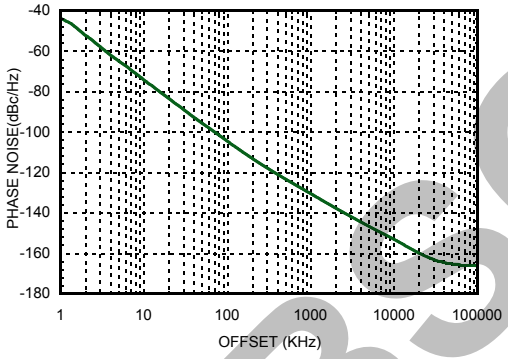


Figure 50. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @4100 MHz with various divider ratios [1]

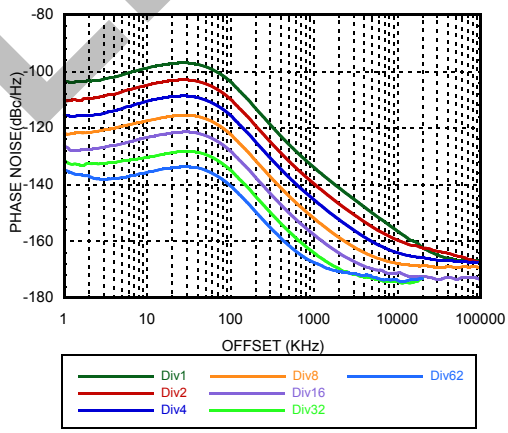
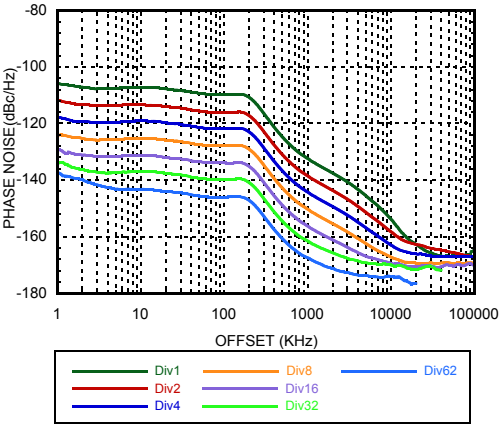


Figure 51. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @ 3300 MHz with various divider ratios [2]



[1] Using 122.88 MHz clock input, 61.44 MHz PFD, 2.5 mA CP, 174 uA Leakage.

[2] Using 100 MHz clock input, 50MHz PFD, 2.5 mA CP, 174 uA Leakage

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Figure 52. Auxiliary LO Output, Open Loop Phase Noise vs. Frequency

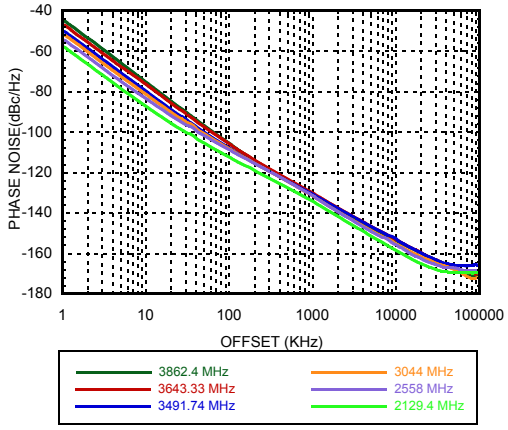


Figure 53. Auxiliary LO Output, Open Loop Phase Noise vs. Temperature

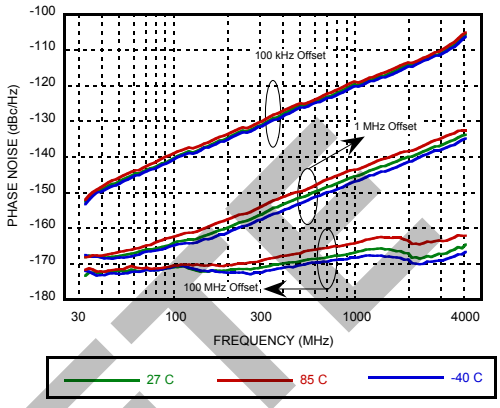


Figure 54. Auxiliary LO Output Power vs Temperature [1]

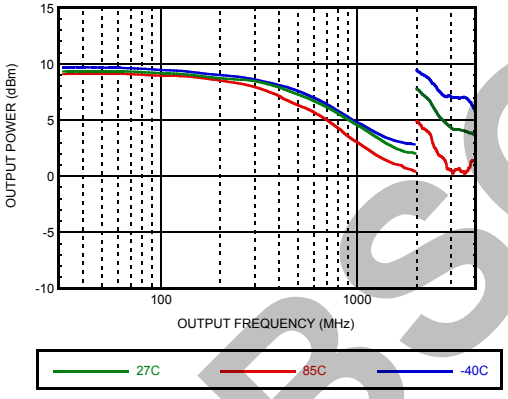


Figure 55. Integrated RMS Jitter [2]

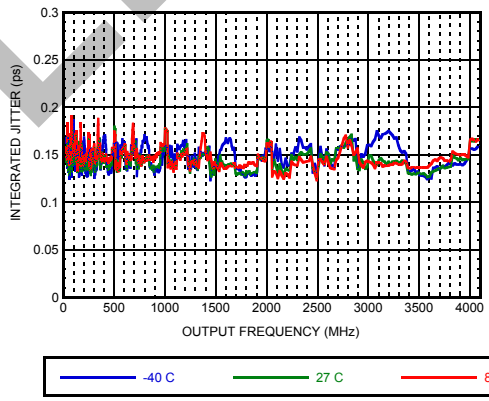


Figure 56. Typical VCO Sensitivity

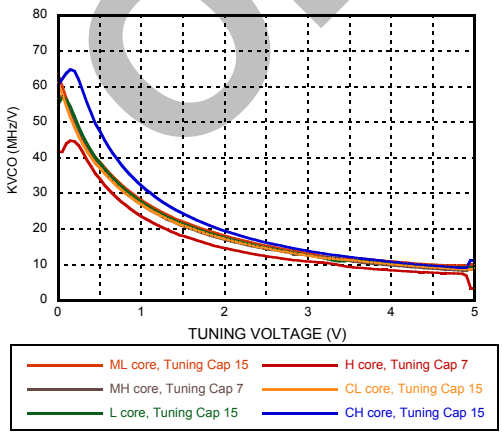
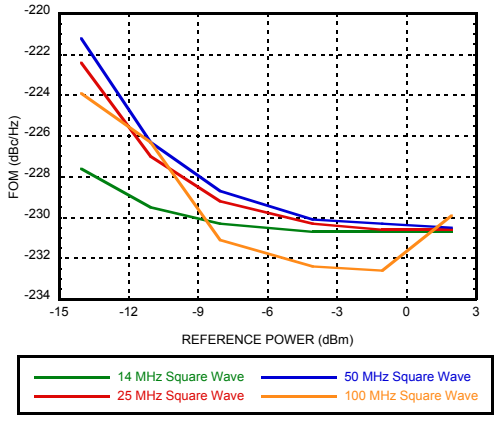


Figure 57. Reference Input Sensitivity, Square Wave, 50 Ω [3]



[1] Both Aux. LO and MOD LO Gain Set to '3' (Max Level), both Aux. LO and MOD LO Buffer Enabled, measured from Auxiliary LO Port.

[2] RMS Jitter data is measured in fractional mode using 50 MHz reference frequency, from 1 kHz to 100 MHz integration bandwidth.

[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

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Figure 58. Reference Input Sensitivity, Sinusoid Wave, 50 Ω [1]

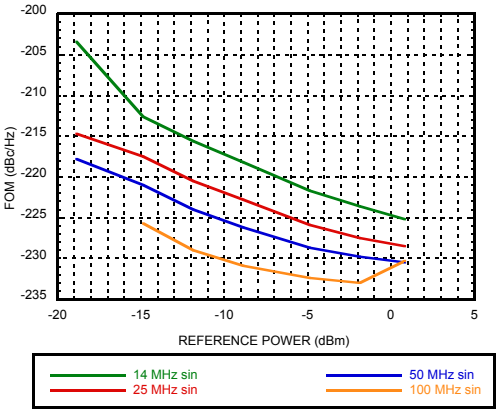


Figure 59. Figure of Merit for PLL/VCO

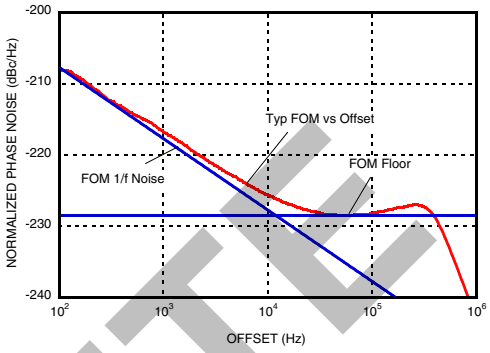


Figure 60. Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode ON [2]

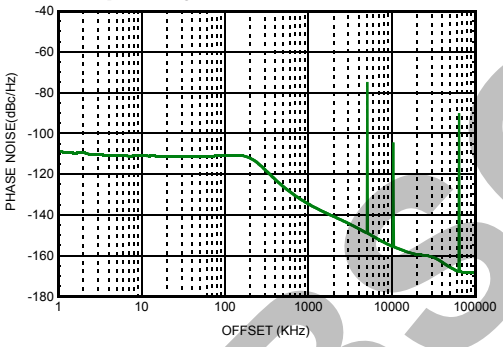


Figure 61. Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode OFF [2]

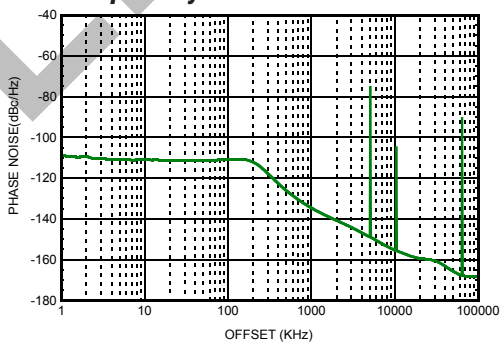


Figure 62. Forward Transmission Gain [3]

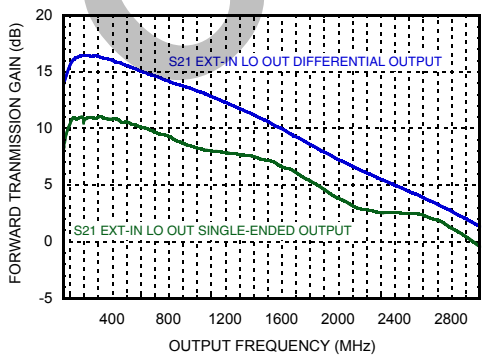
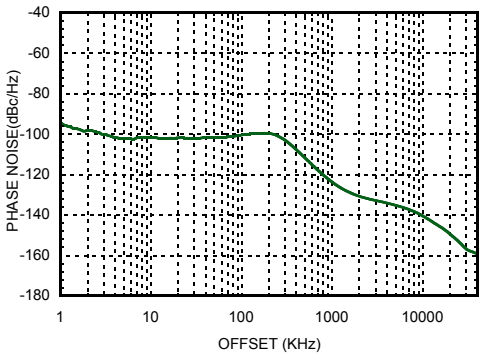


Figure 63. Closed Loop Phase Noise With External VCO HMC384LP4E @ 2200 MHz



[1] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[2] 122.88 MHz clock input, PFD = 61.44 MHz, Channel Spacing = 240 KHz.

[3] S21 from Ext_VCO (pin 43, 44) in and LO (pin32, 33) out.

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Figure 64. Auxiliary LO Differential Output Return Loss

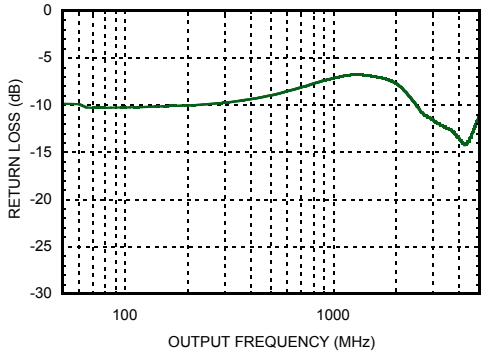


Figure 65. Auxiliary LO Single Ended Output Return Loss

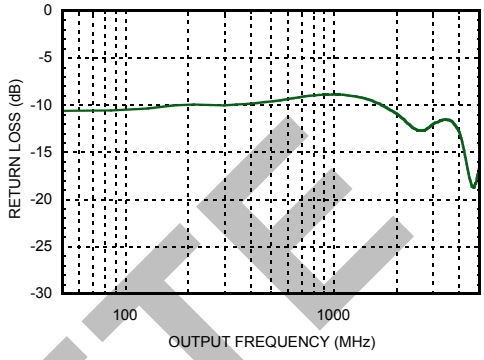


Table 5. Loop Filter Configuration

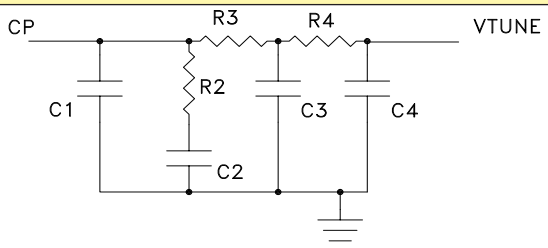
Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
156	180	6.8	47	47	2.2	1	1	

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Table 6. Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
0.7	-65	-45	-67	-63
1.1	-80	-55	-64	-67
1.5	-59	-58	-65	-62
1.9	-59	-54	-72	-64
2.3	-60	-59	-73	-63
2.7	-59	-58	-82	-55
3.1	-60	-58	-77	-48
3.5	-53	-63	-73	-48

LO = Max. level
All values in dBm measured at RF port.

Table 7. MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	-44	-52	-52	-55
1	-49	0	-44	-17	-52
2	-87	-45	-72	-50	-80
3	-88	-62	-88	-71	-87
4	-85	-85	-88	-88	-87

RF Freq. = 0.9 GHz @-5 dBm
LO Freq. = 0.8 GHz @ Max. level
All values in dBc below IF power level (1RF - 1LO).

Table 8. MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xxx	-44	-49	-64	-49
1	-54	0	-43	-28	-65
2	-83	-49	-76	-57	-84
3	-87	-72	-86	-88	-85
4	-83	-83	-85	-85	-87

RF Freq. = 1.9 GHz @-5 dBm
LO Freq. = 1.8 GHz @ Max. level
All values in dBc below IF power level (1RF - 1LO).

Table 9. MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xxx	-44	-47	-65	-53
1	-58	0	-46	-40	-68
2	-80	-60	-75	-67	-85
3	-82	-82	-86	-83	-85
4	-84	-82	-85	-85	-87

RF Freq. = 2.5 GHz @-5 dBm
LO Freq. = 2.4 GHz @Max. level
All values in dBc below IF power level (1RF - 1LO).

Table 10. Truth Table [1]

CHIPEN (V)	PLL/VCO
LOW	OFF
HIGH	ON

[1] IF and LO amplifiers can be disabled through SPI bus. See `Enabling/Disabling Mixer Features` application section.

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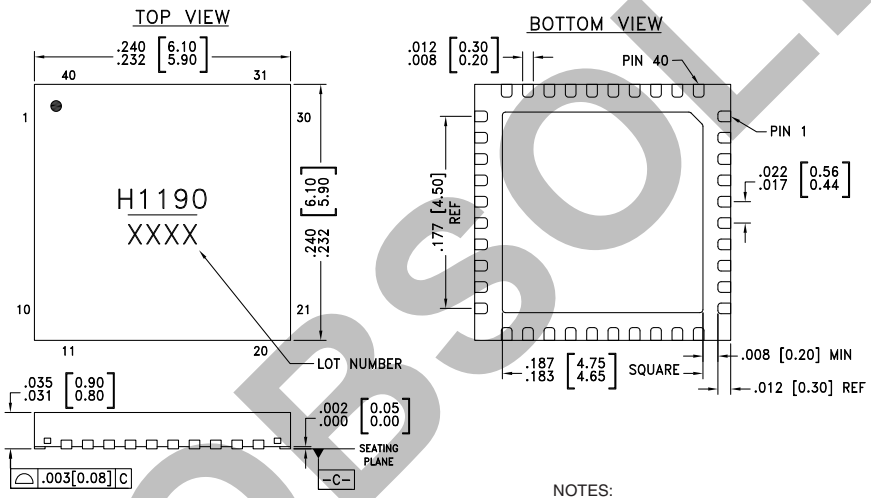
Table 11. Absolute Maximum Ratings

RF Input Power (VBIASIF1,2= +5V, LOVDD=3.0V)	+20 dBm
VBIASIF1,2, LOVDD	6V
VGATE1,2, VDDCP, VCS1, VCS2, LOVDD	-0.3V to +5.5V
3VRVDD, DVDD3V	-0.3V to +3.6V
Max. Channel Temperature	150°C
Thermal Resistance (channel to ground paddle)	3.3°C/W
Storage Temperature	-65 to 150°C
Operating Temperature	-40 to +85°C
ESD Sensitivity (HBM)	Class 1B

Table 12. Recommended Operating Conditions

VDDCP, VCS1, VCS2, VBIASIF1, VBIASIF2,LOBIAS1,LOBIAS2,VCC1,VCC2,VGATE1,VGATE2,VDDLS	5.0 V
LOVDD, 3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF	+3.3 V
Operating Temperature	-40 to +85°C

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC1190LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H1190 XXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

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Table 13. Pin Descriptions

Pin Number	Function	Description
1	VDDCP	Power Supply for charge pump analog section.
2	BIAS	External bypass decoupling for precision bias circuits.
3,4	CP1,CP2	Charge Pump Outputs.
5	3VRVDD	Reference supply, 3.3 V nominal.
6	XREFP	Reference Input. DC bias is generated internally. Normally AC coupled externally.
7	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry, 3.3 V nominal.
8,23	VCS1, VCS2	Bias control pins for IF amplifiers. Connect to 5V supply through 590 Ohms resistors. Refer to application section for proper values of resistors to adjust IF amplifier current.
9	IF1_N	Differential IF outputs. Connect to 5V supply through choke inductors. See application circuit.
10	IF1_P	
21	IF2_P	
22	IF2_N	
11, 20	VBIASIF1, VBIASIF2	Supply voltage pin for IF amplifier's bias circuits. Connect to 5V supply through filtering.
12, 19	VGATE1, VGAET2	Bias pins for mixer cores. Set from 4.7V to 5.0V for operating frequency band.
13, 18	RF1, RF2	RF input pins of the mixer, internally matched to 50 Ohms. RF input pins require off chip DC blocking capacitors. See application circuit.
14, 17	LO_BIAS2, LO_BIAS1	Bias control pins for LO Amplifiers. Connect to 5V supply through 270 Ohms resistors. Refer to application section for proper values of resistors to adjust LO amplifier current.
15,24	RSV	Reserved for internal use.Should be left floating.
16	LOVDD	3V bias supply for LO Drive stages. Refer to application circuit for appropriate filtering and bias generation information.
25	CHIP_EN	Chip Enable. Connect to logic high for normal operation.
26	LON	Negative LO output used for single-ended, differential, or dual output mode.
27	LOP	Positive LO output used for differential or dual outputs only. While it can drive a separate load from LO_N, it cannot be used when LO_N is disabled.
28	VCC1	VCO Analog supply1, 5.0V nominal.
29	VCC2	VCO Analog Supply 2, 5.0V nominal.
30	VTUNE	VCO Varactor. Tuning Port Input.
31	SEN	PLL Serial Port Enable (CMOS) Logic Input.
32	SDI	PLL Serial Port Data (CMOS) Logic Input.
33	SCK	PLL Serial Port Clock (CMOS) Logic Input.
34	LD/SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO).
35	EXT_VC0_N	External VCO negative input
36	EXT_VCO_P	External VCO positive input.
37	VCCHF	Analog supply, 3.3 V nominal
38	VCCPS	Analog supply, Prescaler, 3.3 V nominal
39	VCCPD	Analog supply, Phase Detector, 3.3 V nominal
40	VDDLS	Analog supply, Charge Pump, 5.0 V nominal

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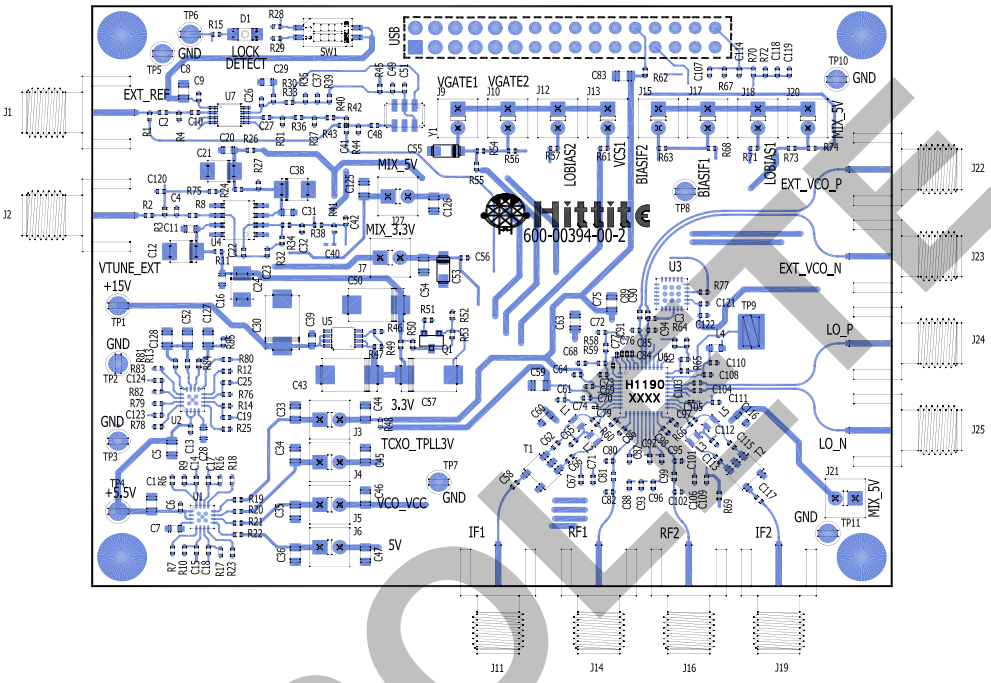
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC1190LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Table 14. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1190LP6GE Evaluation PCB	Eval01-HMC1190LP6G [1]
Evaluation Kit	HMC1190LP6GE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC1190LP6G [2]

[1] Reference this number when ordering Evaluation PCB Only
[2] Reference this number when ordering an HMC1190LP6GE Evaluation KIt

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1.0 Theory of Operation

The block diagram of HMC1190LP6GE PLL with Integrated VCO is shown in Figure 66

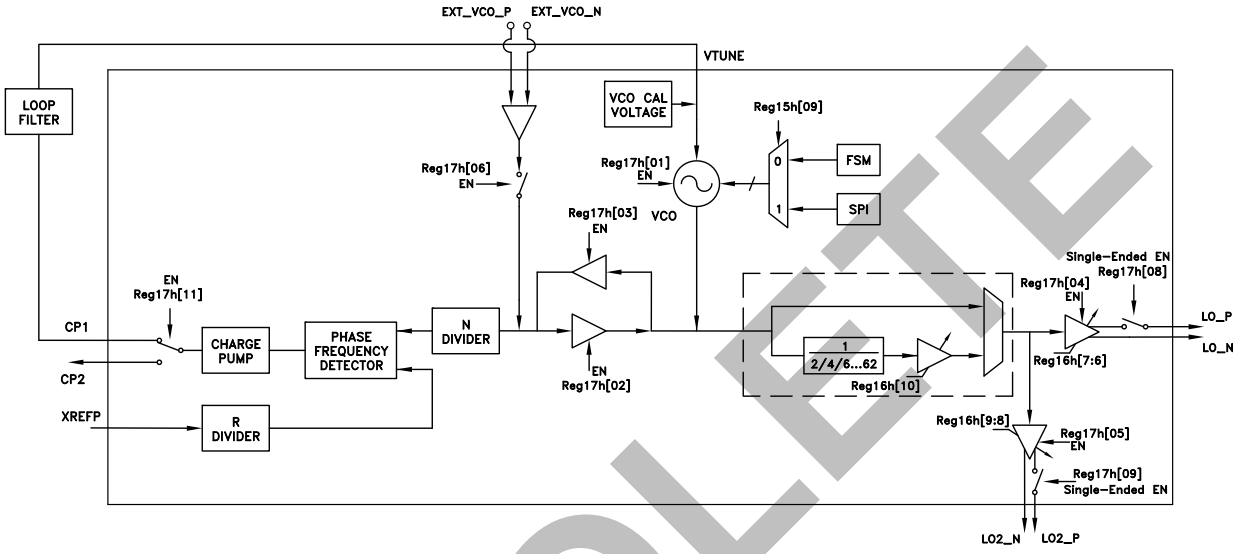

Figure 66. HMC1190LP6GE PLL VCO Block Diagram

1.1 PLL Overview

The PLL divides down the VCO output to the desired comparison frequency via the N-divider (integer value set in Reg 03h, fractional value set in Reg 04h), compares the divided VCO signal to the divided reference signal (reference divider set in Reg 02h) in the Phase Detector (PD), and drives the VCO tuning voltage via the Charge Pump (CP) (configured in Reg 09h) to the VCO subsystem. Some of the additional PLL subsystem functions include:

- Delta Sigma configuration (Reg 06h)
- Exact Frequency Mode (Configured in Reg 0Ch, Reg 06h,Reg 03h, and Reg 04h)
- Lock Detect (LD) Configuration (Reg 07h to configure LD, and Reg 0Fh to configure LD_SDO output pin)
- External CEN pin used as hardware enable pin.

Typically, only writes to the divider registers (integer part Reg 03h, fractional part Reg 04h,VCO Divide Ratio part Reg 04h) are required for HMC1190LP6GE output frequency changes.

Divider registers of the PLL (Reg 03h, and Reg 04h), set the fundamental frequency (2050 MHz to 4100 MHz) of the VCO. Output frequencies ranging from 33 MHz to 2050 MHz are generated by tuning to the appropriate fundamental VCO frequency (2050 MHz to 4100 MHz) by programming N divider (Reg 03h, and Reg 04h), and programming the output divider (divide by 1/2/4/6.../60/62, programmed in Reg 16h) in the VCO register.

For detailed frequency tuning information and example, please see "1.3.7 Frequency Tuning" section.

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1.2 VCO Overview

The VCO consists of a capacitor switched step tuned VCO and an output stage. In typical operation, the VCO is programmed with the appropriate capacitor switch setting which is executed automatically by the PLL AutoCal state machine if AutoCal is enabled (Reg 0Ah[11] = 0, see section "1.2.1 VCO Calibration" for more information). The VCO tunes to the fundamental frequency (2050 MHz to 4100 MHz), and is locked by the CP output from the PLL subsystem. The VCO controls the output stage of the HMC1190LP6GE enabling configuration of:

- VCO Output divider settings configured in Reg 16h (divide by 2/4/6...60/62 to generate frequencies from 33 MHz to 2050 MHz, or divide by 1 to generate fundamental frequencies between 2050 MHz and 4100 MHz)
- Output gain settings (Reg 16h[7:6], Reg 16h[9:8])
- Single-ended or differential output operation (Reg 17h[9:8])
- Always Mute (Reg 16h[5:0])
- Mute when unlock (Reg 17h[7])

1.2.1 VCO Calibration

1.2.1.1 VCO Auto-Calibration (AutoCal)

The HMC1190LP6GE uses a step tuned type VCO. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or 'stepped' by switching in/out VCO tank capacitors. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the HMC1190LP6GE's charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (kvco).

The VCO switches are normally controlled automatically by the HMC1190LP6GE using the Auto-Calibration feature. The Auto-Calibration feature is implemented in the internal state machine. It manages the selection of the VCO sub-band (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via register Reg 15h for testing or for other special purpose operation.

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC1190LP6GE knows which switch position on the VCO is optimum for the desired output frequency. The HMC1190LP6GE supports Auto-Calibration (AutoCal) of the step tuned VCO. The AutoCal fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 67.Note how the tuning voltage stays in a narrow range over a wide range of output frequencies such as fast frequency hopping.

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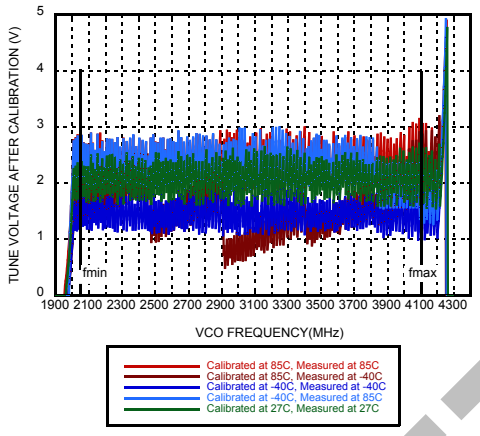

Figure 67.Typical VCO Tuning Voltage After Calibration

The calibration is normally run automatically once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally have to be concerned about which switch setting is used for a given frequency as this is handled by the AutoCal routine. The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency, and ensures that the VCO will stay locked and perform well over it's full temperature range without additional calibration, regardless of the temperature that the VCO was calibrated at.

Auto-Calibration can also be disabled allowing manual VCO tuning. Refer to section 1.2.1.5 for a description of manual tuning.

1.2.1.2 Auto-reLock on Lock Detect Failure

It is possible by setting Reg 0Ah[17] to have the VCO subsystem automatically re-run the calibration routine and re-lock itself if Lock Detect indicates an unlocked condition for any reason. With this option the system will attempt to re-Lock only once.

1.2.1.3 VCO AutoCal on Frequency Change

Assuming Reg 0Ah[11]=*0*, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the AutoCal routine for any reason, at the same frequency, simply rewrite the frequency change with the same value and the AutoCal routine will execute again without changing final frequency.

1.2.1.4 VCO AutoCal Time & Accuracy

The VCO frequency is counted for T_{mmt}, the period of a single AutoCal measurement cycle.

$$T_{mmt} = T_{xtal} \cdot R \cdot 2^n \quad \text{(EQ 1)}$$

n — is set by Reg 0Ah[2:0] and results in measurement periods which are multiples of the PD period, $T_{xtal}R$.

R — is the reference path division ratio currently in use, Reg 02h

T_{xtal} — is the period of the external reference (crystal) oscillator.

The VCO AutoCal counter will, on average, expect to register N counts, rounded down (floor) to the nearest integer, every PD cycle.

N — is the ratio of the target VCO frequency, f_{vco}, to the frequency of the PD, f_{pd}, where N can

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