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HMC1197LP7FE

v03.0314

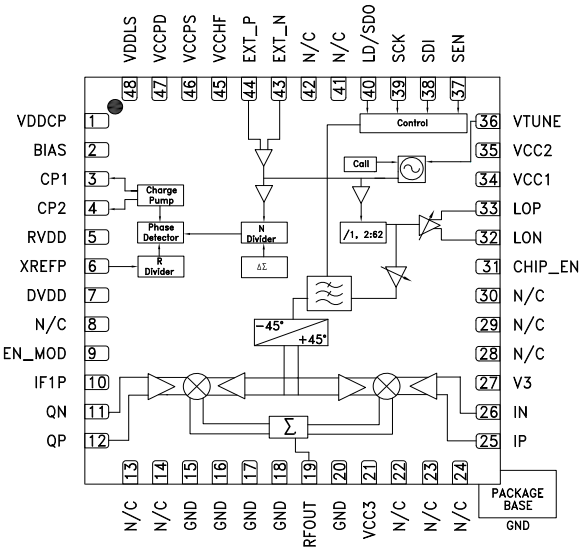
WIDEBAND DIRECT QUADRATURE MODULATOR w/ Fractional-N PLL & VCO, 100 - 4000 MHz

Typical Applications

The HMC1197LP7FE is Ideal for:

- Multiband/Multi-standard Cellular BTS Diversity Transmitters
- Fixed Wireless or WLL
- ISM Transceivers, 900 & 2400 MHz
- GMSK, QPSK, QAM, SSB Modulators
- Multiband Basestations & Repeaters

Functional Diagram



Features

Very Low Noise Floor, -159.5 dBm/Hz

Excellent Carrier & Sideband Suppression

Very High Linearity, +28.5 dBm OIP3

High Output Power, +10.5 dBm Output P1dB

High Modulation Accuracy

Maximum Phase Detector Rate: 100 MHz

Low Phase Noise: -110 dBc/Hz in Band Typical

PLL FOM:

-230 dBc/Hz Integer Mode, -227 dBc/Hz Fractional Mode

< 180 fs Integrated RMS Jitter (1 kHz to 20 MHz)

Differential Auxiliary LO output

External LO Input

Exact Frequency Mode:
0 Hz Fractional Frequency Error

Programmable RF Output Phase

Output Phase Synchronous Frequency Changes

Output Phase Synchronization

Internal LO Mute Function

48 Lead 7x7 mm QFN Package: 49 mm^2

General Description

The HMC1197LP7FE is a low noise, high linearity Direct Quadrature Modulator with Fractional-N PLL&VCO RFIC which is ideal for digital modulation applications from 0.1 to 4.0 GHz including; Cellular/3G, LTE/WiMAX/4G, Broadband Wireless Access & ISM circuits housed in a compact 7x7 mm (LP7) SMT QFN package, the HMC1197LP7FE RFIC requires minimal external components & provides a low cost alternative to more complicated double upconversion architectures. The RF output port is single-ended and matched to 50 Ohms with no external components.

Auxiliary LO output (differential or single-ended), enables the HMC1197LP7FE to distribute identical frequency and phase signals to multiple destinations. Individual gain settings ensure optimal signal levels tailored to each output.

External VCO input allows the HMC1197LP7FE to lock external VCOs, and enables cascaded LO architectures for MIMO radio applications. Two separate Charge Pump (CP) outputs enable separate loop filters optimized for both integrated and external VCOs, and seamless switching between integrated or external VCOs during operation. Programmable RF output phase feature can further phase adjust and synchronize multiple HMC1197LP7FEs enabling scalable MIMO and beam-forming radio architectures.

Integrated programmable Low Pass Filter (LPF) on the modulator LO input ensures no LO harmonic contribution to modulator sideband rejection performance. Sixteen programmable LPF bands enable true wideband operation, eliminating the need for external band specific harmonic filtering hardware.

Additional features include configurable LO output mute function. Exact Frequency Mode that enables the HMC1197LP7FE to generate fractional frequencies with 0 Hz frequency error and the ability to synchronously change frequencies without changing the phase of the output signal.

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HMC1197* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC1197LP7F Evaluation Board

DOCUMENTATION

Data Sheet

- HMC1197 Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: LP7, LP7D, LP7F, LP7G (QTR: 2014-00374 REV: 01)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

DESIGN RESOURCES

- HMC1197 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC1197 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

Table 1. Electrical Specifications, See Test Conditions on page-4.

Parameter	Typ.	Typ.	Typ.	Typ.	Units
Frequency Range, RF	450-960	1700-2200	2200-2700	3400-4000	MHz
Output Power	-2.0	-1.1	-1.3	-3.2	dBm
Conversion Voltage Gain	-6.0	-5.1	-5.3	-7.2	dB
Output P1dB	+10.5	+10.5	+10	+9.5	dBm
Output Noise Floor	-159.5	-157.0	-156.5	-156.5	dBm/Hz
Output IP3	+28.5	+26.5	+26.0	+23.5	dBm
Carrier Feedthrough (uncalibrated)	-40	-37.0	-33.5	-34.5	dBm
Sideband Suppression (uncalibrated)	45	45	43	30.5	dBc
RF Port Return Loss	12.5	15	16	16	dB

Table 2. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Output					
RF Frequency Range		100		4000	MHz
RF Return Loss			15		dB
Baseband Input Port					
Baseband Input DC Voltage (Vbbdc)			+0.5 (+0.4 to +0.6)		V
Baseband Input DC Bias Current (Ibbdc)	Single-ended.		110		pA
Single-ended Baseband Input Capacitance	De-embed to the lead of the device.		4.5		pF
DC Power Supply					
Supply Voltage (VCC1, VCC2, VCC3, VDDLS, VDDCP, BIAS, IF1P)		+4.75	+5.0	+5.25	V
Supply Current of +5V Supply (I_{CC1})	Modulator ON and PLL ON		320		mA
	Modulator OFF and PLL ON		152		mA
	Modulator OFF and PLL OFF		12		mA
Supply Voltage (V3, DVDD, RVDD, VCCPD, VCCPS, VCCHF)		3.15	+3.3	3.45	V
Supply Current of +3.3V Supply (I_{CC2})	Modulator ON and PLL ON		48		mA
	Modulator OFF and PLL ON		48		mA
	Modulator OFF and PLL OFF		1		mA
Enable/Disable Interface					
EN High Level	Modulator disabled		5		V
EN Low Level	Modulator enabled		0		V
Enable/Disable Settling Time			400/400		ns
LO Leakage Isolation	EN_MOD=5V, LO=2.1GHz		-75		dBm
Logic Inputs					
Logic High		1.2			V
Logic Low				0.6	V
Input Current				+/- 1	uA
Input Capacitance			2		pF
LO Output Characteristics					
LO Output Frequency		50		4100	MHz
VCO Frequency at PLL Input		2000		4100	MHz

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Table 2. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
VCO Fundamental Frequency		2000		4100	MHz
VCO Output Divider					
VCO Output Divider Range	1, 2, 4, ... 60, 62	1		62	
PLL RF Divider Characteristics					
19-Bit N Divider Range	Integer	16		524287	
	Fractional	20		524283	
Phase Detector (PD)					
PD Frequency	Fractional Mode	DC		100	MHz
	Integer Mode	DC		100	MHz
Harmonics					
fo Mode at 4000 MHz	2nd / 3rd / 4th		-30/-22/-32		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled	1	2	3.3	Vpp
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at fo @ 3 GHz/2 = 1.5 GHz					
10 kHz Offset			-83		dBc/Hz
100 kHz Offset			-113		dBc/Hz
1 MHz Offset			-139.5		dBc/Hz
10 MHz Offset			-165.5		dBc/Hz
100 MHz Offset			-167		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz

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Table 2. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
VCO Characteristics					
VCO Tuning Sensitivity at 3862 MHz	Measured at 2.5 V		15		MHz/V
VCO Tuning Sensitivity at 3643 MHz	Measured at 2.5 V		14.5		MHz/V
VCO Tuning Sensitivity at 3491 MHz	Measured at 2.5 V		16.2		MHz/V
VCO Tuning Sensitivity at 3044 MHz	Measured at 2.5 V		14.6		MHz/V
VCO Tuning Sensitivity at 2558 MHz	Measured at 2.5 V		15.4		
VCO Tuning Sensitivity at 2129 MHz	Measured at 2.5 V		14.8		
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

Table 3. Test Conditions: Unless Otherwise Specified, the Following Test Conditions Were Used

Parameter	Condition
Temperature	+25 °C
Baseband Input Frequency	200 kHz
Baseband Input DC Voltage (Vbbdc)	+0.5 V
Baseband Input AC Voltage (Peak to Peak Differential, I and Q)	1.0 V
Baseband Input AC Voltage for OIP3 Measurements (Peak to Peak Differential, I and Q)	500 mV per tone @ 150 & 250 KHz
Baseband Input AC Voltage for Noise Floor Measurements (Peak to Peak Differential, I and Q)	no baseband input voltage
Frequency Offset for Output Noise Measurements	20 MHz
Supply Voltage (VCC1, VCC2, VCC3, VDDLS, VDDCP, BIAS)	+5.0V
Supply Voltage (V3, DVDD, RVDD, VCCPD, VCCPS, VCCHF)	+3.3V
LO Power Level	Maximum Power
Mounting Configuration	Refer to HMC1197LP7FE Application Schematic Herein
Sideband & Carrier Feedthrough	Uncalibrated

Table 4. Filter Bank Selection vs. Frequency

Frequency (MHz)	≤ 500	600	700	800	900	1000/1100	1200	1300/1400/1500	1600	1700/1800	1900/2000	2000 ≥
Frequency (MHz)	≤ 500	600	700	800	900	1000/1100	1200	1300/1400/1500	1600	1700/1800	1900/2000	2000 ≥
Filter Bank Selection	0	1	5	7	8	0	7	8	9	10	11	15

Calibrated vs. Uncalibrated Test Results

During the Uncalibrated Sideband and Carrier Suppression tests, care is taken to ensure that the I/Q signal paths from the Vector Signal Generator (VSG) to the Device Under Test (DUT) are equal. The “Uncalibrated” Sideband and Carrier Suppression plots were measured at T= -40 °C, +25 °C, and +85 °C.

The “Calibrated” Sideband Suppression data was plotted after a manual adjustment of the I/Q amplitude balance and I/Q phase offset (skew) at +25 °C, 5V and 3.3V Vcc, LO maximum power level. The +25 °C adjustment settings were held constant during tests over temperature.

The “Calibrated” Carrier Suppression data was plotted after a manual adjustment of the IP/IN & QP/QN DC offsets at +25 °C, 5V and 3.3V Vcc, LO maximum power level. The +25 °C adjustment settings were held constant during tests over temperature.

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Figure 1. RF Output Power vs. Frequency Over Temperature

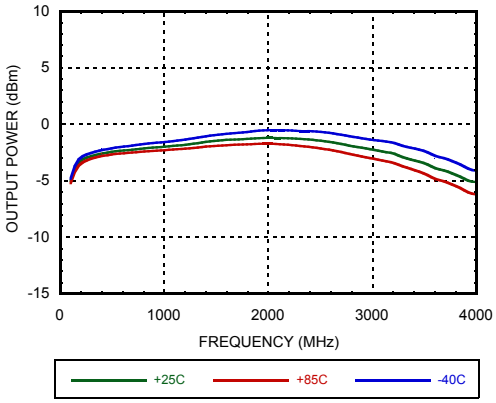


Figure 2. RF Output IP3, P1dB & Noise Floor @ 20 MHz Offset vs. Frequency Over Temperature

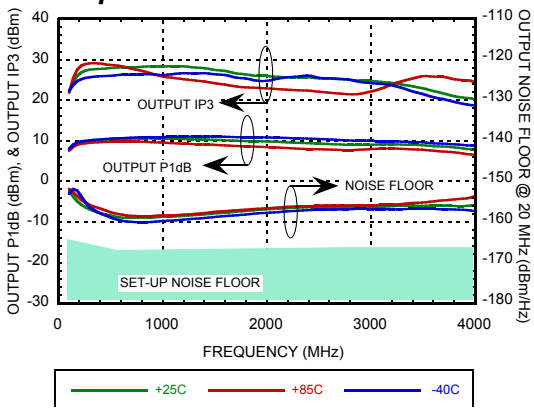


Figure 3. Uncalibrated Carrier Feedthrough vs. Frequency Over Temperature [1]

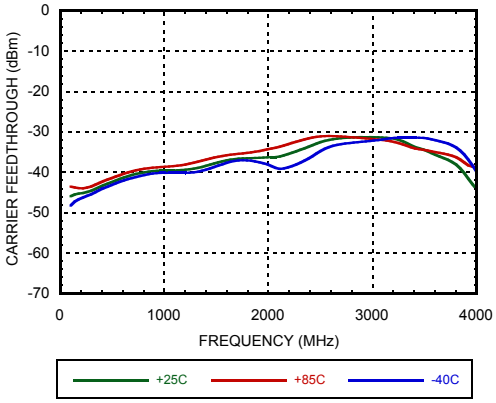


Figure 4. Calibrated Carrier Feedthrough vs. Frequency Over Temperature [1]

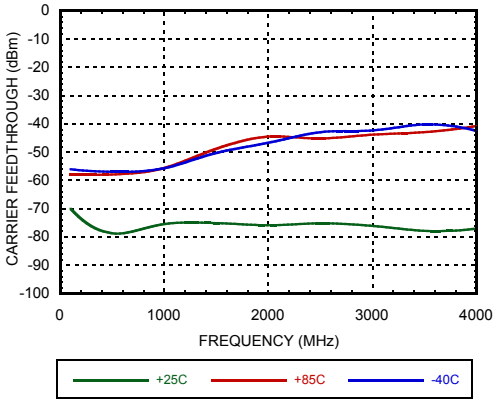


Figure 5. Uncalibrated Carrier Feedthrough vs. Frequency Over Temperature When Modulator is Disabled

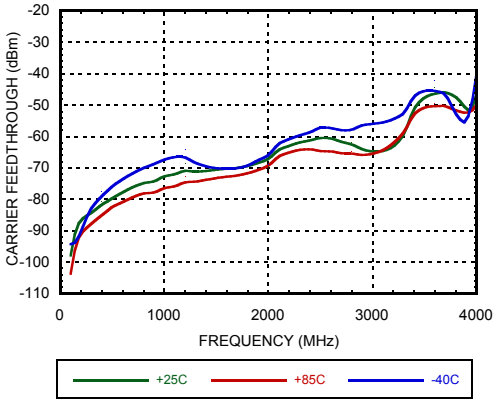
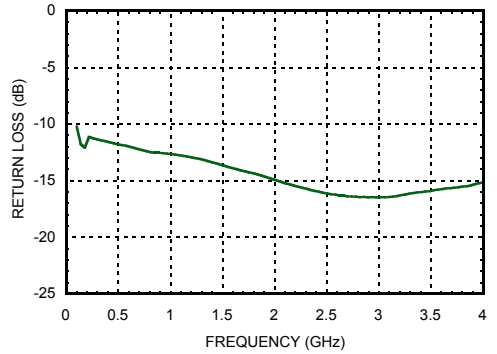


Figure 6. RF Return Loss vs. Frequency



[1] See note titled "Calibrated vs. Uncalibrated test results" herein.

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Figure 7. RF Output Power & SBR vs. Frequency Over LO Power

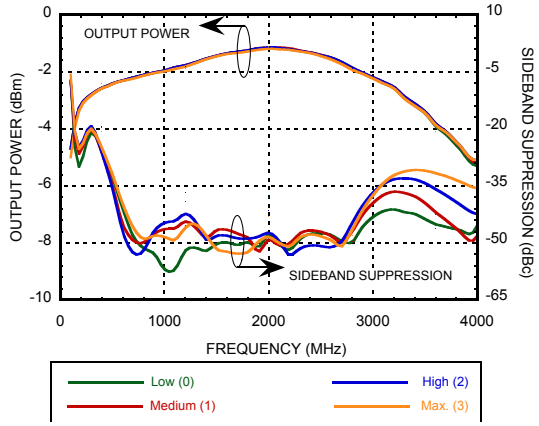


Figure 8. RF Output IP3, P1dB & Noise Floor @ 20 MHz Offset vs. Frequency Over LO Power

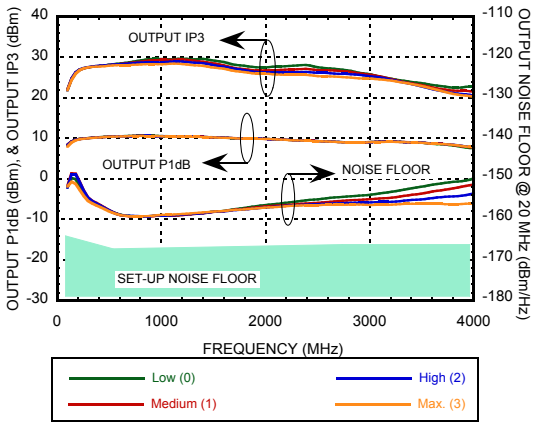


Figure 9. Uncalibrated Sideband Suppression vs. Frequency Over Temperature [1]

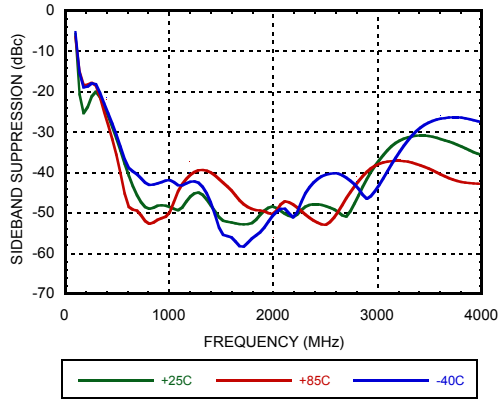


Figure 10. Calibrated Sideband Suppression vs. Frequency Over Temperature [1]

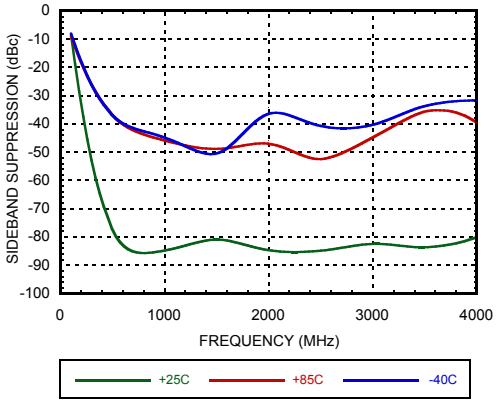


Figure 11. RF Output Power & SBR vs. Frequency Over Supply Voltage

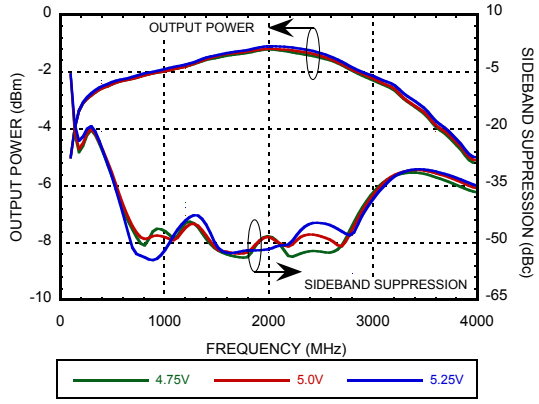
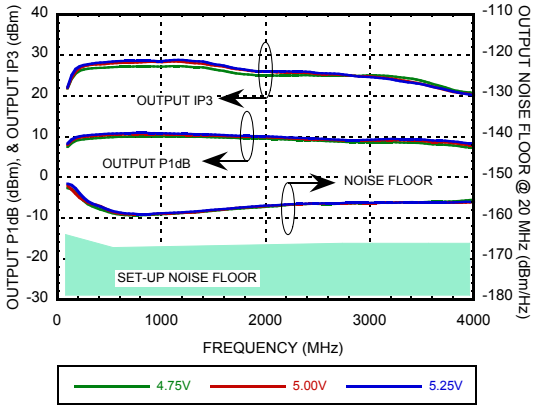


Figure 12. RF Output IP3, P1dB & NoiseFloor @ 20 MHz Offset vs. Frequency Over Supply Voltage



[1] See note titled "Calibrated vs. Uncalibrated test results" herein.

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Figure 13. RF Output Power vs. Baseband Voltage @ 2100 MHz

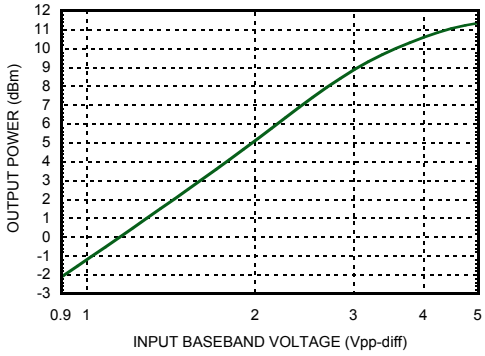


Figure 14. RF Output Noise @ 20 MHz Offset vs. Output Power Over LO Frequency

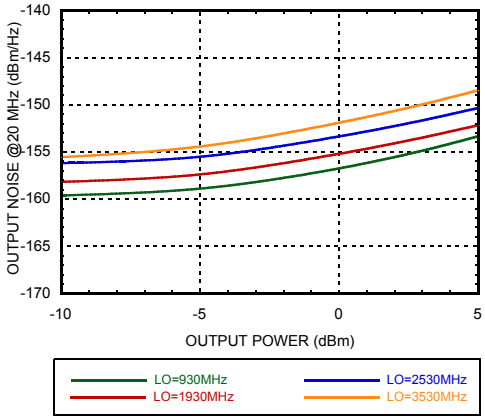
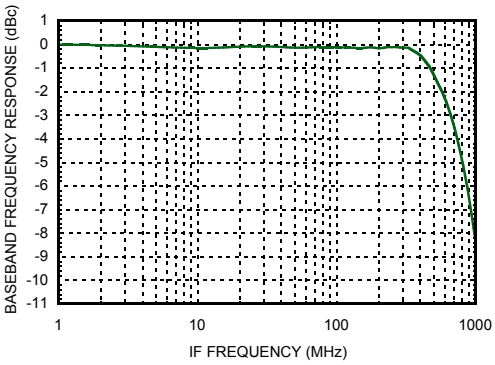


Figure 15. Normalized Baseband Frequency Response [1]



[1] I/Q input bandwidth normalized to gain at 1 MHz (fLO=1800 MHz). I/Q inputs are matched to 100 Ohms differentially.

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Figure 16. Auxiliary LO Output, Open Loop Phase Noise @ 3600 MHz

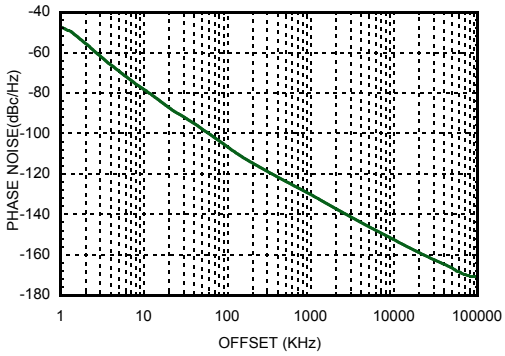


Figure 17. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @3600 MHz with various divider ratios [1]

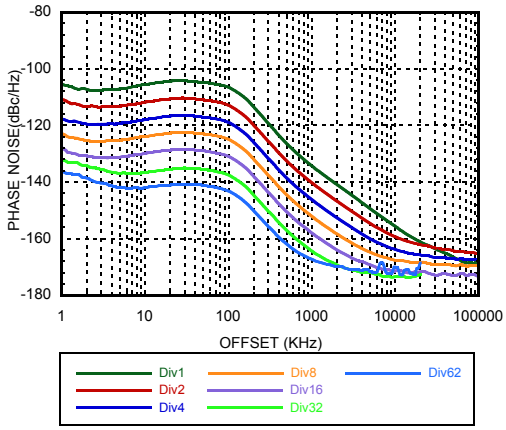


Figure 18. Auxiliary LO Output, Open Loop Phase Noise @ 4100 MHz

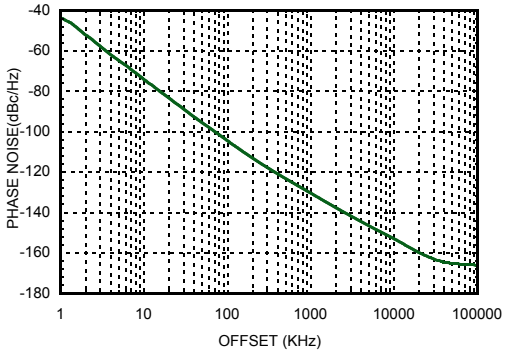


Figure 19. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @4100 MHz with various divider ratios [1]

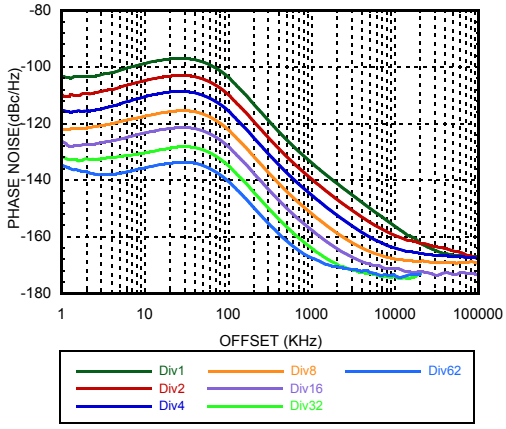
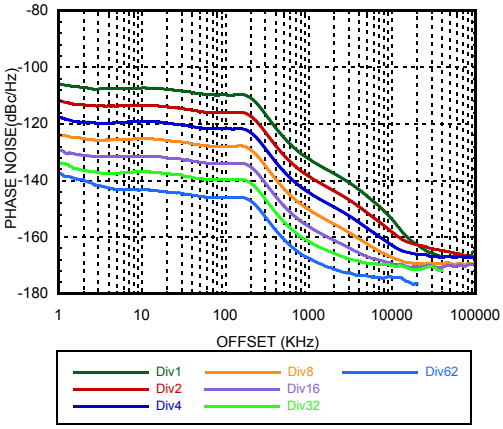


Figure 20. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @ 3300 MHz with various divider ratios [2]



[1] Using 122.88 MHz clock input, 61.44 MHz PFD, 2.5 mA CP, 174 uA Leakage

[2] Using 100 MHz clock input, 50MHz PFD, 2.5 mA CP, 174 uA Leakage

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Figure 21. Auxiliary LO Output, Open Loop Phase Noise vs. Frequency

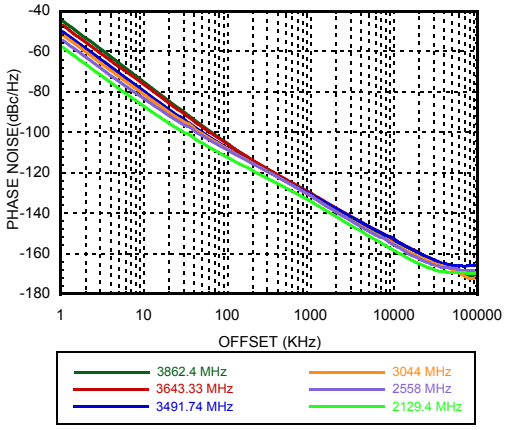


Figure 22. Auxiliary LO Output, Open Loop Phase Noise vs. Temperature

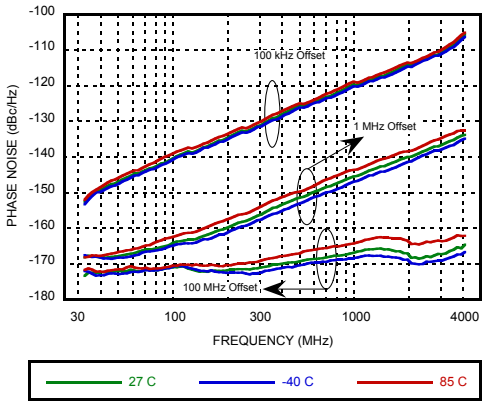


Figure 23. Auxiliary LO Output Power vs Temperature [1]

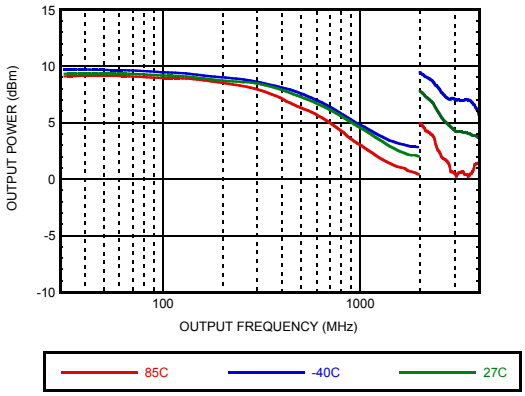


Figure 24. Integrated RMS Jitter [2]

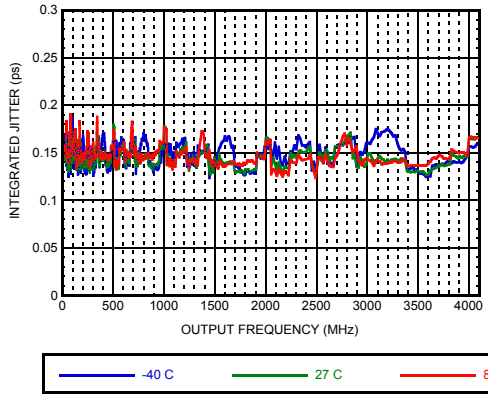


Figure 25. Typical VCO Sensitivity

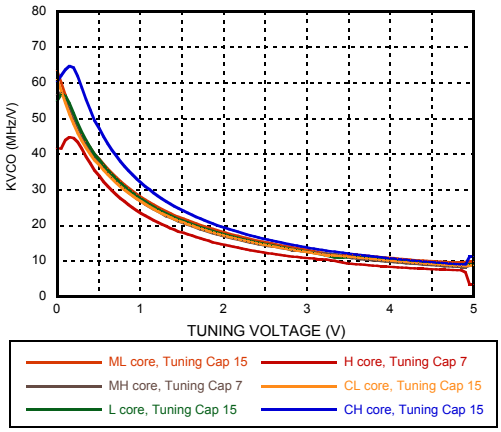
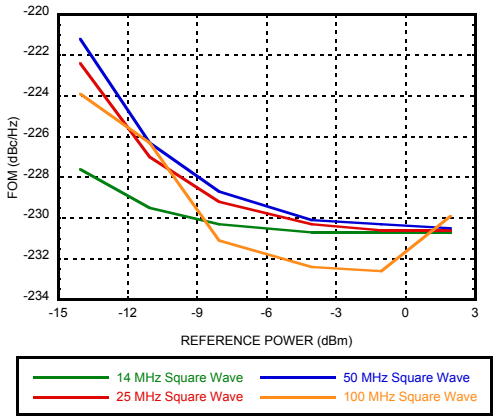


Figure 26. Reference Input Sensitivity, Square Wave, 50 Ω [3]



[1] Both Aux. LO and MOD LO Gain Set to '3' (Max Level), both Aux. LO and MOD LO Buffer Enabled, measured from Auxiliary LO Port.

[2] RMS Jitter data is measured in fractional mode using 50 MHz reference frequency, from 1 kHz to 100 MHz integration bandwidth.

[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

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Figure 27. Reference Input Sensitivity, Sinusoid Wave, 50 Ω [1]

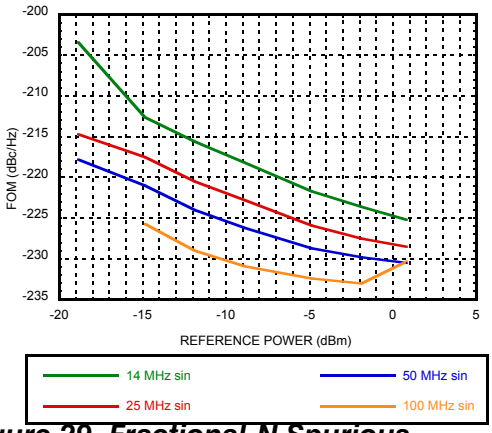


Figure 28. Figure of Merit for PLL/VCO

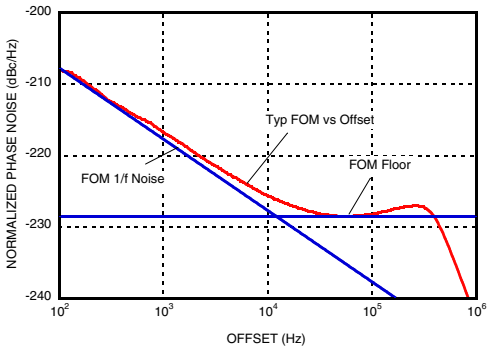


Figure 29. Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode ON [2]

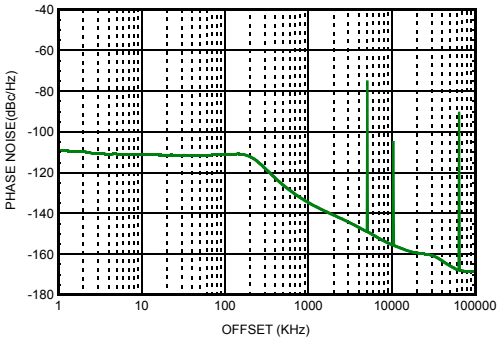


Figure 30. Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode OFF [2]

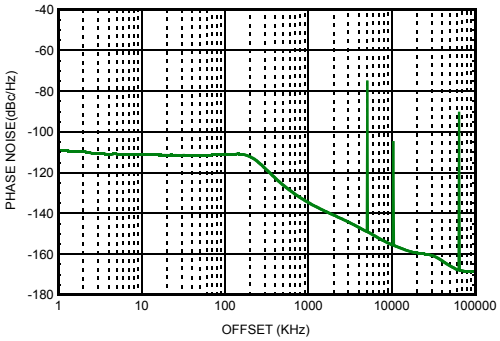


Figure 31. Forward Transmission Gain [3]

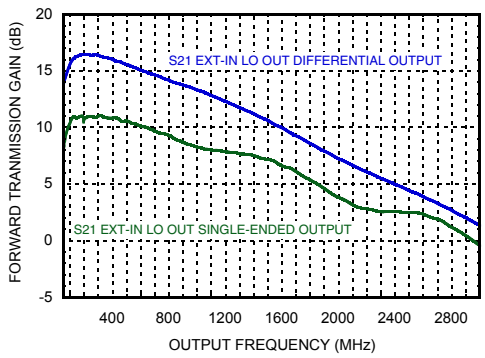
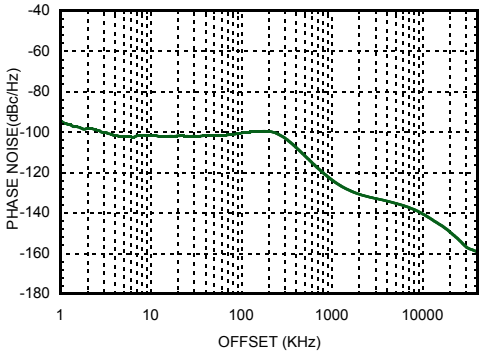


Figure 32. Closed Loop Phase Noise With External VCO HMC384LP4E @ 2200 MHz



[1] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[2] 122.88 MHz clock input, PFD = 61.44 MHz, Channel Spacing = 240 KHz.

[3] S21 from Ext_VCO (pin 43, 44) in and LO (pin32, 33) out.

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Figure 33. Auxiliary LO Differential Output Return Loss

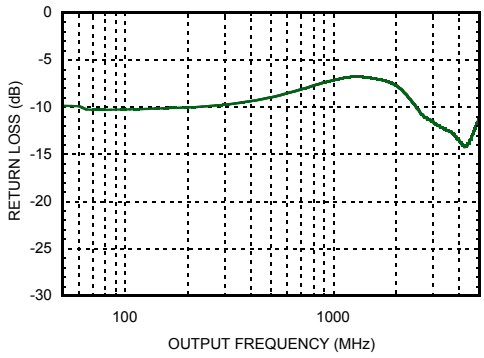


Figure 34. Auxiliary LO Single Ended Output Return Loss

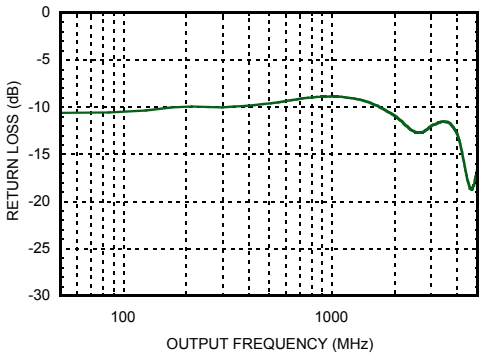


Table 5. Loop Filter Configuration

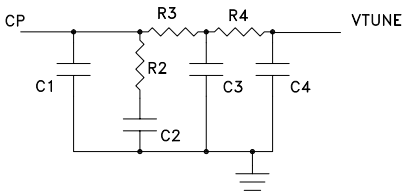
Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
156	180	6.8	47	47	2.2	1	1	

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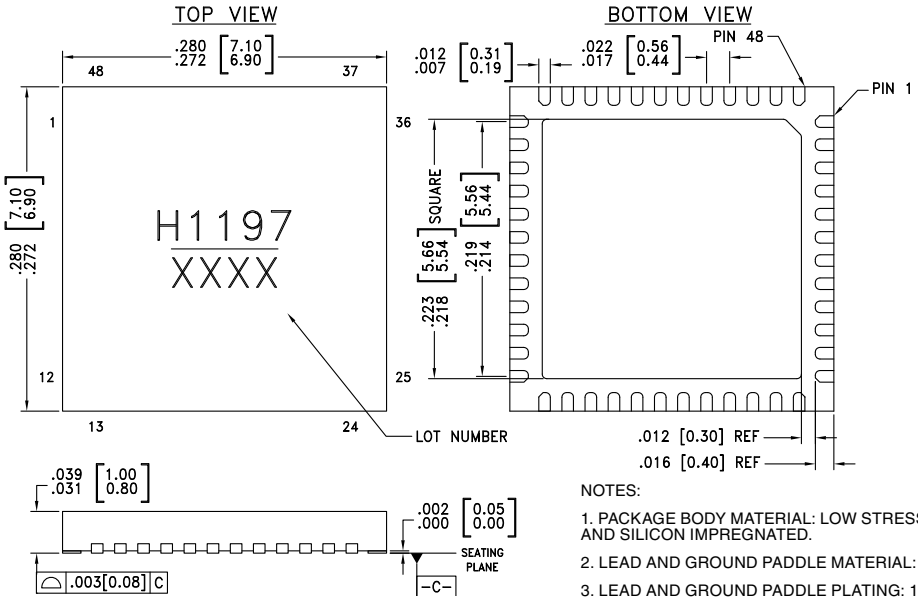
Table 6. Absolute Maximum Ratings

VCC1, VCC2, VCC3, VDDLS, VDDCP, BIAS, IF1P, EN_MOD	-0.3V to +5.5V
V3, DVDD, RVDD, VCCPD, VCCPS, VCCHF	-0.3V to +3.6V
Baseband Input Voltage (AC + DC) (Reference to GND)	-0.3V to + 1.3V
Junction Temperature	150°C
Thermal Resistance (R_{th}) (junction to ground paddle)	4.5 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 7. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC1197LP7FE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H1197 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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Table 8. Pin Descriptions

Pin Number	Function	Description
1	VDDCP	Power Supply for charge pump analog section, 5.0V nominal.
2	BIAS	External bypass decoupling for precision bias circuits, 5.0V nominal.
3,4	CP1,CP2	Charge Pump Outputs.
5	RVDD	Reference Supply, 3.3V nominal.
6	XREFP	Reference Input. DC bias is generated internally. Normally AC coupled externally.
7	DVDD	DC Power Supply for Digital (CMOS) Circuitry, 3.3V nominal.
8, 13, 14, 22, 23, 24, 28, 29, 30, 41, 42	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
9	EN_MOD	This pin has a 10 Kohm pulldown resistor to GND. When connected to GND or left floating the chip is fully enabled. When connected to VCC the LO amplifiers and the mixers are disabled.
10	IF1P	Supply voltage for the LO and mixer stage, 5.0V nominal.
11, 12	QN, QP	Q channel differential baseband input.These are high impedance ports. The nominal recommended bias voltage is 0.45V (0.4V-0.5V)[1].The nominal recommended baseband input AC voltage is 1.3V peak-to-peak differential.By adjusting the DC offsets on ports QN & QP , the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltege for optimization is less than 15 mV. The amplitude and phase difference between The I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level
15, 16, 17, 18, 20	GND	These pins and package base must be connected to RF and DC ground.
19	RFOUT	DC coupled and matched to 50 Ohms. Output requires an external DC blocking capacitor.
21	VCC3	Supply voltage for the output stages, 5.0V nominal.
25, 26	IP, IN	I channel differential baseband input. These are high impedance ports. The nominal recommended bias voltage is 0.45V (0.4V-0.5V). The nominal recommended baseband input AC voltage is 1.3V peak-to-peak differential.By adjusting the DC offsets on ports IN & IP , the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltege for optimization is less than 15 mV. The amplitude and phase difference between The I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level
27	V3	Supply pin for low pass filter, 3.3V nominal.
31	CHIP_EN	Chip Enable. Connect to logic high for normal operation.
32, 33	LON, LOP	LO outputs. AC coupled and matched to 50 Ohms single ended. Do not need external DC decoupling capacitors. The ports could be single-ended or differential.
34	VCC1	VCO analog supply 1, 5.0V nominal.
35	VCC2	VCO analog supply 2, 5.0V nominal.
36	VTUNE	VCO Varactor. Tuning Port Input.
37	SEN	PLL Serial Port Enable (CMOS) Logic Input.
38	SDI	PLL Serial Port Data (CMOS) Logic Input.
39	SCK	PLL Serial Port Clock (CMOS) Logic Input.

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Pin Descriptions

Pin Number	Function	Description
40	LD/SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO).
43	EXT_N	External VCO negative input.
44	EXT_P	External VCO positive input.
45	VCCHF	Analog supply, 3.3V nominal.
46	VCCPS	Analog supply, Prescaler, 3.3V nominal.
47	VCCPD	Analog supply, Phase Detector, 3.3 V nominal.
48	VDDLS	Analog supply, Charge Pump, 5.0 V nominal.

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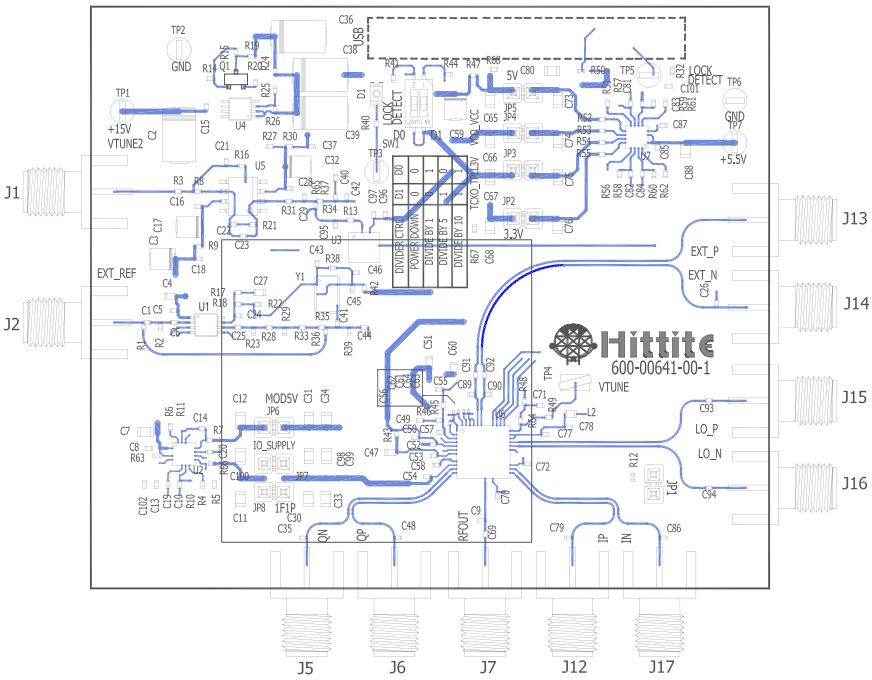
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC1197LP7FE from the "Search by Part Number" pull down menu to view the product splash page.

Table 9. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1197LP7FE Evaluation PCB	EVAL01-HMC1197LP7F
Evaluation Kit	HMC1197LP7FE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC1197LP7F

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1.0 Theory of Operation

The block diagram of HMC1197LP7FE PLL with Integrated VCO is shown in Figure 35

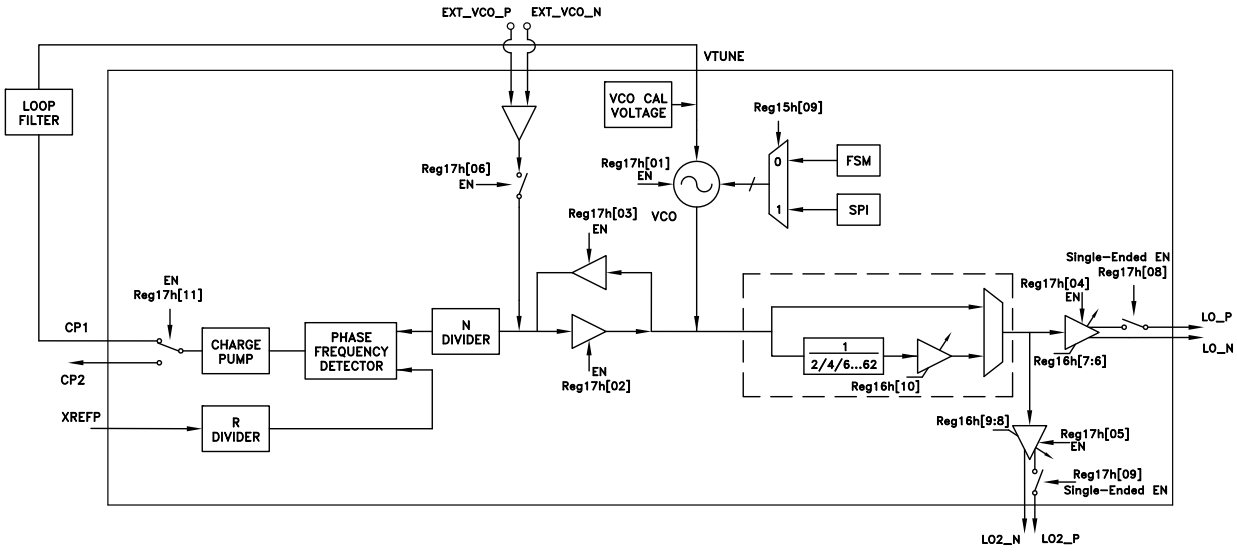

Figure 35. HMC1197LP7FE PLL VCO Block Diagram

1.1 PLL Overview

The PLL divides down the VCO output to the desired comparison frequency via the N-divider (integer value set in Reg 03h, fractional value set in Reg 04h), compares the divided VCO signal to the divided reference signal (reference divider set in Reg 02h) in the Phase Detector (PD), and drives the VCO tuning voltage via the Charge Pump (CP) (configured in Reg 09h) to the VCO subsystem. Some of the additional PLL subsystem functions include:

- Delta Sigma configuration (Reg 06h)
- Exact Frequency Mode (Configured in Reg 0Ch, Reg 06h,Reg 03h, and Reg 04h)
- Lock Detect (LD) Configuration (Reg 07h to configure LD, and Reg 0Fh to configure LD_SDO output pin)
- External CEN pin used as hardware enable pin.

Typically, only writes to the divider registers (integer part Reg 03h, fractional part Reg 04h,VCO Divide Ratio part Reg 04h) are required for HMC1197LP7FE output frequency changes.

Divider registers of the PLL (Reg 03h, and Reg 04h), set the fundamental frequency (2050 MHz to 4100 MHz) of the VCO. Output frequencies ranging from 33 MHz to 2050 MHz are generated by tuning to the appropriate fundamental VCO frequency (2050 MHz to 4100 MHz) by programming N divider (Reg 03h, and Reg 04h), and programming the output divider (divide by 1/2/4/6.../60/62, programmed in Reg 16h) in the VCO register.

For detailed frequency tuning information and example, please see "1.3.7 Frequency Tuning" section.

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1.2 VCO Overview

The VCO consists of a capacitor switched step tuned VCO and an output stage. In typical operation, the VCO is programmed with the appropriate capacitor switch setting which is executed automatically by the PLL AutoCal state machine if AutoCal is enabled (Reg 0Ah[11] = 0, see section "1.2.1 VCO Calibration" for more information). The VCO tunes to the fundamental frequency (2050 MHz to 4100 MHz), and is locked by the CP output from the PLL subsystem. The VCO controls the output stage of the HMC1197LP7FE enabling configuration of:

- VCO Output divider settings configured in Reg 16h (divide by 2/4/6...60/62 to generate frequencies from 33 MHz to 2050 MHz, or divide by 1 to generate fundamental frequencies between 2050 MHz and 4100 MHz)
- Output gain settings (Reg 16h[7:6], Reg 16h[9:8])
- Single-ended or differential output operation (Reg 17h[9:8])
- Always Mute (Reg 16h[5:0])
- Mute when unlock (Reg 17h[7])

1.2.1 VCO Calibration

1.2.1.1 VCO Auto-Calibration (AutoCal)

The HMC1197LP7FE uses a step tuned type VCO. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or 'stepped' by switching in/out VCO tank capacitors. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the HMC1197LP7FE's charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (kvco).

The VCO switches are normally controlled automatically by the HMC1197LP7FE using the Auto-Calibration feature. The Auto-Calibration feature is implemented in the internal state machine. It manages the selection of the VCO sub-band (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via register Reg 15h for testing or for other special purpose operation.

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC1197LP7FE knows which switch position on the VCO is optimum for the desired output frequency. The HMC1197LP7FE supports Auto-Calibration (AutoCal) of the step tuned VCO. The AutoCal fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 36.Note how the tuning voltage stays in a narrow range over a wide range of output frequencies such as fast frequency hopping.

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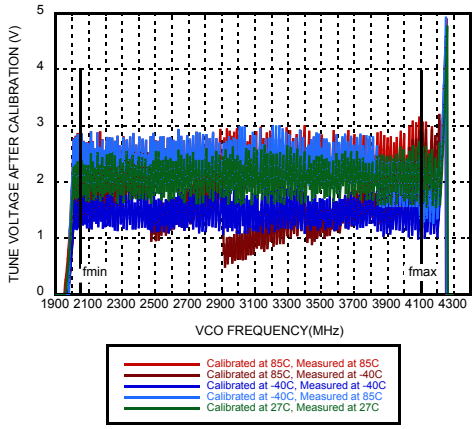

Figure 36. Typical VCO Tuning Voltage After Calibration

The calibration is normally run automatically once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally have to be concerned about which switch setting is used for a given frequency as this is handled by the AutoCal routine. The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency, and ensures that the VCO will stay locked and perform well over it's full temperature range without additional calibration, regardless of the temperature that the VCO was calibrated at.

Auto-Calibration can also be disabled allowing manual VCO tuning. Refer to section 1.2.1.5 for a description of manual tuning.

1.2.1.2.2 Auto-reLock on Lock Detect Failure

It is possible by setting Reg 0Ah[17] to have the VCO subsystem automatically re-run the calibration routine and re-lock itself if Lock Detect indicates an unlocked condition for any reason. With this option the system will attempt to re-Lock only once.

1.2.1.3.3 VCO AutoCal on Frequency Change

Assuming Reg 0Ah[11]=*0*, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the AutoCal routine for any reason, at the same frequency, simply rewrite the frequency change with the same value and the AutoCal routine will execute again without changing final frequency.

1.2.1.4.4 VCO AutoCal Time & Accuracy

The VCO frequency is counted for T_{mmt}, the period of a single AutoCal measurement cycle.

$$T_{mmt} = T_{xtal} \cdot R \cdot 2^n \quad \text{(EQ 1)}$$

n — is set by Reg 0Ah[2:0] and results in measurement periods which are multiples of the PD period, $T_{xtal}R$.

R — is the reference path division ratio currently in use, Reg 02h

T_{xtal} — is the period of the external reference (crystal) oscillator.

The VCO AutoCal counter will, on average, expect to register N counts, rounded down (floor) to the nearest integer, every PD cycle.

N — is the ratio of the target VCO frequency, f_{vco}, to the frequency of the PD, f_{pd}, where N can

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be any rational number supported by the N divider.

N is set by the integer (N_{int} = Reg 03h) and fractional (N_{frac} = Reg 04h) register contents

$$N = N_{int} + N_{frac} / 2^{24} \quad \text{(EQ 2)}$$

The AutoCal state machine runs at the rate of the FSM clock, T_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$T_{FSM} = T_{xtal} \cdot 2^{m} \quad \text{(EQ 3)}$$

m is 0, 2, 4 or 5 as determined by Reg 0Ah[14:13]

The expected number of VCO counts, V, is given by

$$V = floor\ (N \cdot 2^{n}) \quad \text{(EQ 4)}$$

The nominal VCO frequency measured, f_{vcom}, is given by

$$f_{vcom} = V \cdot f_{xtal} / (2^{n} \cdot R) \quad \text{(EQ 5)}$$

where the worst case measurement error, f_{err} , is:

$$f_{err} \approx \pm f_{pd} / 2^{n+1} \quad \text{(EQ 6)}$$

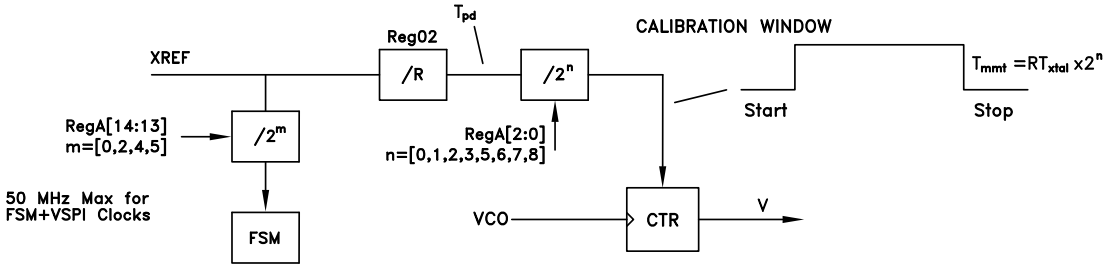

Figure 37. VCO Calibration

A 5-bit step tuned VCO, for example, nominally requires 5 measurements for calibration, worst case 6 measurements, and hence 7 VSPI data transfers of 20 clock cycles each. Total calibration time, worst case, is given by:

$$T_{cal} = k128T_{FSM} + 6T_{PD}\ 2^{n} + 7 \cdot 20T_{FSM} \quad \text{(EQ 7)}$$

or equivalently

$$T_{cal} = T_{xtal}\ (6R \cdot 2^{n} + (140+(3 \cdot 128)) \cdot 2^{m}) \quad \text{(EQ 8)}$$

For guaranteed hold of lock, across temperature extremes, the resolution should be better than 1/8th the frequency step caused by a VCO sub-band switch change. Better resolution settings will show no improvement.

1.2.1.4.1.1 VCO AutoCal Example

The HMC1197LP7FE must satisfy the maximum f_{pd} limited by the two following conditions:

a. N ≥ 16 (f_{int}), N ≥ 20.0 (f_{frac}), where N = f_{VCO}/ f_{pd}

b. f_{pd} ≤ 100 MHz

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Suppose the HMC1197LP7FE output frequency is to operate at 2.01 GHz. Our example crystal frequency is f_{xtal} = *50 MHz, R=1, and m=0 (*Figure 37*)*, hence T_{FSM} = 20 ns (50 MHz). Note, when using AutoCal, the maximum AutoCal Finite State Machine (FSM) clock cannot exceed 50 MHz (see Reg 0Ah[14:13]). The FSM clock does not affect the accuracy of the measurement, it only affects the time to produce the result. This same clock is used to clock the 16 bit VCO serial port.

If time to change frequencies is not a concern, then one may set the calibration time for maximum accuracy, and therefore not be concerned with measurement resolution.

Using an input crystal of 50 MHz (R=1 and fpd=50 MHz) the times and accuracies for calibration using (EQ 6) and (EQ 8) are shown in Table 10 Where minimal tuning time is 1/8th of the VCO band spacing.

Across all VCOs, a measurement resolution better than 800 kHz will produce correct results. Setting m = 0, n = 5, provides 781 kHz of resolution and adds 8.6 µs of AutoCal time to a normal frequency hop. Once the AutoCal sets the final switch value, 8.64 µs after the frequency change command, the fractional register will be loaded, and the loop will lock with a normal transient predicted by the loop dynamics. Hence as shown in this example that AutoCal typically adds about 8.6 µs to the normal time to achieve frequency lock. Hence, AutoCal should be used for all but the most extreme frequency hopping requirements.

Table 10. AutoCal Example with F_{xtal} = 50 MHz, R = 1, m = 0

Control Value *Reg0Ah[2:0]*	n	2^n	T_{mmt} (µs)	T_{cal} (µs)	F_{err} Max
0	0	1	0.02	4.92	± 25 MHz
1	1	2	0.04	5.04	± 12.5 MHz
2	2	4	0.08	5.28	± 6.25 MHz
3	3	8	0.16	5.76	± 3.125 MHz
4	5	32	0.64	8.64	± 781 kHz
5	6	64	1.28	12.48	± 390 kHz
6	7	128	2.56	20.16	± 195 kHz
7	8	256	5.12	35.52	± 98 kHz

1.2.1.5 Manual VCO Calibration for Fast Frequency Hopping

If it is desirable to switch frequencies quickly it is possible to eliminate the AutoCal time by calibrating the VCO in advance and storing the switch number vs frequency information in the host. This can be done by initially locking the HMC1197LP7FE on each desired frequency using AutoCal, then reading, and storing the selected VCO switch settings. The VCO switch settings are available inReg 15h[8:1] after every AutoCal operation. The host must then program the VCO switch settings directly when changing frequencies. Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when AutoCal is disabled. Hence frequency changes with manual control and AutoCal disabled, requires a minimum of two serial port transfers to the HMC1197LP7FE, once to set the VCO switches, and once to set the PLL frequency.

If AutoCal is disabled Reg 0Ah[11]=1, the VCO will update its registers with the value written via Reg 15h[8:1] immediately.

1.2.2 Registers required for Frequency Changes in Fractional Mode

A large change of frequency, in fractional mode (Reg 06h[11]=1), may require Main Serial Port writes to:

1. The integer register intg, Reg 03h *(only required if the integer part changes)*
2. Manual VCO Tuning Reg 15h only required for manual control of VCO if Reg 0Ah[11]=1 *(AutoCal disabled)*

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3. VCO Divide Ratio and Gain Register
   - Reg 16h[5:0] is required to change the VCO Output Divider value if needed.
   - Reg 16h[10:6] is required to change the Output Gain if needed.
4. The fractional register, Reg 04h. The fractional register write triggers AutoCal if Reg 0Ah[11]=0, and is loaded into the Delta Sigma modulator automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah[11]=1, the fractional frequency change is loaded into the Delta Sigma modulator immediately when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with AutoCal enabled (Reg 0Ah[11]=0), usually only require a single write to the fractional register. Worst case, 3 Main Serial Port transfers to the HMC1197LP7FE could be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, then the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register Reg 04h for frequency changes.

1.2.3 Registers Required for Frequency Changes in Integer Mode

A change of frequency, in integer mode (Reg 06h[11]=0), requires Main Serial Port writes to:

1. VCO register
   - Reg 15h only required for manual control of VCO if Reg 0Ah[11]=1 (AutoCal disabled)
   - Reg 16h is required to change the VCO Output Divider value if needed
2. The integer register Reg 03h.
   - In integer mode, an integer register write triggers AutoCal if Reg 0Ah[11]=0, and is loaded into the prescaler automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah[11]=1, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally changes to the integer register cause large steps in the VCO frequency, hence the VCO switch settings must be adjusted. AutoCal enabled is the recommended method for integer mode frequency changes. If AutoCal is disabled (Reg 0Ah[11]=1), a prior knowledge of the correct VCO switch setting and the corresponding adjustment to the VCO is required before executing the integer frequency change.

1.2.4 VCO Output Mute Function

The HMC1197LP7FE features an intelligent output mute function with the capability to disable the VCO output while maintaining the PLL and VCO subsystems fully functional. The mute function is automatically controlled by the HMC1197LP7FE, and provides a number of mute control options including:

1. Always mute (Reg 16h[5:0] = 0d). This mode is used for manual mute control.
2. Automatically mute the outputs during VCO calibration (Reg 17h[7] = 1) that occurs during output frequency changes.

This mode can be useful in eliminating any out of band emissions during freqeuncy changes, and ensuring that the system emits only desired frequencies. It is enabled by writing Reg 17h[7] = 1. Typical isolation when the HMC1197LP7FE is muted is always better than 60 dB, and is ~ 30 dB better than disabling the output buffers of the HMC1197LP7FE via Reg 17h[5:4].

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1.3 PLL Overview

1.3.1 Charge Pump (CP) & Phase Detector (PD)

The Phase detector (PD) has two inputs, one from the reference path divider and one from the RF path divider. When in lock these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. We refer to the frequency of operation of the PD as f_{pd}. Most formulae related to step size, delta-sigma modulation, timers etc., are functions of the operating frequency of the PD, f_{pd}. f_{pd} is also referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

1.3.1.1 Charge Pump

A simplified diagram of the charge pump is shown in Figure 38. The CP consists of 4 programmable current sources, two controlling the CP Gain (Up Gain Reg 09h[13:7], and Down Gain Reg 09h[6:0]) and two controlling the CP Offset, where the magnitude of the offset is set by Reg 09h [20:14], and the direction is selected by Reg 09h [21]=1 for up and Reg 09h [22]=1 for down offset.

CP Gain is used at all times, while CP Offset is only recommended for fractional mode of operation. Typically the CP Up and Down gain settings are set to the same value (Reg 09h[13:7] = Reg 09h[6:0]).

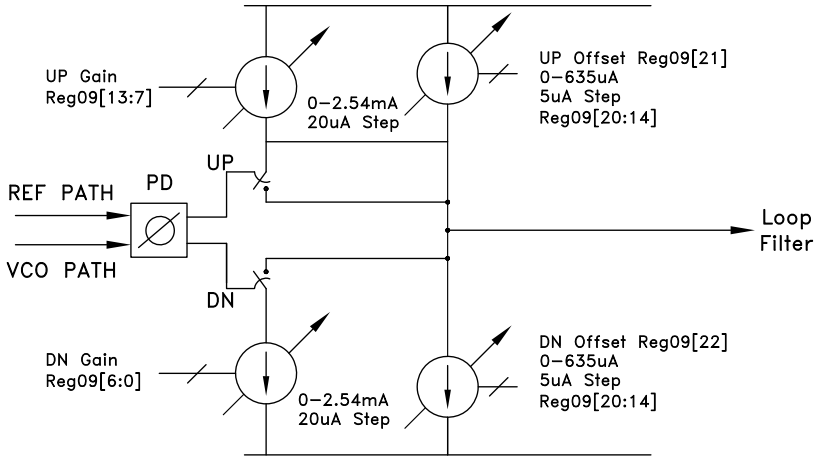

Figure 38. Charge Pump Gain & Offset Control

1.3.1.2 Charge Pump Gain

Charge pump Up and Down gains are set by Reg 09h[13:7] and Reg 09h[6:0] respectively. The current gain of the pump in Amps/radian is equal to the gain setting of this register divided by 2π.

Typical CP gain setting is set to 2 to 2.5 mA, however lower values can also be used. Values < 1 mA may result in degraded Phase Noise performance.

For example, if both Reg 09h[13:7] and Reg 09h[6:0] are set to '50d' the output current of each pump will be 1 mA and the phase frequency detector gain k_p = 1 mA/2π radians, or 159 µA/rad.

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1.3.1.3 Charge Pump Phase Offset

In Integer Mode, the phase detector operates with zero offset. The divided reference signal and the divided VCO signal arrive at the phase detector inputs at the same time. Integer mode does not require any CP Offset current. When operating in Integer Mode simply disable CP offset in both directions (Up and down), by writing Reg 09h[22:21] = '00'b and set the CP Offset magnitude to zero by writingReg 09h[20:14]= 0.

In Fractional Mode CP linearity is of paramount importance. Any non-linearity degrades phase noise and spurious performance.

In fractional mode, these non-linearities are eliminated by operating the PD with an average phase offset, either positive or negative (either the reference or the VCO edge always arrives first at the PD ie. leads).

A programmable CP offset current source is used to add DC current to the loop filter and create the desired phase offset. Positive current causes the VCO to lead, negative current causes the reference to lead.

The CP offset is controlled via Reg 09h[20:14]. The phase offset is scaled from 0 degrees, that is the reference and the VCO path arrive in phase, to 360 degrees, where they arrive a full cycle late.

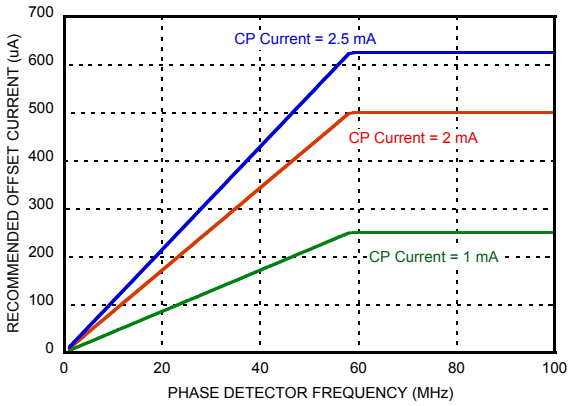
The specific level of charge pump offset current Reg 09h[20:14] is provided in (EQ 9). It is also plotted in Figure 39 vs. PD frequency for typical CP Gain currents.

$$\text{Required CP Offset} = \min\left[\left(4.3\times10^{-9}\times F_{PD}\times I_{CP}\right), 0.25\times I_{CP}\right] \quad \text{(EQ 9)}$$

where:

F_{PD}: Comparison frequency of the Phase Detector (Hz)

I_{CP}: is the full scale current setting (A) of the switching charge pump (set in Reg 09h[6:0], [13:7]



Recommended CP offset current vs PD frequency for typical CP gain currents. Calculated using (EQ 9)

The required CP offset current should never exceed 25 % of the programmed CP current. It is recommended to enable the Up Offset and disable the Down Offset by writing Reg 09h[22:21] = '10'b.

Operation with CP offset influences the required configuration of the Lock Detect function. Refer to the description of Lock Detect function in section 1.3.5.

When operating with PD frequency >=80MHz, the CP Offset current should be disabled for the frequency change and then re-enabled after the PLL has settled. If the CP Offset current is enabled during a frequency change it may not lock.

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1.3.1.4 Phase Detector Functions

Phase detector register Reg 0Bhallows manual access to control special phase detector features.

Setting Reg 0Bh[5] = 0, masks the PD up output, which prevents the charge pump from pumping up.`

Setting (Reg 0Bh[6]) = 0, masks the PD down output, which prevents the charge pump from pumping down.

Clearing both Reg 0Bh[5] and Reg 0Bh[6] tri-states the charge pump while leaving all other functions operating internally.

PD Force UP Reg 0Bh[9] = 1 and PD Force DN Reg 0Bh[10] = 1 allows the charge pump to be forced up or down respectively. This will force the VCO to the ends of the tuning range which can be useful in VCO testing.

1.3.2 Reference Input Stage

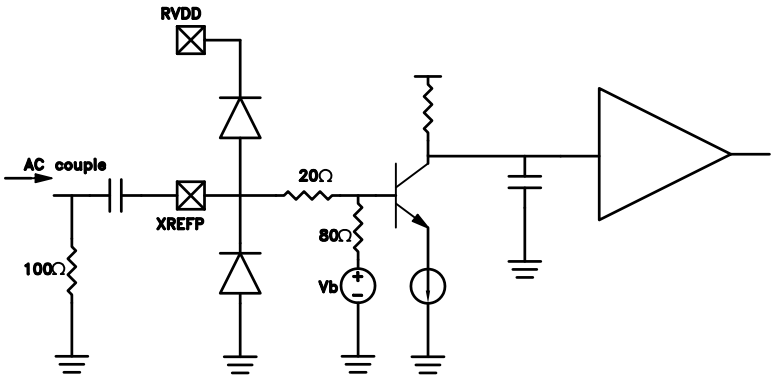

Figure 39. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation controlled by Reg 08h[21]. High Gain (Reg 08h[21] = 0), recommended below 200 MHz, and High frequency (Reg 08h[21] = 1), for 200 to 350 MHz operation. The buffer is internally DC biased, with 100 Ω internal termination. For 50 Ω match, an external 100 Ω resistor to ground should be added, followed by an AC coupling capacitor (impedance < 1 Ω), then to the XREFP pin of the part.

At low frequencies, a relatively square reference is recommended to keep the input slew rate high. At higher frequencies, a square or sinusoid can be used. The following table shows the recommended operating regions for different reference frequencies. If operating outside these regions the part will normally still operate, but with degraded reference path phase noise performance.

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