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1 dB LSB GaAs MMIC 3-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 6 GHz



Typical Applications

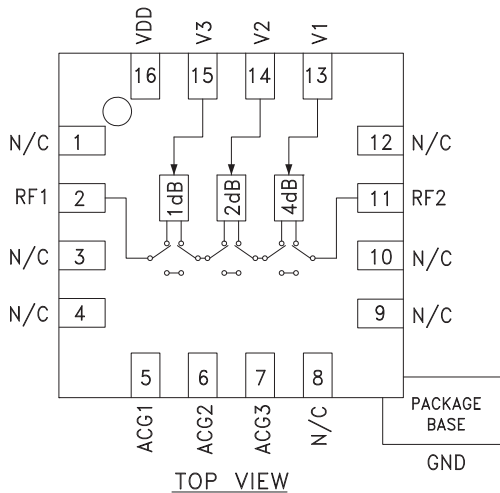
The HMC468LP3 / HMC468LP3E is ideal for:

- Cellular; UMTS/3G Infrastructure
- Fixed Wireless & WLL
- Microwave Radio & VSAT
- Test Equipment

Features

- 1 dB LSB Steps to 7 dB
- High IP3: +50 dBm
- ± 0.25 dB Typical Bit Error
- Single Control Line Per Bit
- Single +5V Supply
- 16 Lead 3x3mm SMT Package: 9mm²
- Included in the HMC-DK004 Designer's Kit

Functional Diagram



General Description

The HMC468LP3 & HMC468LP3E are broadband 3-bit GaAs IC digital attenuators in low cost leadless surface mount packages. Covering DC to 6.0 GHz, the insertion loss is less than 1 dB typical up to 4 GHz. The attenuator bit values are 1 (LSB), 2 and 4 dB for a total attenuation of 7 dB. Attenuation accuracy is excellent at ±0.4 dB typical step error with an IIP3 of +50 dBm. Three control voltage inputs, toggled between 0 and +5V, are used to select each attenuation state. A single Vdd bias of +5V is required.

Electrical Specifications, $T_A = +25^\circ C$, With $V_{dd} = +5V$ & $V_{ctl} = 0/+5V$

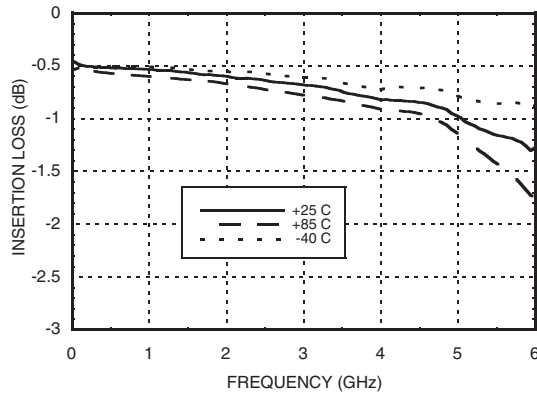
| Parameter | Frequency (GHz) | Min. | Typ. | Max. | Units |
|--|-----------------|----------------------------------|-----------------------------------|------|-------|
| Insertion Loss | DC - 2.5 GHz | | 0.7 | 1.0 | dB |
| | 2.5 - 4.5 GHz | | 0.9 | 1.3 | dB |
| | 4.5 - 6.0 GHz | | 1.3 | 1.8 | dB |
| Attenuation Range | DC - 6 GHz | | 7 | | dB |
| Return Loss (RF1 & RF2, All Atten. States) | DC - 4 GHz | | 20 | | dB |
| | 4.0 - 6.0 GHz | | 15 | | dB |
| Attenuation Accuracy: (Referenced to Insertion Loss) | All States | DC - 2.5 GHz | ± 0.2 + 2% of Atten. Setting Max. | | dB |
| | 1 - 4 dB States | 2.5 - 6.0 GHz | ± 0.3 + 3% of Atten. Setting Max. | | dB |
| | 5 - 7 dB States | 2.5 - 6.0 GHz | ± 0.4 + 4% of Atten. Setting Max. | | dB |
| Input Power for 0.1 dB Compression | 0.25 - 6.0 GHz | | 20 | | dBm |
| Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone) | 0.25 - 6.0 GHz | | 50 | | dBm |
| Switching Characteristics | DC - 6 GHz | | | | |
| | | tRISE, tFALL (10/90% RF) | | 110 | ns |
| | | tON, tOFF (50% CTL to 10/90% RF) | | 135 | ns |

* Bypass capacitor connecting ACG1, ACG2 & ACG3 to RF ground required per pin description herein.

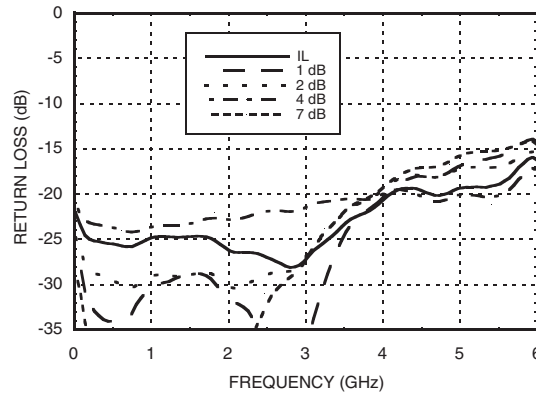


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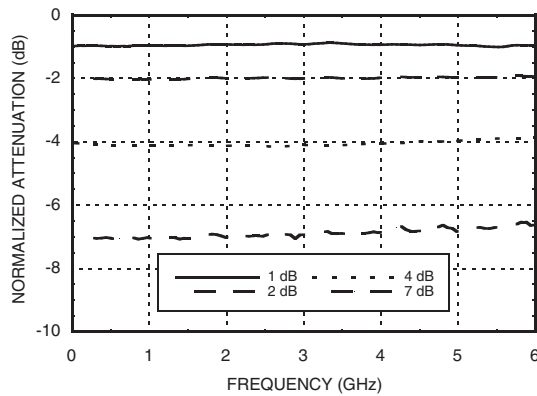
Insertion Loss



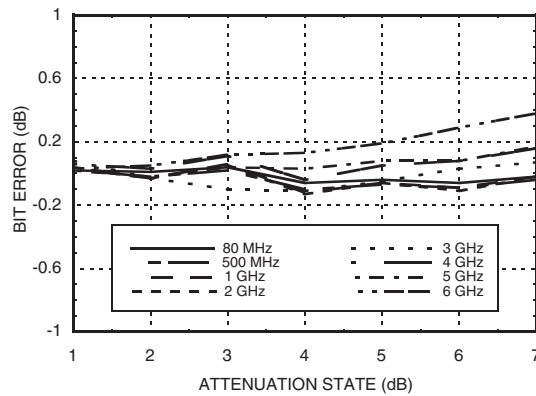
Return Loss RF1, RF2
(Only Major States are Shown)



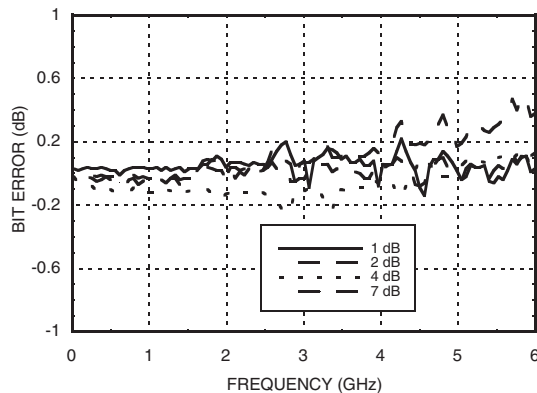
Normalized Attenuation
(Only Major States are Shown)



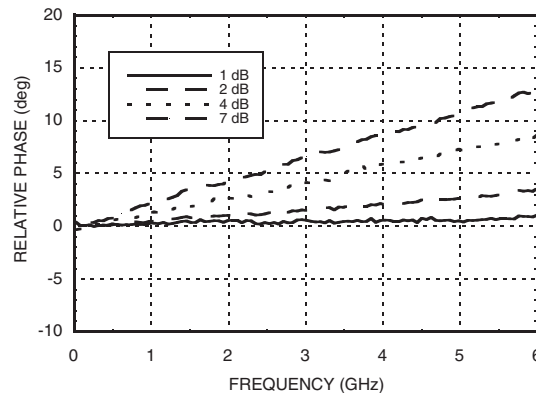
Bit Error vs. Attenuation State



Bit Error vs. Frequency
(Only Major States are Shown)



Relative Phase vs. Frequency
(Only Major States are Shown)



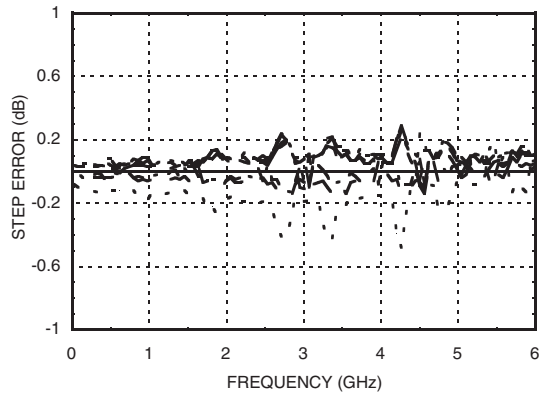
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**Worst Case Step Error
Between Successive Attenuation States**



Truth Table

| Control Voltage Input | | | Attenuation Setting RF1 - RF2 |
|-----------------------|------------|------------|----------------------------------|
| V1 4 dB | V2 2 dB | V3 1 dB | |
| High | High | High | Reference I.L. |
| High | High | Low | 1 dB |
| High | Low | High | 2 dB |
| Low | High | High | 4 dB |
| Low | Low | Low | 7 dB |

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

Bias Voltage & Current

| Vdd Range= +5.0 Vdc ± 10% | | |
|---------------------------|--------------------|--------------------|
| Vdd (Vdc) | Idd (Typ.) (mA) | Idd (Max.) (mA) |
| +5.0 | 1.05 | 1.8 |

TTL/CMOS Control Voltages

| State | Bias Condition |
|-------|-------------------------------|
| Low | 0 to 0.8 Vdc @ -5 uA Typ. |
| High | +2.0 to +5.0 Vdc @ 40 uA Typ. |



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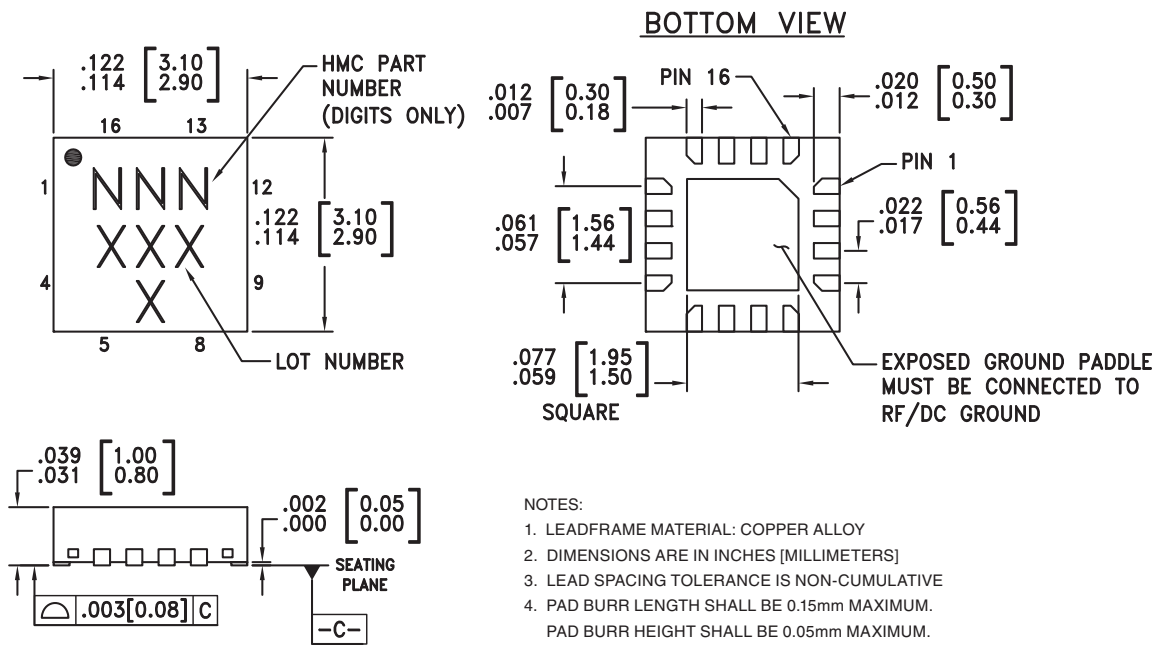
Absolute Maximum Ratings

| | |
|----------------------------|------------------------|
| Control Voltage (V1 to V3) | -0.5 Vdc to Vdd +1 Vdc |
| Bias Voltage (Vdd) | +7 Vdc |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| RF Input Power | +30 dBm |
| ESD Sensitivity (HBM) | Class 1A |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC468LP3 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 ^[1] | 468 XXXX |
| HMC468LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | 468 XXXX |

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX



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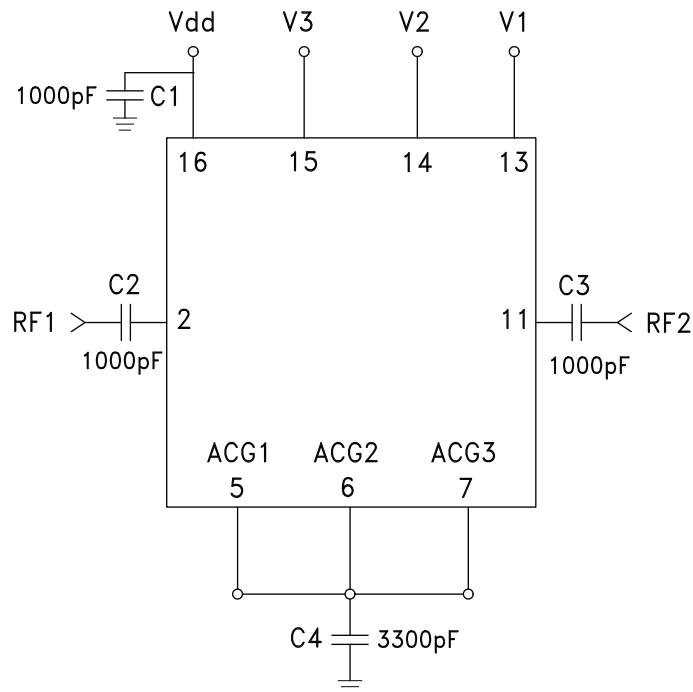
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ATTENUATORS - SMT

Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|-----------------------|-------------|---|---------------------|
| 1, 3, 4, 8, 9, 10, 12 | N/C | These pins should be connected to PCB RF ground to maximize performance. | |
| 2, 11 | RF1, RF2 | This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required | |
| 13 - 15 | V1 - V3 | See truth table and control voltage table. | |
| 5 - 7 | ACG1 - ACG3 | External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. | |
| 16 | Vdd | Supply Voltage | |
| | GND | Package bottom has an exposed metal paddle that must be connected to RF/DC ground. | |

Application Circuit



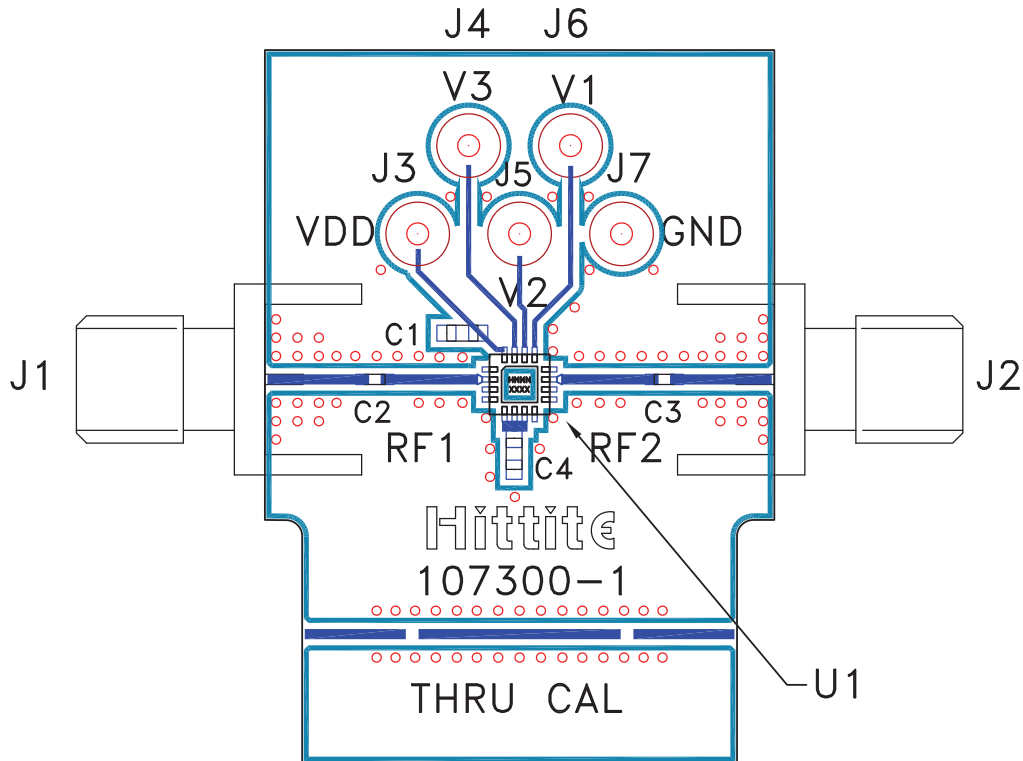
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Evaluation PCB



List of Materials for Evaluation PCB 107302 [1]

| Item | Description |
|---------|---|
| J1 - J2 | PCB Mount SMA Connector |
| J3 - J7 | DC Pin |
| C1 | 1000 pF Capacitor, 0603 Pkg. |
| C2, C3 | 100 pF Capacitor, 0402 Pkg. |
| C4 | 3300 pF Capacitor, 0603 Pkg. |
| U1 | HMC468LP3 / HMC468LP3E Digital Attenuator |
| PCB [2] | 107300 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.