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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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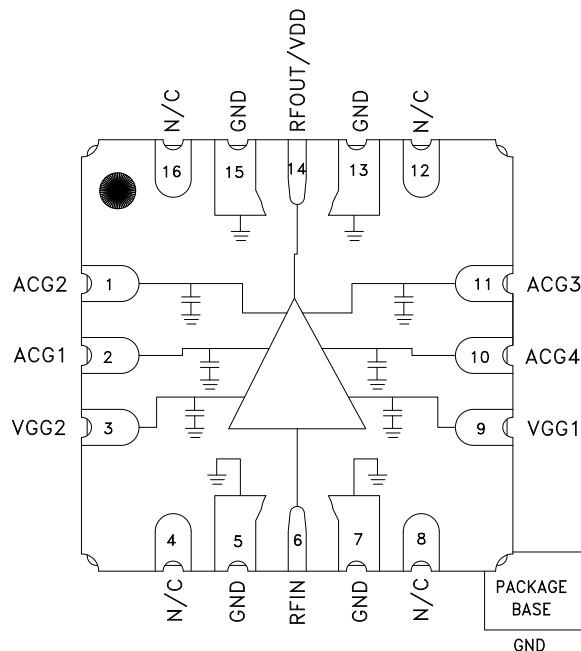
GaAs pHEMT MMIC 0.25 WATT POWER AMPLIFIER DC - 40 GHz

Typical Applications

The HMC5805LS6 is ideal for:

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Diagram



Features

- High P1dB Output Power: 22 dBm
- High Psat Output Power: 24 dBm
- High Gain: 13.5 dB
- High Output IP3: 33 dBm
- Supply Voltage: +10 V @ 175 mA
- 16 Lead Ceramic 6x6 mm SMT Package: 36 mm²

General Description

The HMC5805LS6 is a GaAs pHEMT MMIC Distributed Power Amplifier which operates between DC and 40 GHz. The amplifier provides 13 dB of gain, 33 dBm output IP3 and +22 dBm of output power at 1 dB gain compression while requiring 175 mA from a +10 V supply. The HMC5805LS6 exhibits a slightly positive gain slope from 8 to 32 GHz, making it ideal for EW, ECM, Radar and test equipment applications. The HMC5805LS6 amplifier I/Os are internally matched to 50 Ohms and the 6x6 mm SMT package is well suited for automated assembly techniques.

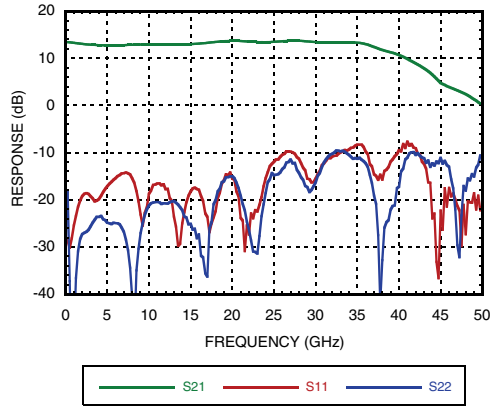
Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{dd} = +10\text{V}$, $V_{gg2} = +3.5\text{V}$, $I_{dd} = 175\text{mA}^*$

| Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
|---|---------|-------|------|---------|------|------|---------|------|------|-------|
| Frequency Range | DC - 12 | | | 12 - 35 | | | 35 - 40 | | | GHz |
| Gain | 11 | 13 | | 11.5 | 13.5 | | 7 | 10 | | dB |
| Gain Flatness | | ±0.35 | | | ±0.5 | | | ±1.0 | | dB |
| Gain Variation Over Temperature | | 0.02 | | | 0.03 | | | 0.05 | | dB/°C |
| Input Return Loss | | 18 | | | 15 | | | 12 | | dB |
| Output Return Loss | | 24 | | | 13 | | | 11 | | dB |
| Output Power for 1 dB Compression (P1dB) | 20 | 22 | | 19 | 21 | | 16 | 19 | | dBm |
| Saturated Output Power (Psat) | | 24 | | | 23.5 | | | 21 | | dBm |
| Output Third Order Intercept (IP3) | | 33 | | | 31 | | | 27 | | dBm |
| Noise Figure | | 4.5 | | | 4 | | | 7 | | dB |
| Supply Current (Idd) (Vdd= 10V, Vgg1= -0.8V Typ.) | | 175 | | | 175 | | | 175 | | mA |

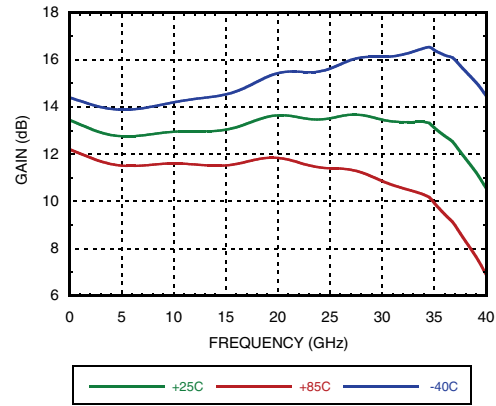
* Adjust Vgg1 between -2 to 0 V to achieve Idd = 175 mA typical.

GaAs pHEMT MMIC 0.25 WATT POWER AMPLIFIER DC - 40 GHz

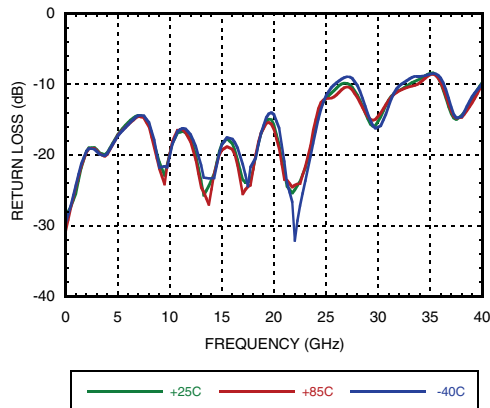
Gain & Return Loss



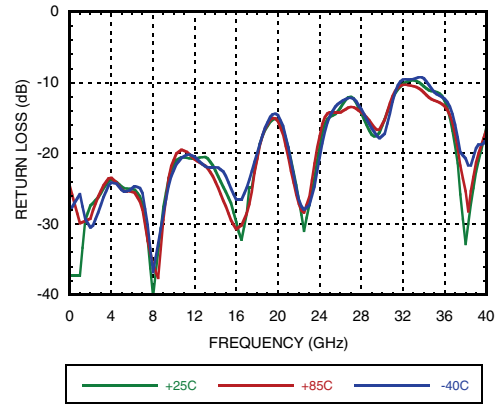
Gain vs. Temperature



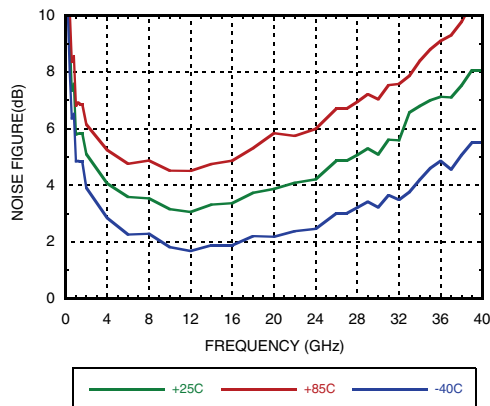
Input Return Loss vs. Temperature



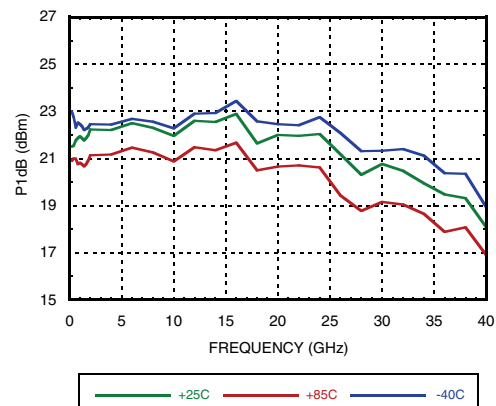
Output Return Loss vs. Temperature



Noise Figure vs. Temperature

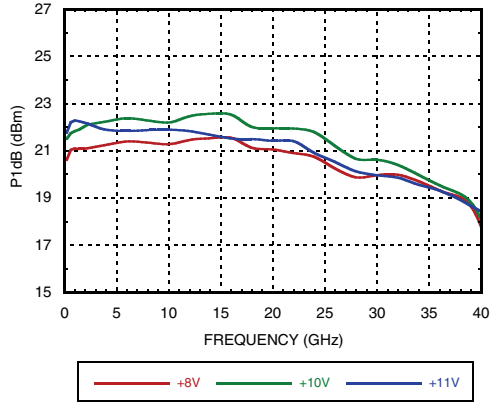


P1dB vs. Temperature

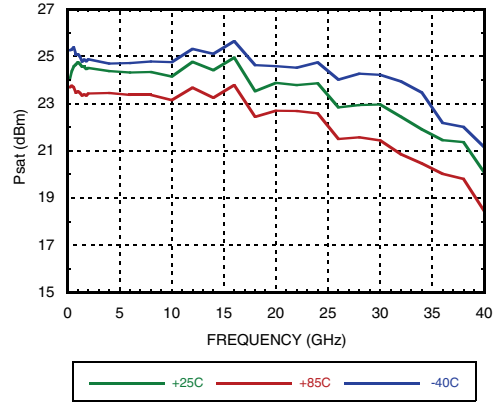


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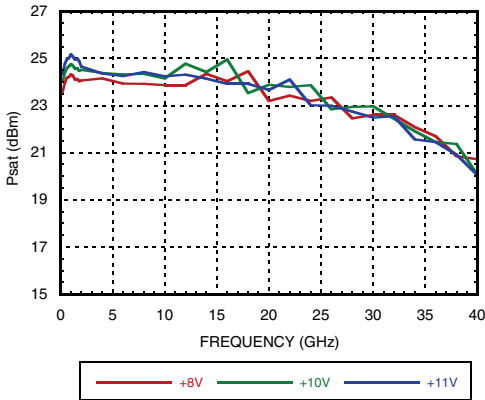
P1dB vs. Supply Voltage



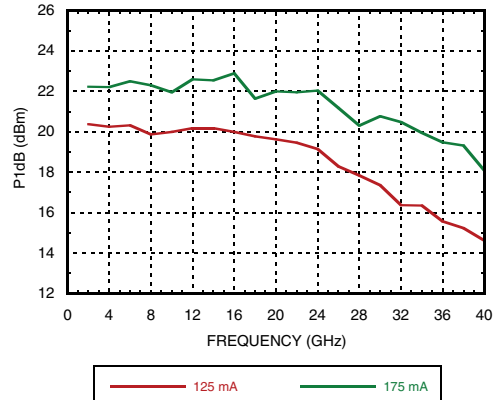
Psat vs. Temperature



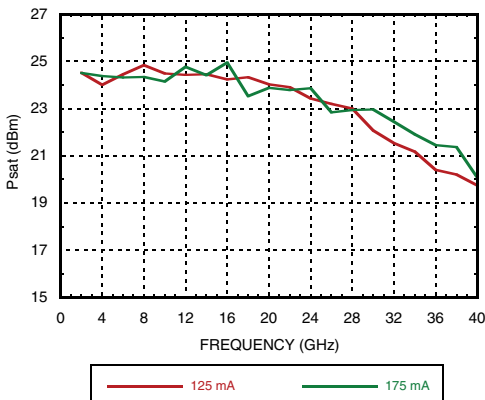
Psat vs. Supply Voltage



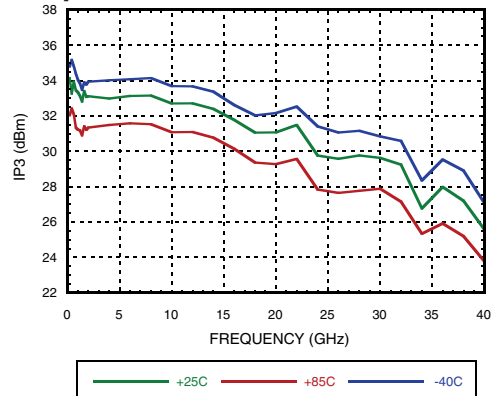
P1dB vs. Supply Current



Psat vs. Supply Current

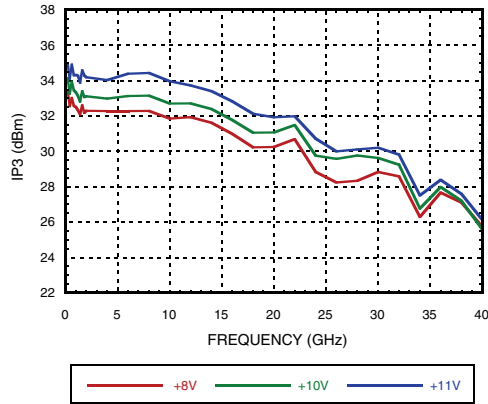


Output IP3 vs. Temperature @ Pout=12 dBm / Tone

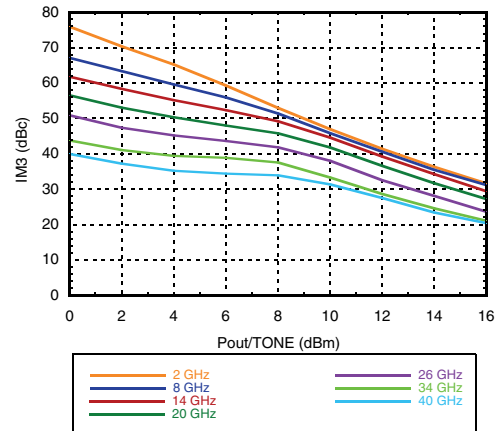


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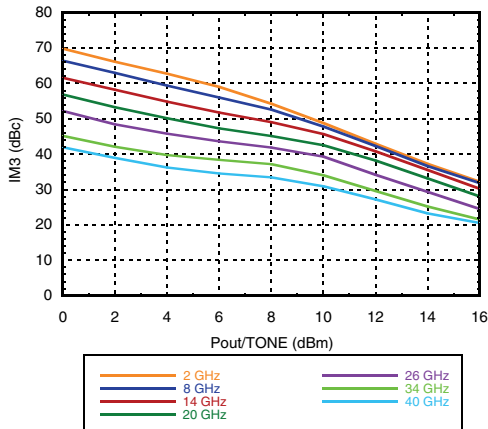
**Output IP3 vs. Supply Voltage
@ Pout=12 dBm / Tone**



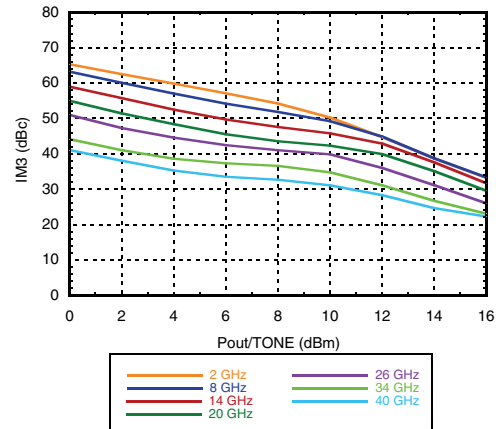
Output IM3 @ Vdd=+8V



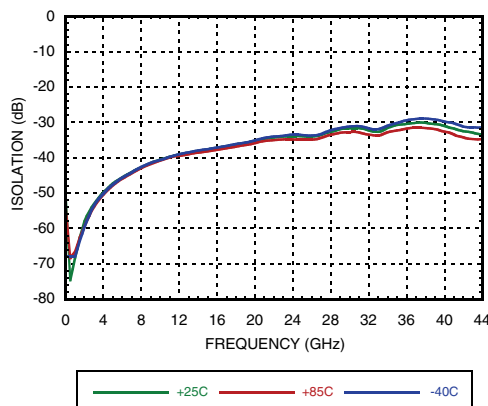
Output IM3 @ Vdd=+10V



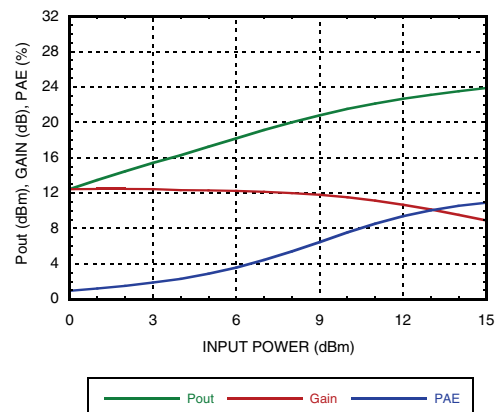
Output IM3 @ Vdd=+11V



Reverse Isolation vs. Temperature

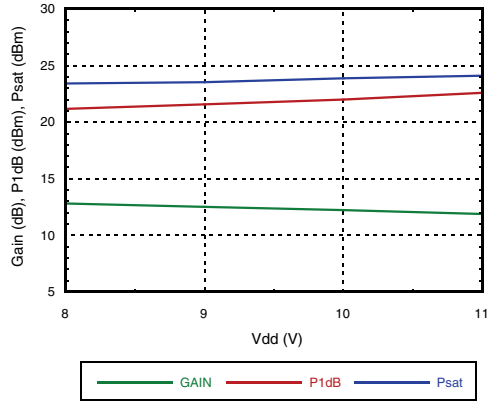


Power Compression @ 20GHz

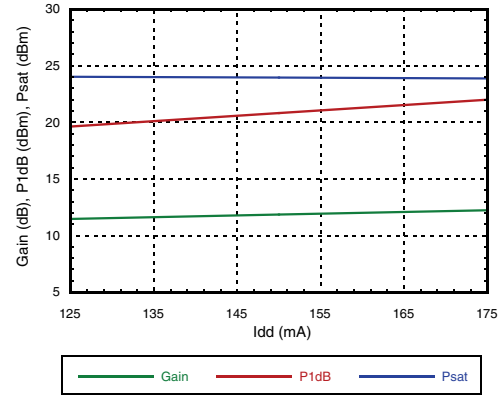


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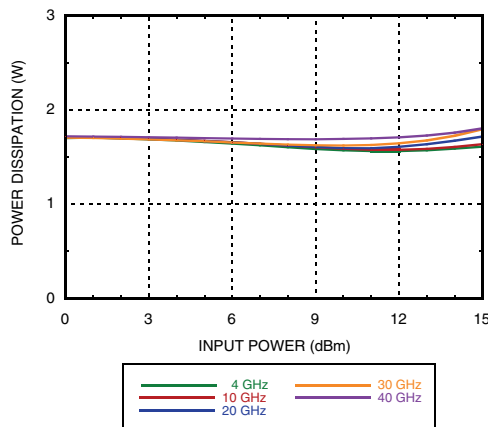
Gain and Power vs. Supply Voltage



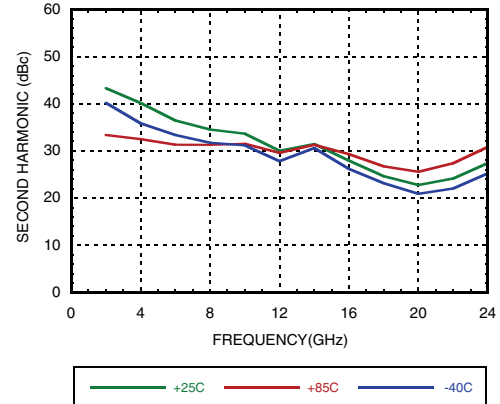
Gain and Power vs. Supply Current



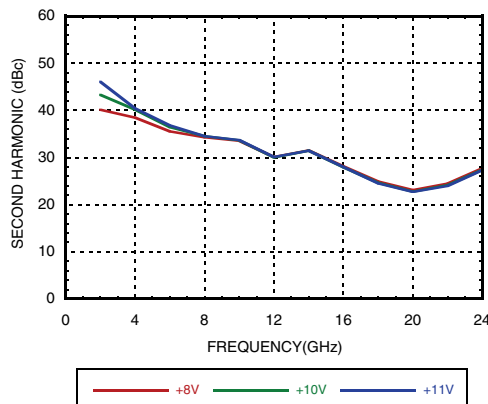
Power Dissipation



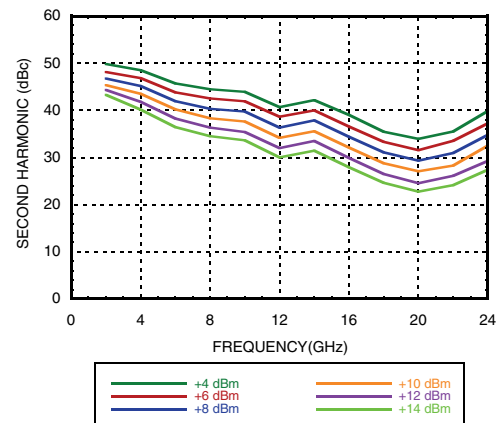
Second Harmonics vs. Temperature @ Pout=14 dBm



Second Harmonics vs. Vdd @ Pout=14 dBm



Second Harmonics vs. Pout



GaAs pHEMT MMIC 0.25 WATT POWER AMPLIFIER DC - 40 GHz

Absolute Maximum Ratings

| | |
|--|--|
| Drain Bias Voltage (Vdd) | 12V |
| Gate Bias Voltage (Vgg1) | -3 to 0 Vdc |
| Gate Bias Voltage (Vgg2) | For Vdd = 12V, Vgg2 = 5.5V Idd >145mA For Vdd between 8.5V to 11V, Vgg2 = (Vdd - 6.5V) up to 4.5V For Vdd < 8.5V, Vgg2 must remain > 2V |
| RF Input Power (RFIN) | 17 dBm |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T= 85 °C) (derate 69 mW/°C above 85 °C) | 2.1 W |
| Thermal Resistance (channel to ground paddle) | 31.1 °C/W |
| Output Power into VSWR >7:1 | 24 dBm |
| Storage Temperature | -65 to 150 °C |
| Operating Temperature | -40 to 85 °C |
| ESD Sensitivity (HBM) | Class 0 Passed 150V |

Typical Supply Current vs. Vdd

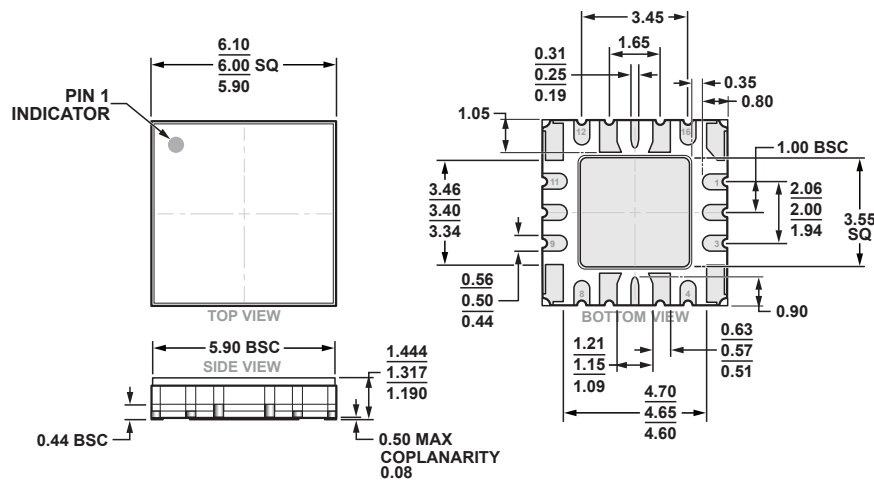
| Vdd (V) | Idd (mA) |
|---------|----------|
| +9 | 175 |
| +10 | 175 |
| +11 | 175 |

Note: Amplifier will operate over full voltage ranges shown above. Vgg adjusted to achieve Idd = 175 mA.



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]
Dimensions shown in millimeters

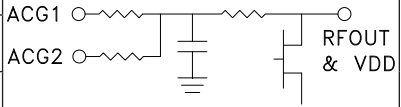
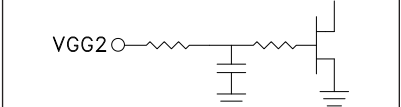
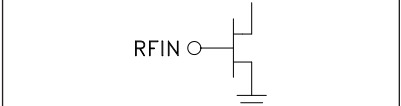
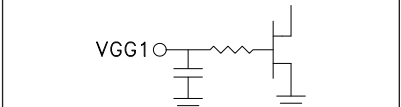
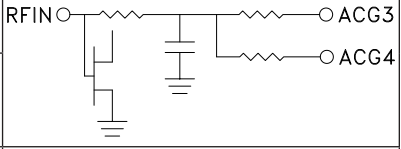
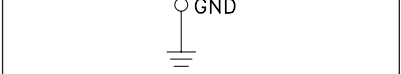
Table 1. Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Option | Package Marking ^[1] |
|--------------|-----------------------|------------------|------------|----------------|--------------------------------|
| HMC5805LS6 | ALUMINA, WHITE | Gold over Nickel | N/A | EP-16-2 | H5805 XXXX |
| HMC5805LS6TR | ALUMINA, WHITE | Gold over Nickel | N/A | EP-16-2 | H5805 XXXX |

[1] 4-Digit lot number XXXX

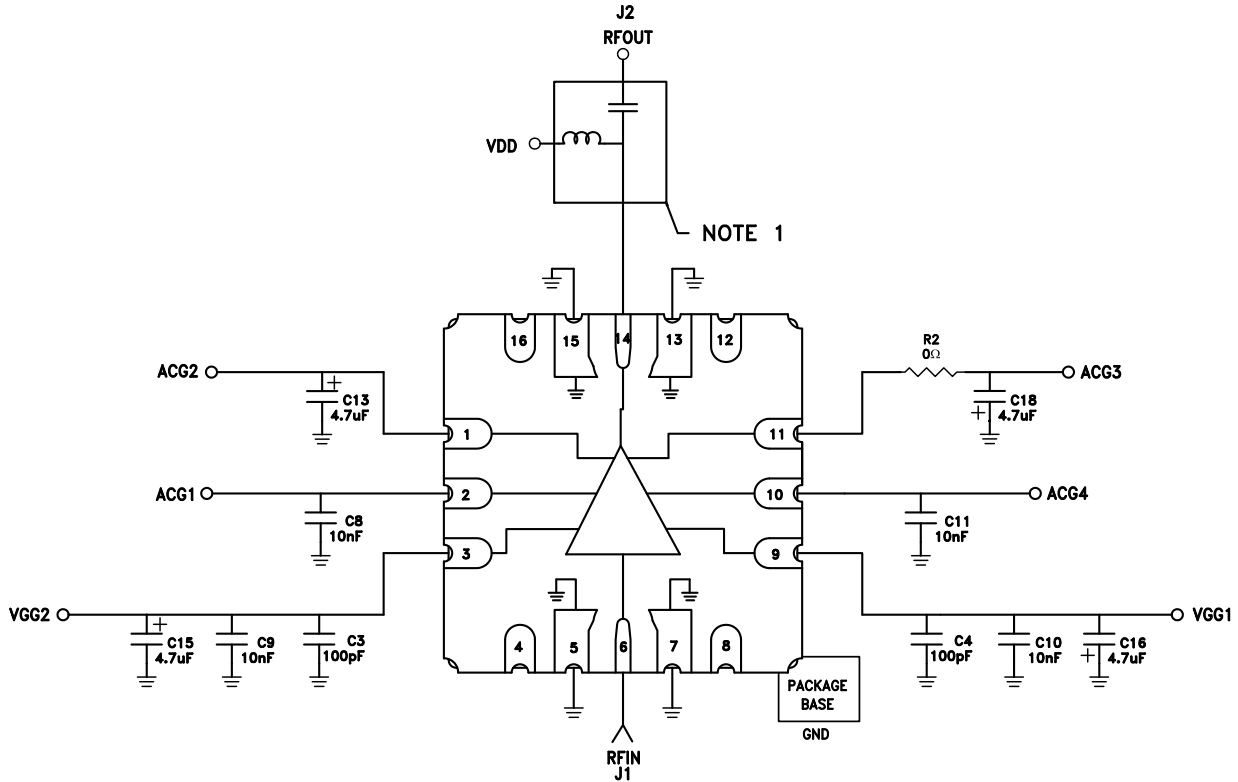
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Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|--------------|-------------|---|---|
| 1, 2, 14 | ACG2 | Low frequency termination. Attach bypass capacitor per application circuit herein. |  |
| | ACG1 | Low frequency termination. Attach bypass capacitor per application circuit herein. | |
| | RFOUT & VDD | RF output for amplifier. Connect DC bias (VDD) network to provide drain current (I _{dd}). See application circuit herein. | |
| 3 | VGG2 | Gate control 2 for amplifier. Attach bypass capacitors per application circuit herein. For normal operation +3.5V should be applied to Vgg2. |  |
| 6 | RFIN | This pin is DC coupled and matched to 50 Ohms. Blocking capacitor is required. |  |
| 9 | VGG1 | Gate control 1 for amplifier. Attach bypass capacitors per application circuit herein. Please follow "MMIC Amplifier Biasing Procedure" application note. |  |
| 10 | ACG4 | Low frequency termination. Attach bypass capacitor per application circuit herein. |  |
| 11 | ACG3 | Low frequency termination. Attach bypass capacitor per application circuit herein. | |
| 5, 7, 13, 15 | GND | These pins and exposed ground paddle must be connected to RF/DC ground. |  |
| 4, 8, 12, 16 | N/C | These pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |

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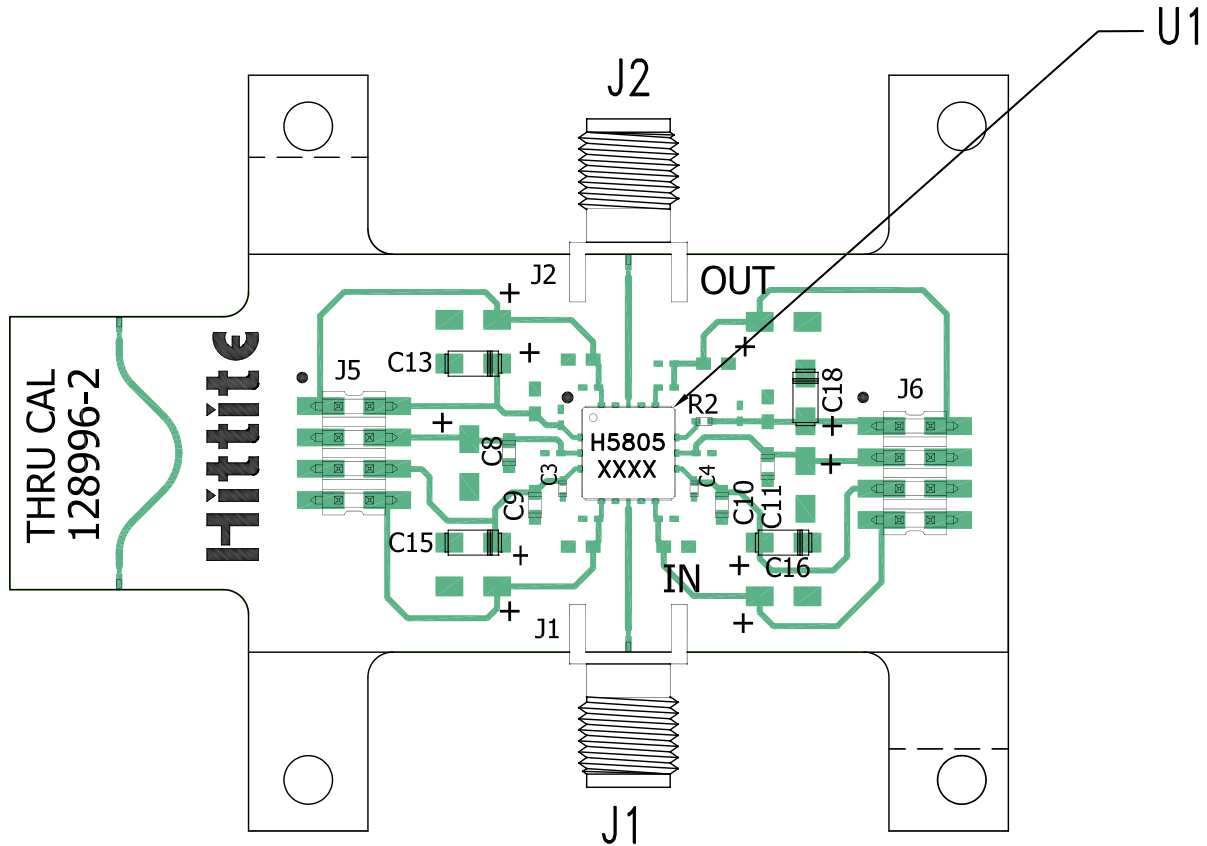
Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee with low series resistance and capable of providing 250 mA

**GaAs pHEMT MMIC 0.25 WATT POWER AMPLIFIER
DC - 40 GHz**

Evaluation PCB



List of Materials for Evaluation 132033-HMC5805LS6 [1]

| Item | Description |
|--------------------|--------------------------------|
| J1, J2 | PCB Mount K Connectors, SRI |
| J5, J6 | DC Pins |
| C3, C4 | 100 pF Capacitors, 0402 Pkg. |
| C8 - C11 | 0.01 μF Capacitors, 0603 Pkg. |
| C13, C15, C16, C18 | 4.7 μF Capacitors, Case A Pkg. |
| R2 | Zero Ohm Resistor, 0402 Pkg. |
| U1 | HMC5805LS6 Amplifier |
| PCB [2] | 128996 Evaluation PCB |

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices upon request.

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

**GaAs pHEMT MMIC 0.25 WATT POWER AMPLIFIER
DC - 40 GHz****Notes**