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60 GHz Millimeterwave Transmitter, 57 GHz to 64 GHz

Data Sheet **HMC6300**

FEATURES

- Frequency band: 57 GHz to 64 GHz
- RF signal bandwidth: up to 1.8 GHz
- Output power for 1 dB compression: 15 dBm
- Gain: 5 dB to 35 dB
- Digital and analog RF and IF gain control
- Integrated frequency synthesizer
- Integrated image reject filter
- Partially external loop filter
- Support for external local oscillator (LO)
- On-chip temperature sensor
- Support for 256 QAM modulation
- Integrated minimum shift keying (MSK) modulator
- Universal analog I/Q baseband interface
- 3-wire serial digital interface
- 65-ball, RoHS compliant, wafer level ball grid array

APPLICATIONS

- Small cell backhaul
- 60 GHz industrial, scientific, and medical (ISM) band data transfer
- Multiple Gbps data communication
- WiGig/802.11ad radio
- High definition video transmission
- Radar/high resolution imaging

GENERAL DESCRIPTION

The HMC6300 is a complete millimeterwave transmitter integrated circuit in a 6 mm × 4 mm RoHS compliant wafer level ball grid array (WLBGA) that operates from 57 GHz to 64 GHz with up to 1.8 GHz modulation bandwidth.

An integrated synthesizer provides tuning in 250 MHz, 500 MHz, or 540 MHz steps with excellent phase noise to support up to 64 QAM modulation. Optionally, an external LO can be injected allowing for user selectable LO characteristics or phase coherent transmit and receive operation, as well as modulation up to 256 QAM. Support for a wide variety of modulation formats is provided through a universal analog baseband I/Q interface. The transmitter chip optionally supports dedicated frequency-shift keying (FSK), minimum shift keying (MSK), and on-off keying (OOK) modulation formats for lower cost and lower power serial data links without the need for high speed data converters.

A differential output provides up to 15 dBm linear output power into a 100 Ω load. Single-ended operation is also supported up to 12 dBm. Together with the HMC6301, a complete 60 GHz transceiver chipset is provided for multiple Gbps operation in the unlicensed 60 GHz ISM band.

FUNCTIONAL BLOCK DIAGRAM

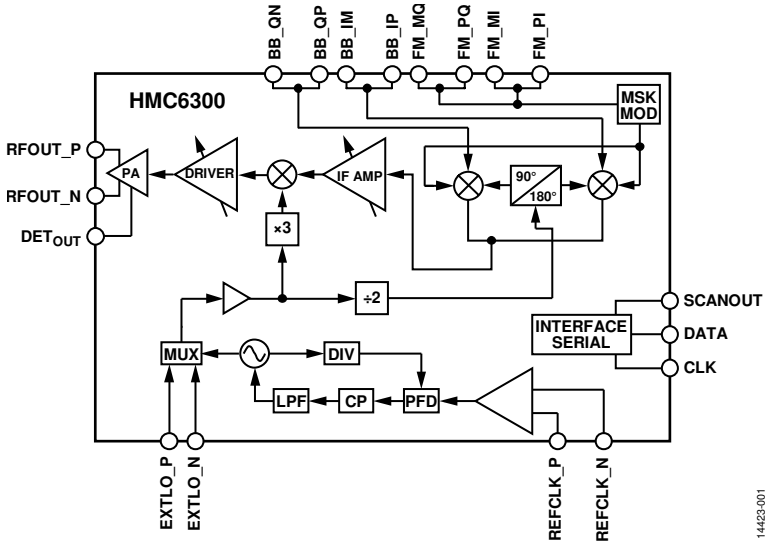

Figure 1.

Rev. B

Document Feedback

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- HMC6300 Evaluation Board

DOCUMENTATION

Data Sheet

- HMC6300: 60 GHz Millimeterwave Transmitter, 57 GHz to 64 GHz Data Sheet

User Guides

- UG-1031: Getting Started with the EK1HMC6350 Evaluation Kit and Software

DESIGN RESOURCES

- HMC6300 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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REVISION HISTORY

12/2016—Rev. A to Rev. B

Changes to Figure 11 and Figure 14 ... 11
Changes to Ordering Guide ... 25

9/2016—v00.0716 to Rev. A

Updated Format ... Universal
Added Minimum Gain Parameter, Table 1 ... 3
Changes to Recommended Operating Conditions, Table 3 ... 5
Changes to Figure 17 ... 14
Added Ordering Guide Section ... 25

7/2016—Revision v00.0716: Initial Version

SPECIFICATIONS

T_A = 25°C, reference frequency = 71.4286 MHz, IF bandwidth = maximum, input impedance = 100 Ω differential, output impedance = 100 Ω differential, input signal level (high modulator gain) = −36 dBm on each of the four baseband inputs, power amplifier configuration is differential, unless otherwise noted.

ELECTRICAL SPECIFICATIONS, 57 GHz TO 63 GHz

Table 1. Electrical Specifications, 57 GHz to 63 GHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY STEP SIZE	With 71.4286 MHz reference clock		250		MHz
	With 142.857 MHz reference clock		500		MHz
	With 154.2857 MHz reference clock		540		MHz
MODULATION BANDWIDTH	Full I/Q bandwidth		1.8		GHz
GAIN					
Minimum Gain			5		dB
Maximum Gain		32.5	35		dB
Modulator Gain Control	High and low gain settings		9		dB
IF Gain Control			14		dB
RF Gain Control			22		dB
OUTPUT POWER					
Output Power for 1 dB Compression (P1dB)	Balanced into 100 Ω		15		dBm
Saturated Output Power (P_{SAT})	Balanced into 100 Ω	13.9	17		dBm
Output Power for 1 dB Compression (P1dB)	Singled-ended into 50 Ω		12		dBm
Saturated Output Power (P_{SAT})	Singled-ended into 50 Ω		14		dBm
Detector Power Range			−10 to +15		dBm
TEMPERATURE SENSOR RANGE	Four levels	−40		+85	°C
SUPPRESSION AND REJECTION					
Sideband Suppression		15	30		dBc
Image Rejection			40		dBc
LO Suppression	At 6/7 of RF carrier frequency (3 × LO)	10	20		dBc
Carrier Suppression	Without calibration		30		dBc
PHASE					
Phase Noise					
@ 100 kHz Offset			−75		dBc/Hz
@ 1 MHz Offset			−93		dBc/Hz
@ 10 MHz Offset			−114		dBc/Hz
@ 100 MHz Offset			−122		dBc/Hz
Phase-Locked Loop (PLL) Bandwidth	Using internal filter		300		kHz
POWER DISSIPATION					
Balanced			1.0		W
Single-Ended			0.88		W
Balanced, External LO			0.75		W

ELECTRICAL SPECIFICATIONS, 63 GHz TO 64 GHz

Table 2. Electrical Specifications, 63 GHz to 64 GHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY STEP SIZE	With 71.4286 MHz reference clock		250		MHz
	With 142.857 MHz reference clock		500		MHz
	With 154.2857 MHz reference clock		540		MHz
MODULATION BANDWIDTH	Full I/Q bandwidth		1.8		GHz
GAIN					
Maximum Gain		30.5	32		dB
Modulator Gain Control	High and low gain settings		9		dB
IF Gain Control			14		dB
RF Gain Control			22		dB
OUTPUT POWER					
Output Power for 1 dB Compression (P1dB)	Balanced into 100 Ω		15		dBm
Saturated Output Power (P_{SAT})	Balanced into 100 Ω	13.9	17		dBm
Output Power for 1 dB Compression (P1dB)	Singled-ended into 50 Ω		12		dBm
Saturated Output Power(P_{SAT})	Singled-ended into 50 Ω		14		dBm
Detector Power			−10 to +15		dBm
TEMPERATURE SENSOR RANGE	Four levels	−40		+85	°C
SUPPRESSION AND REJECTION					
Sideband Suppression		15	30		dBc
Image Rejection			40		dBc
LO Suppression	At 6/7 of RF carrier frequency (3 × LO)	10	20		dBc
Carrier Suppression	Without calibration		30		dBc
PHASE					
Phase Noise @ 100 kHz Offset			−75		dBc/Hz
Phase Noise @ 1 MHz Offset			−93		dBc/Hz
Phase Noise @ 10 MHz Offset			−114		dBc/Hz
Phase Noise @ 100 MHz Offset			−122		dBc/Hz
PLL Bandwidth	Using internal filter		300		kHz
POWER DISSIPATION					
Balanced			1.0		W
Single-Ended			0.88		W
Balanced, External LO)			0.75		W

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Power Amplifier	VCC_{PAN}, VCC_{PAP}	3.9	4	4.1	V dc
	VDD_{PA}	2.565	2.7	2.835	V dc
Driver	VCC_{DRV}	2.565	2.7	2.835	V dc
Divider	VCC_{DIV}	2.565	2.7	2.835	V dc
Mixer	VCC_{MIX}	2.565	2.7	2.835	V dc
Intermediate Frequency	VCC_{IF}	2.565	2.7	2.835	V dc
Radio Frequency Variable Gain Amplifier	VCC_{RFVGA}	2.565	2.7	2.835	V dc
Tripler	VCC_{TRIP}	2.565	2.7	2.835	V dc
VCO	VCC_{VCO}	2.565	2.7	2.835	V dc
Digital Circuit	VDD_{D}	1.3	1.35	1.48	V dc
Synthesizer	VDD_{SYN}	1.3	1.35	1.48	V dc
INPUT VOLTAGE RANGE					
Serial Digital Interface	DATA, ENABLE, CLK, RESET				
Logic High		0.9	1.2	1.4	V
Logic Low		−0.05	+0.1	+0.3	V
REFERENCE CLOCK					
Reference Clock, Positive	REFCLK_P		3.3 V or 2.5 V LVPECL/LVDS,		V
			1.2 V CMOS		V
Reference Clock, Negative	REFCLK_N		3.3 V or 2.5 V LVPECL/LVDS,		V
			1.2 V CMOS		V
BASEBAND I/Q					
In-Phase Baseband Input					
Negative	BB_IM	5	100	750	mV p-p
Positive	BB_IP	5	100	750	mV p-p
Quadrature Baseband Input					
Negative	BB_QN	5	100	750	mV p-p
Positive	BB_QP	5	100	750	mV p-p
BASEBAND I/Q, COMMON MODE					
In-Phase Baseband Input					
Negative	BB_IM		1.6		V
Positive	BB_IP		1.6		V
Quadrature Baseband Input					
Negative	BB_QN		1.6		V
Positive	BB_QP		1.6		V
MSK DATA					
MSK In-Phase Input					
Negative (Minus)	FM_MI	200	500	750	mV p-p
Positive	FM_PI	200	500	750	mV p-p
MSK Quadrature Input					
Negative (Minus)	FM_MQ	200	500	750	mV p-p
Positive	FM_PQ	200	500	750	mV p-p
MSK COMMON MODE			1.1		V
ANALOG GAIN CONTROL					
RF Variable Gain Amplifier	ANA_{RFVGA}	0.1	1.1	2.5	V
IF Variable Gain Amplifier	ANA_{IFVGA}	0.1	1.1	2.5	V
EXTERNAL LO					
Positive	EXTLO_P	0	3	5	dBm
Negative	EXTLO_N	0	3	5	dBm

Parameter	Symbol	Min	Typ	Max	Unit
DRAIN CURRENT					
1.35 V			10		mA
2.7 V			277		mA
4.0 V (Balanced)			58		mA
4.0 V (Singled-Ended)			29		mA

POWER CONSUMPTION

Table 4.

Parameter	Voltage (V)	Typical Current (mA)	Typical Power Consumption (mW)
VCC_{PAN}	4.0	29	116
VCC_{PAP}	4.0	29	116
VCC_{DRV}	2.7	32	86
VCC_{DIV}	2.7	46	124
VCC_{MIX}	2.7	32	86
VCC_{IF}	2.7	31	84
VCC_{RFVGA}	2.7	20	54
VCC_{TRIP}	2.7	56	151
VCC_{VCO}	2.7	52	140
VCC_{PA}	2.7	8	22
VCC_{D}	1.35	0.08	0.1
VCC_{SYN}	1.35	10	13

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VCC_{DRV}	2.85 V
VCC_{DIV}	2.85 V
VCC_{PAN}, VCC_{PAP}	4.2 V
VCC_{VCO}	2.85 V
VCC_{RFVGA}	2.85 V
VCC_{IF}	2.85 V
VCC_{MIX}	2.85 V
VCC_{TRIP}	2.85 V
VDD_{SYN}	1.6 V
VDD_{PA}	2.85 V
VDD_{D}	1.6 V
Serial Digital Interface Input Voltage	1.5 V
Thermal Resistance (R_{TH}), Junction to Ground Paddle	9.57°C
Baseband Inputs: BB, FM (Each)	0.75 V p-p
Storage Temperature	−55°C to +150°C
Operating Temperature	−40°C to 85°C
Reflow Temperature (Maximum Peak)	260°C
ESD Sensitivity, Charged Device Model (CDM)	Class C3 (250 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

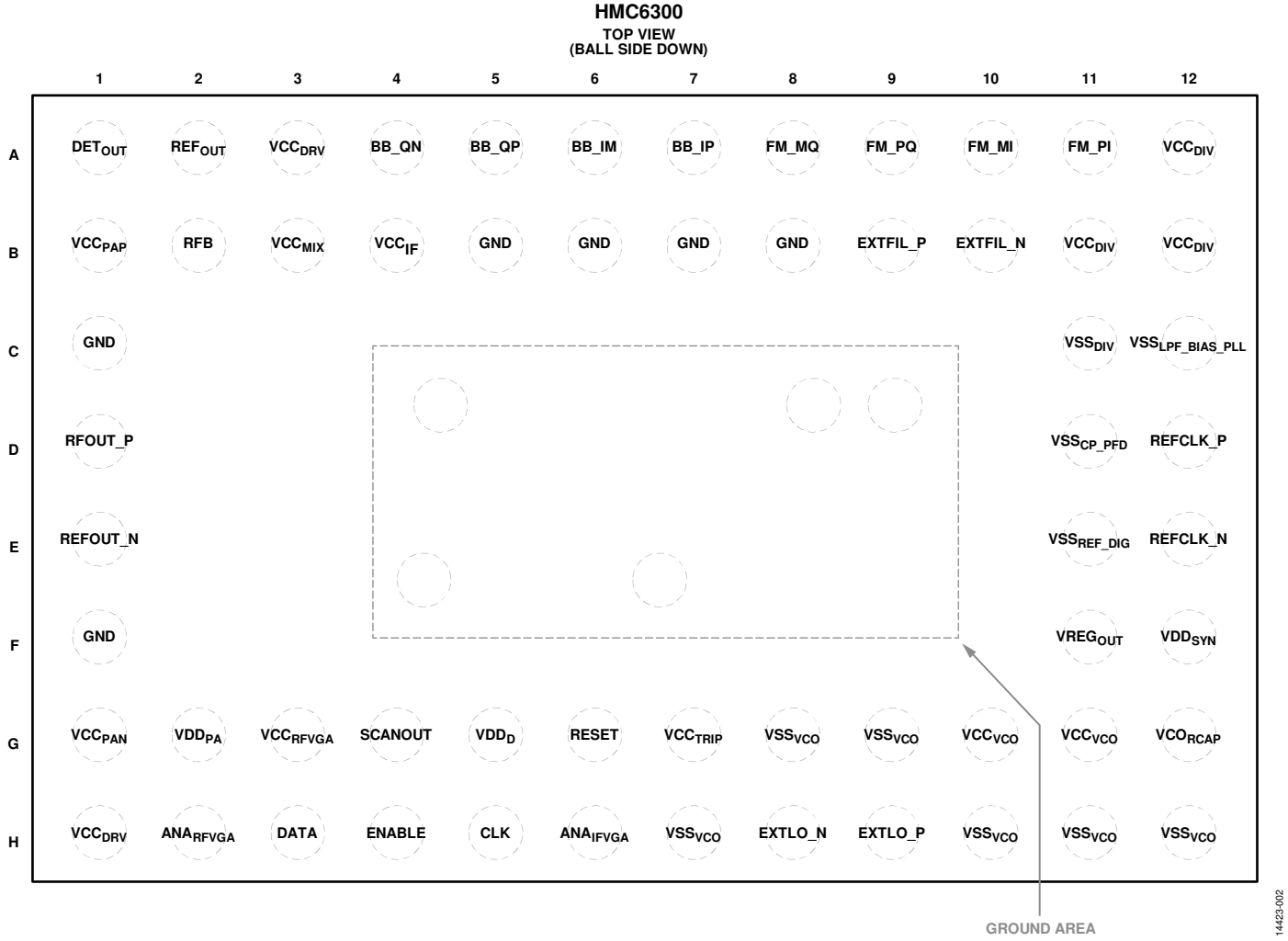

Figure 2. Pin Configuration Diagram

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	DET_{OUT}	Detector Output (0.6 V dc to 2.6 V dc).
A2	REF_{OUT}	Detector Reference Output (0.6 V dc).
A3, H1	VCC_{DRV}	Driver Power Supply (2.7 V dc).
A4	BB_QN	Quadrature Negative Baseband Input. This pin is dc-coupled and matched to 50 Ω.
A5	BB_QP	Quadrature Positive Baseband Input. This pin is dc-coupled and matched to 50 Ω.
A6	BB_IM	In-Phase Negative Baseband Input. This pin is dc-coupled and matched to 50 Ω.
A7	BB_IP	In-Phase Positive Baseband Input. This pin is dc-coupled and matched to 50 Ω.
A8	FM_MQ	FSK Negative (Minus) Quadrature Input. This pin is dc-coupled and matched to 50 Ω.
A9	FM_PQ	FSK Positive Quadrature Input. This pin is dc-coupled and matched to 50 Ω.
A10	FM_MI	FSK Negative (Minus) In-Phase Input. This pin is dc-coupled and matched to 50 Ω.
A11	FM_PI	FSK Positive In-Phase Input. This pin is dc-coupled and matched to 50 Ω.
A12, B11, B12	VCC_{DIV}	Divider Power Supply (2.7 V dc).
B1	VCC_{PAP}	Power Amplifier Power Supply (4.0 V dc).
B2	RFB	Detector Circuit Feedback.
B3	VCC_{MIX}	Mixer Power Supply (2.7 V dc).
B4	VCC_{IF}	IF Power Supply (2.7 V dc).
B5 to B8, C1, F1	GND	Analog Ground Connect.

Pin No.	Mnemonic	Description
B9	EXTFIL_P	External PLL Filter (Positive).
B10	EXTFIL_N	External PLL Filter (Negative).
C11	VSS_{DIV}	Digital Ground for the Synthesizer.
C12	$VSS_{LPF\_BIAS\_PLL}$	Digital Ground for Synthesizer.
D1	RFOUT_P	Radio Frequency Output (Positive). This pin is ac-coupled and is differentially matched to 100 Ω. This output port is disabled when single-ended output is selected.
D11	VSS_{CP_PFD}	Digital Ground for Synthesizer.
D12	REFCLK_P	External Reference Clock (Positive). This pin can be dc or ac matched to 50 Ω.
E1	RFOUT_N	Radio Frequency Output (Negative). This pin is ac coupled and is diff matched to 100 Ω. This pin is used if single-ended output is selected.
E11	VSS_{REF_DIG}	Digital Ground for Synthesizer.
E12	REFCLK_N	External Reference Clock (Negative). This pin can be dc or ac matched to 50 Ω.
F11	$VREG_{OUT}$	VCO Regulator Output.
F12	VDD_{SYN}	Synthesizer Power Supply (1.3 V dc).
G1	VCC_{PAN}	Power Amplifier Power Supply (4.0 V dc).
G2	VDD_{PA}	Power Amplifier Power Supply (2.7 V dc).
G3	VCC_{RFVGA}	RF VGA Power Supply (2.7 V dc).
G4	SCANOUT	Serial Digital Interface Output (1.2 V CMOS).
G5	VDD_{D}	Digital Circuits Power Supply (1.3 V dc).
G6	RESET	Serial Digital Interface Reset (1.2 V CMOS).
G7	VCC_{TRIP}	Tripler Power Supply (2.7 V dc).
G8, G9, H7, H10 to H12	VSS_{VCO}	Digital Ground for the VCO.
G10, G11	VCC_{VCO}	VCO Power Supply (2.7 V dc).
G12	VCO_{RCAP}	External Capacitor Connection for the VCO Regulator.
H2	ANA_{RFVGA}	0.1 V to 2.4 V RF VGA Analog Control. Connect Pin H2 to 2.7 V dc for digital control.
H3	DATA	Serial Digital Interface Data (1.2 V CMOS).
H4	ENABLE	Serial Digital Interface Enable (1.2 V CMOS).
H5	CLK	Serial Digital Interface Clock (1.2 V CMOS).
H6	ANA_{IFVGA}	0.1 V to 2.4 V IF VGA Analog Control. Connect Pin H6 to 2.7 V dc for digital control.
H8	EXTLO_N	External LO (Negative) Input.
H9	EXTLO_P	External LO (Positive) Input.

TYPICAL PERFORMANCE CHARACTERISTICS

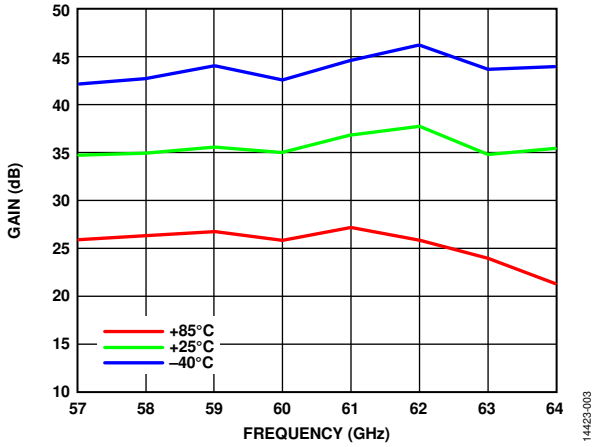

Figure 3. Maximum Gain vs. Frequency over Temperature, IF and RF Attenuation = 0 dBm

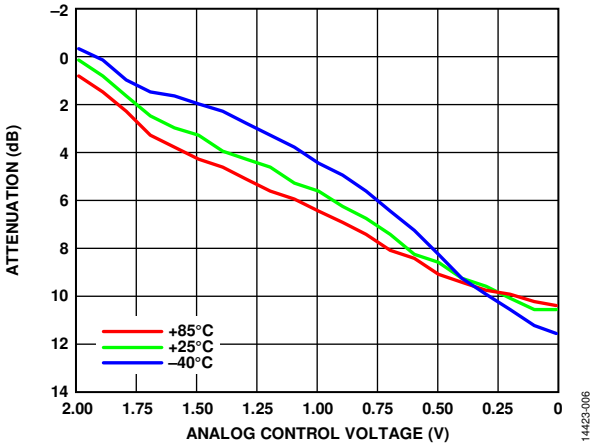

Figure 6. IF Attenuation vs. Analog Control Voltage over Temperature, Measurement Taken at 60 GHz, RF Attenuation = 0 dBm

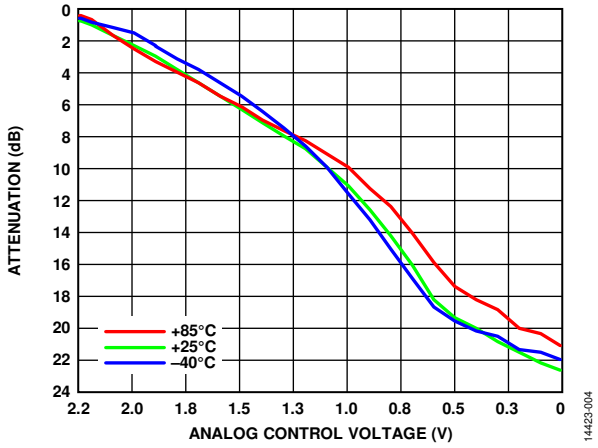

Figure 4. RF Attenuation vs. Analog Control Voltage over Temperature, Measurement Taken at 60 GHz, IF Attenuation = 0 dBm

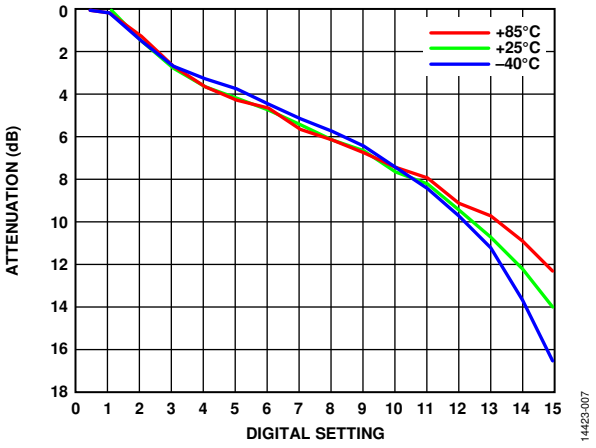

Figure 7. IF Attenuation vs. Digital Setting over Temperature, Measurement Taken at 60 GHz, RF Attenuation = 0 dBm

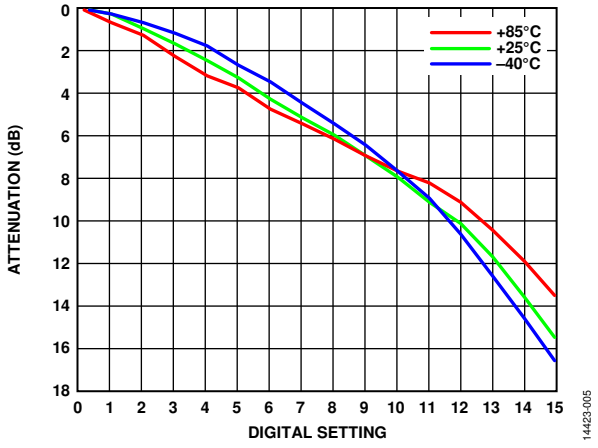

Figure 5. RF Attenuation vs. Digital Setting over Temperature, Measurement Taken at 60 GHz, IF Attenuation = 0 dBm

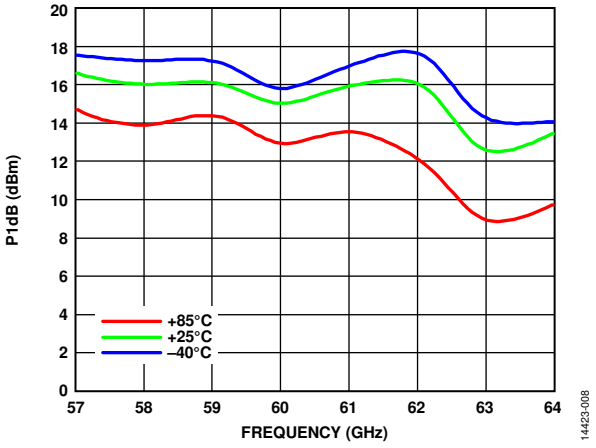

Figure 8. Output P1dB vs. Frequency over Temperature, IF and RF Attenuation = 0 dBm

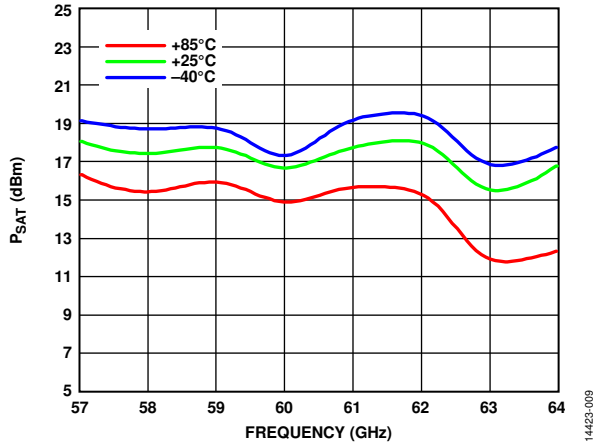

Figure 9. Output Saturated Power (P_{SAT}) vs. Frequency over Temperature, IF and RF Attenuation = 0 dBm

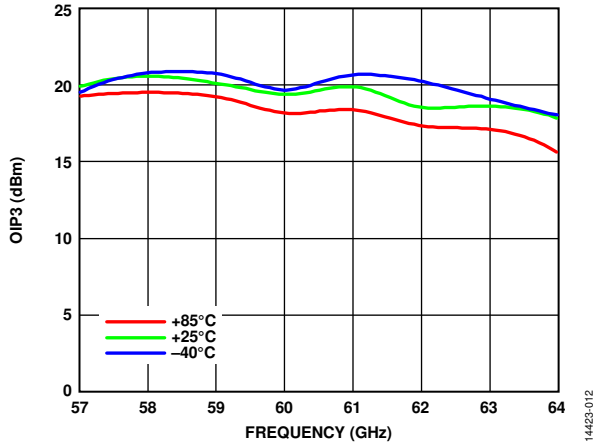

Figure 12. OIP3 vs. Frequency over Temperature, Total P_{OUT} = 0 dBm, IF and RF Attenuation = 0 dBm

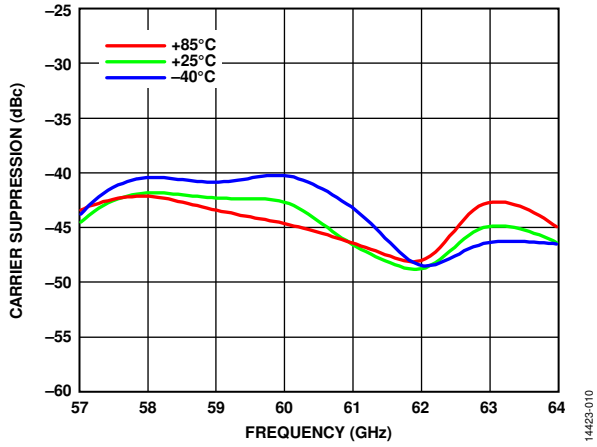

Figure 10. Carrier Suppression vs. Frequency over Temperature, IF and RF Attenuation = 0 dBm

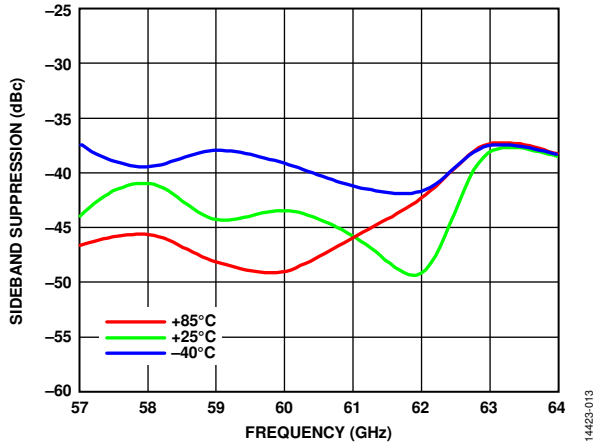

Figure 13. Sideband Suppression vs. Frequency over Temperature, IF and RF Attenuation = 0 dBm

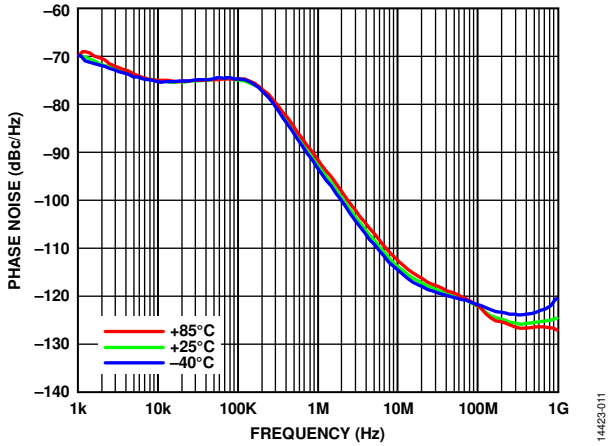

Figure 11. Phase Noise vs. Frequency Offset over Temperature, Internal LO, Measurement Taken at 60 GHz

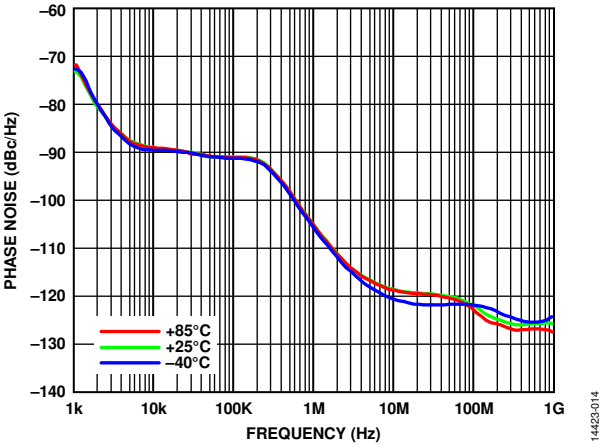

Figure 14. Phase Noise vs. Frequency Offset over Temperature, External LO, Measurement Taken at 60 GHz

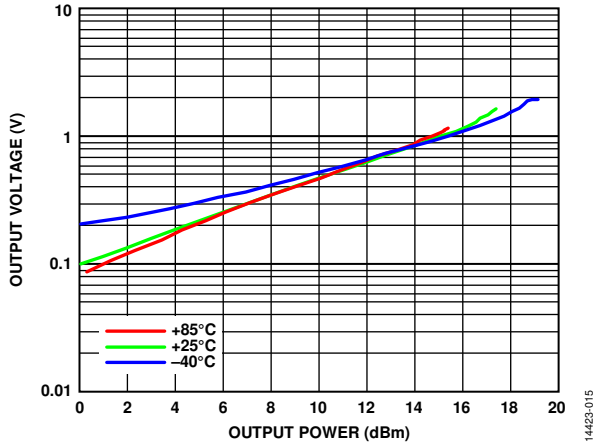

Figure 15. Detector Output Voltage vs. Output Power over Temperature, Measurement Taken at 60 GHz, and 1.15 kΩ Connecting DET_{OUT} and RFB Pins

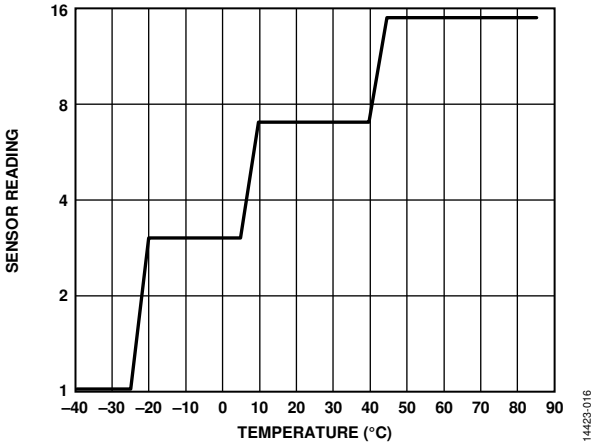

Figure 16. Temperature Sensor Reading vs. Temperature

THEORY OF OPERATION

An integrated frequency synthesizer creates a low phase noise LO between 16.3 GHz and 18.3 GHz. The step size of the synthesizer equates to 250 MHz steps at RF when used with a 71.42857 MHz reference crystal or 500 MHz if used with a 142.857 reference crystal. To support IEEE channels (ISM band) with a 540 MHz step size, use a 154.2857 MHz reference crystal.

If the chip is configured for I/Q baseband input, these signals are quadrature modulated onto an 8 GHz to 9.1 GHz sliding IF using the synthesized LO divided by two. There are also options to input AM/FM/FSK/MSK waveforms directly to the on-chip IF modulators. The IF signal is then filtered and amplified with 14 dB of variable gain, then mixed with three times the LO frequency to upconvert to an RF frequency between 57 GHz and 64 GHz.

Integrated notch filters attenuate the lower mixing product at 40 GHz to 46 GHz. Three RF amplifier stages provide gain to allow up to 15 dBm of linear and differential output power with 22 dB of variable gain. IF and RF gain can be controlled using either analog voltages or the digital SPI. For lower power consumption, half of the power amplifier can be disabled to run in a single-ended configuration; this drops the output power by 3 dB.

An on-chip power detector can be used to monitor the rms output power. The detector output pin (DET_{OUT}) is connected through an external resistor to the RFB pin. A resistor value of 1.15 kΩ is recommended for optimal coverage up to the P1dB point of the transmitter. The REF_{OUT} pin provides the reference voltage for the detector, and the difference between DET_{OUT} and REF_{OUT} is used to estimate the output power.

The phase noise and quadrature balance of the on-chip synthesizer is sufficient to support up to 64 QAM modulation. For higher order modulation (up to 256 QAM or less than 250 MHz step size), the HMC6300 can be operated using an external LO.

The HMC6300 transmitter is ideal for FDD operation together with the HMC6301 receiver chip. However, both devices can support TDD operation by enabling and disabling the circuits. All of the enables are placed in register array, four of which allow for full chip enable or disable in one SPI write.

There are no special power sequencing requirements for the HMC6300; all voltages are to be applied simultaneously.

REGISTER ARRAY ASSIGNMENT AND SERIAL INTERFACE

The register arrays for both the transmitter and receiver are organized into 32 rows of 8 bits. Using the serial interface, the arrays are written or read one row at a time, as shown in Figure 17 and Figure 18, respectively. Figure 17 shows the sequence of signals on the ENABLE, CLK, and DATA lines to write one 8-bit row of the register array. The ENABLE line goes low, the first of 18 data bits (Bit 0) is placed on the DATA line, and 2 ns or longer after the DATA line stabilizes, the CLK line goes high to clock in Data Bit 0. The DATA line should remain stable for at least 2 ns after the rising edge of CLK.

A write operation requires 18 data bits and 18 clock pulses, as shown in Figure 17. The 18 data bits contain the 8-bit register array row data (LSB is clocked in first), followed by the register array row address (ROW 0 through ROW 23, 000000 to 001111, LSB first), the read/write bit (set to 1 to write), and finally the Tx Chip Address 110, LSB first).

The Tx IC supports a serial interface running up to several hundred megahertz, and the interface is 1.2 V CMOS levels.

Note that the register array row address is six bits, but only four are used to designate 32 rows, the two MSBs are 0.

After the 18th clock pulse of the write operation, the ENABLE line returns high to load the register array on the IC; prior to the rising edge of the ENABLE line, no data is written to the array. The CLK line should have stabilized in the low state at least 2 ns prior to the rising edge of the ENABLE line.

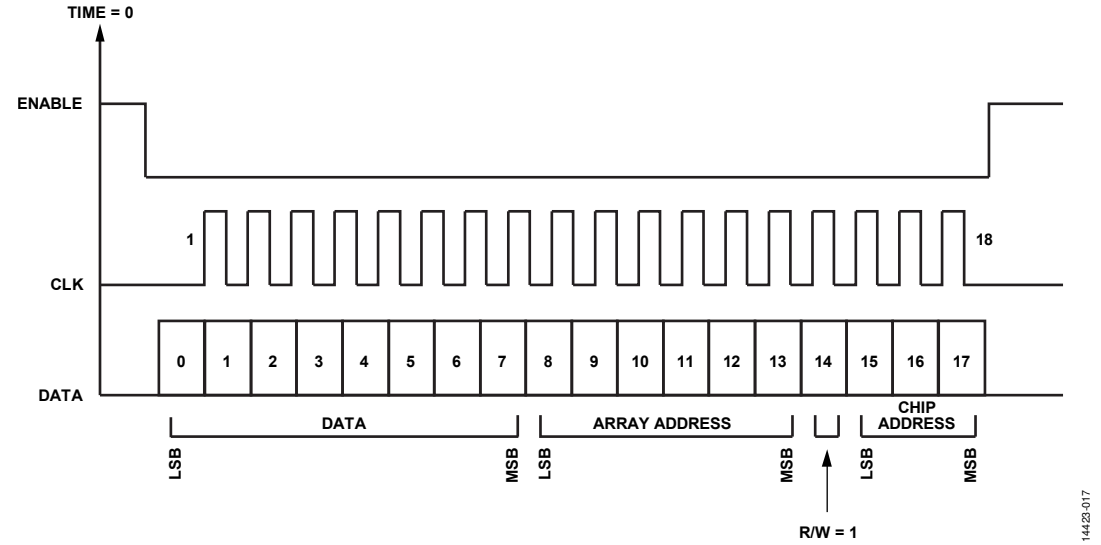

Figure 17.Timing Diagram for Writing a Row of the Transmitter Serial Interface

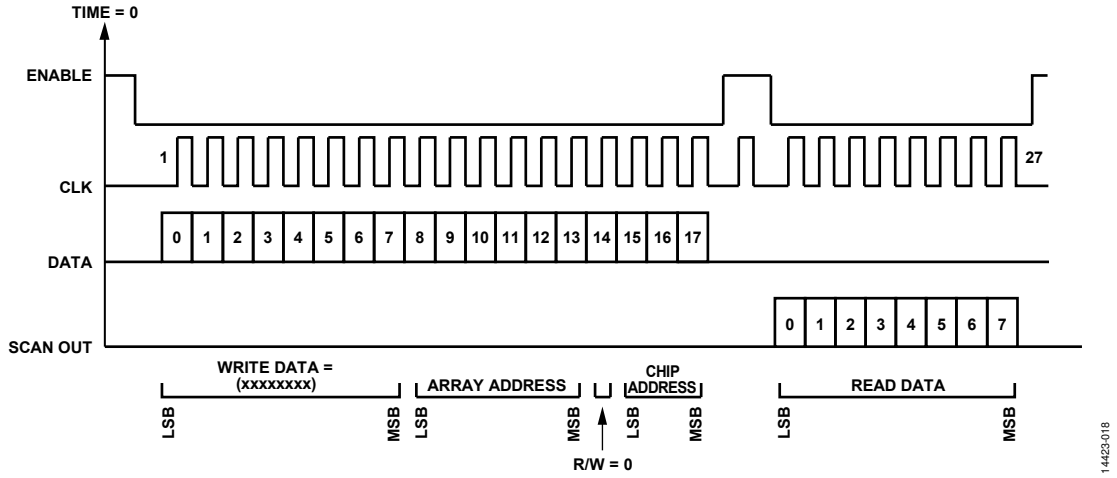

Figure 18. Timing Diagram for Reading a Row of the Transmitter Serial Interface

TRANSMITTER REGISTER ARRAY ASSIGNMENTS

In the following table, N/A means not applicable. All register arrays are read/write, unless otherwise indicated.

Table 7. Transmitter Register Array Assignments

Register Array Row and Bit	Internal Signal Name	Signal Function
ROW0	N/A	Not used.
ROW1		
ROW1, Bit 7	pa_sel_vgbs<3>	Controls the regulator for the base voltage of the power amplifier output transistors. ROW1, Bits[7:3] = 1100 for normal operation.
ROW1, Bit 6	pa_sel_vgbs<2>	
ROW1, Bit 5	pa_sel_vgbs<1>	
ROW1, Bit 4	pa_sel_vgbs<0>	
ROW1, Bit 3	ifvga_q_cntrl<0>	
ROW1, Bit 2	pa_sel_vref<2>	Controls the bias current for the power amplifier output transistors. ROW1, Bits[2:0] = 010 for normal operation.
ROW1, Bit 1	pa_sel_vref<1>	
ROW1, Bit 0	pa_sel_vref<0>	

Register Array Row and Bit	Internal Signal Name	Signal Function
ROW2		
ROW2, Bit 7 ROW2, Bit 6 ROW2, Bit 5 ROW2, Bit 4	pa_sel_alc_dac<3> pa_sel_alc_dac<2> pa_sel_alc_dac<1> pa_sel_alc_dac<0>	Factory diagnostics; ROW2. Bits[7:4] = 1111 for normal operation.
ROW2, Bit 3	pa_sep_pa_pwrdn_fast	Active high for normal operation.
ROW2, Bit 2	pa_pwrdwn_fast	Active high for normal operation.
ROW2, Bit 1	pa_se_sel	Control for Tx output interface; active low for differential Tx output; active high for Tx single-ended output.
ROW2, Bit 0	power_det_pwrdn	Active low to enable Tx power detector.
ROW3		
ROW3, Bit 7 ROW3, Bit 6 ROW3, Bit 5	driver_bias<2> driver_bias<1> driver_bias<0>	Controls the bias current for the power amplifier driver. ROW3, Bits[7:5] = 111 for normal operation.
ROW3, Bit 4 ROW3, Bit 3 ROW3, Bit 2	driver_bias2<2> driver_bias2<1> driver_bias2<0>	Controls the bias current for the Power Amplifier Predriver 2. ROW3, Bits[4:2] = 101 for normal operation.
ROW3, Bit 1	en_ifmix_HiCG	Active high to enable high gain mode in IF mixer.
ROW3, Bit 0	en_tempflash	Active high to enable temperature sensor.
ROW4		
ROW4, Bit 7	driver_pwrdn	Active high to power down the driver amplifier.
ROW4, Bit 6	upmixer_pwrdn	Active high to power down the upmixer.
ROW4, Bit 5	ifvga_pwrdn	Active high to power down the IF VGA.
ROW4, Bit 4	divider_pwrdn	Active high to power down the divider.
ROW4, Bit 3	pa_pwrdn	Active high to power down the power amplifier.
ROW4, Bit 2	rfvga_pwrdn	Active high to power down the RF VGA.
ROW4, Bit 1	tripler_pwrdn	Active high to power down the tripler.
ROW4, Bit 0	if_upmixer_pwrdn	Active high to power down the IF upmixer.
ROW5		
ROW5, Bit 7 ROW5, Bit 6 ROW5, Bit 5 ROW5, Bit 4 ROW5, Bit 3 ROW5, Bit 2 ROW5, Bit 1 ROW5, Bit 0	tripler_bias<13> tripler_bias<12> tripler_bias<11> tripler_bias<10> tripler_bias<9> tripler_bias<8> tripler_bias<7> tripler_bias<6>	Controls bias of frequency tripler. ROW5, Bits[7:0] = 11111111 for normal operation.
ROW6		
ROW6, Bit 7 ROW6, Bit 6 ROW6, Bit 5 ROW6, Bit 4 ROW6, Bit 3 ROW6, Bit 2	tripler_bias<5> tripler_bias<4> tripler_bias<3> tripler_bias<2> tripler_bias<1> tripler_bias<0>	Controls bias of frequency tripler. ROW6, Bits[7:2] = 111011 for normal operation.
ROW6, Bit 1 ROW6, Bit 0	N/A	Not used.
ROW7		
ROW7, Bit 7 ROW7, Bit 6 ROW7, Bit 5 ROW7, Bit 4	ifvga_vga_adj<3> ifvga_vga_adj<2> ifvga_vga_adj<1> ifvga_vga_adj<0>	IF variable gain amplifier gain control bits. ROW7, Bits[7:4] = 0000 is highest gain and 1101 is lowest gain. Attenuation is ≈ 1.3 dB per step, ≈ 17 dB maximum.

Register Array Row and Bit	Internal Signal Name	Signal Function
ROW7, Bit 3 ROW7, Bit 2 ROW7, Bit 1 ROW7, Bit 0	ifvga_tune<3> ifvga_tune<2> ifvga_tune<1> ifvga_tune<0>	Controls the tuning of the IF filter for the variable gain amplifier. ROW7, Bits[3:0] = 1111 for normal operation.
ROW8		
ROW8, Bit 7 ROW8, Bit 6 ROW8, Bit 5 ROW8, Bit 4	ifvga_bias<3> ifvga_bias<2> ifvga_bias<1> ifvga_bias<0>	Controls the bias current of the IF variable gain amplifier. ROW8, Bits[7:4] = 1000 for normal operation.
ROW8, Bit 3 ROW8, Bit 2 ROW8, Bit 1 ROW8, Bit 0	if_upmixer_tune<3> if_upmixer_tune<2> if_upmixer_tune<1> if_upmixer_tune<0>	Controls the tuning of the IF filter for the IF to RF upmixer. ROW8, Bits[3:0] = 1111 for normal operation.
ROW9		
ROW9, Bit 7 ROW9, Bit 6 ROW9, Bit 5	ifvga_q_cntrl<2> ifvga_q_cntrl<1> ifvga_q_cntrl<0>	Controls the Q of the IF filter in the baseband to IF upmixer. ROW9, Bits[7:5] = 000 for the highest Q and highest gain. To reduce Q and widen bandwidth, increment ROW9, Bits[7:5] in sequence, as follows: 001 100 101
ROW9, Bit 4 ROW9, Bit 3 ROW9, Bit 2 ROW9, Bit 1 ROW9, Bit 0	N/A	Not used.
ROW10		
ROW10, Bit 7	enable_FM	Active high to enable FSK/MSK modulation inputs. 0 = normal I/Q operation.
ROW10, Bit 6	if_refsel	Reserved for diagnostic purposes. ROW10, Bits[6:5] = 10 for normal operation.
ROW10, Bit 5	bg_monitor	
ROW10, Bit 4	enDig_IFVGA_Gain_Control	Active high to enable digital control of IFVGA gain.
ROW10, Bit 3	ipc_pwrdn	Active high to power down the chip current reference generator.
ROW10, Bit 2	if_bgmux_pwrdn	Active high to power down one of three on-chip band gap references (IF) and associated mux.
ROW10, Bit 1	upmix_cal_pwrdn	Active high to power down upmixer calibration.
ROW10, Bit 0	TempSensor_pwrdn	Active high to power down the temperature sensor.
ROW11		
ROW11, Bit 7 ROW11, Bit 6 ROW11, Bit 5 ROW11, Bit 4	RFVGAgain<3> RFVGAgain<2> RFVGAgain<1> RFVGAgain<0>	RF variable gain amplifier control bits. ROW11, Bits[7:4] gain settings as follows: 0000 = highest gain. 1111 = lowest gain. Attenuation is ≈ 1.3 dB/step, ≈ 17 dB maximum.
ROW11, Bit 3	enRFVGA_Ana	Active high to enable analog gain control of RFVGA.
ROW11, Bit 2 ROW11, Bit 1 ROW11, Bit 0	RFVGA_ICtrl<2> RFVGA_ICtrl<1> RFVGA_ICtrl<0>	Controls bias current of RF variable amplifier. ROW11, Bits[2:0] = 011 for normal operation.
ROW12		
ROW12, Bit 7 ROW12, Bit 6 ROW12, Bit 5 ROW12, Bit 4 ROW12, Bit 3	upmix_cal<7> upmix_cal<7> upmix_cal<7> upmix_cal<7> upmix_cal<7>	3 × LO feedthrough calibration of RF upmixer. ROW12, Bits[7:0] = 01100100 for uncalibrated operation.

Register Array Row and Bit	Internal Signal Name	Signal Function
ROW12, Bit 2 ROW12, Bit 1 ROW12, Bit 0	upmix_cal<7> upmix_cal<7> upmix_cal<7>	
ROW13	N/A	Not used.
ROW14	N/A	Not used.
ROW15	N/A	Not used.
ROW16		
ROW16, Bit 7	byp_synth_LDO	Factory diagnostics. 0 = normal operation.
ROW16, Bit 6	en_cpShort	Factory diagnostics. 0 = normal operation.
ROW16, Bit 5	en_cpCMFB	Enables CMFB circuit for charge pump, set to 1 when synthesizer is in use.
ROW16, Bit 4	en_cp_dump	Enables auxiliary circuit for charge pump, set to 1 when synthesizer is in use.
ROW16, Bit 3	en_cpTRIST	Factory Diagnostics. 0 = normal operation.
ROW16, Bit 2	en_cp	Enables charge pump, set to 1 when synthesizer is in use.
ROW16, Bit 1	en_synth_LDO	Enables LDO for synthesizer, set to 1 when synthesizer is in use.
ROW16, Bit 0	enbar_synthBG	Factory diagnostics. 0 = normal operation.
ROW17		
ROW17, Bit 7	en_lockd_clk	Enables lock detector for synthesizer, set to 1 when synthesizer is in use.
ROW17, Bit 6	en_test_divOut	Factory diagnostics. 0 = normal operation.
ROW17, Bit 5	en_vtune_flash	Enables flash ADCs for VCO vtune port, set to 1 when synthesizer is in use.
ROW17, Bit 4	en_reBuf_DC	Enables dc coupling for reference clock buffer.
ROW17, Bit 3	en_refBuf	Enables reference clock buffer, set to 1 when synthesizer is in use.
ROW17, Bit 2	en_stick_div	Factory diagnostics. 0 = normal operation.
ROW17, Bit 1	en_FBDiv_cml2cmos	Enables auxiliary circuit for the feedback divider chain, set to 1 when synthesizer is in use.
ROW17, Bit 0	en_FBDiv	Enables feedback divider chain, set to 1 when synthesizer is in use.
ROW18		
ROW18, Bit 7	N/A	Not used.
ROW18, Bit 6	en_nb250m	Active high to enable, 250 MHz channel step size.
ROW18, Bit 5	byp_vco_LDO	Factory diagnostics. 0 = normal operation.
ROW18, Bit 4	en_extLO	Enables external LO, set to 0 when synthesizer is in use.
ROW18, Bit 3	en_vcoPk	Factory diagnostics. 0 = normal operation.
ROW18, Bit 2	en_vco	Enables internal VCO, set to 1 when synthesizer is in use.
ROW18, Bit 1	en_vco_reg	Enables internal regulator for VCO, set to 1 when synthesizer is in use.
ROW18, Bit 0	enbar_vcoGB	Factory diagnostics. 0 = normal operation.
ROW19		
ROW19, Bit 7 ROW19, Bit 6 ROW19, Bit 5 ROW19, Bit 4 ROW19, Bit 3 ROW19, Bit 2	N/A	Not used.

Register Array Row and Bit	Internal Signal Name	Signal Function
ROW19, Bit 1	refsel_synthBG	Factory diagnostics. 1 = normal operation.
ROW19, Bit 0	muxRef	Factory diagnostics. 0 = normal operation.
ROW20		
ROW20, Bit 7	N/A	Not used.
ROW20, Bit 6	Fbdiv_code<6>	Feedback divider ratio for the integer-N synthesizer based on Table 8 to Table 10.
ROW20, Bit 5	Fbdiv_code<5>	
ROW20, Bit 4	Fbdiv_code<4>	
ROW20, Bit 3	Fbdiv_code<3>	
ROW20, Bit 2	Fbdiv_code<2>	
ROW20, Bit 1	Fbdiv_code<1>	
ROW20, Bit 0	Fbdiv_code<0>	
ROW21		
ROW21, Bit 7	N/A	Not used.
ROW21, Bit 6		
ROW21, Bit 5		
ROW21, Bit 4	refsel_vcoBG	Factory diagnostics. 1 = normal operation.
ROW21, Bit 3	vco_biasTrim<3>	Sets VCO tank bias current. ROW21, Bits[3:0] = 0010 for normal operation.
ROW21, Bit 2	vco_biasTrim<2>	
ROW21, Bit 1	vco_biasTrim<1>	
ROW21, Bit 0	vco_biasTrim<0>	
ROW22		
ROW22, Bit 7	N/A	Not used.
ROW22, Bit 6		
ROW22, Bit 5		
ROW22, Bit 4	vco_bandSel<4>	Set for desired frequency. Table 8, Table 9, and Table 10 contain approximate band settings depending on the reference clock frequency. ROW22, Bits[4:0] = valid range 00000 to 10011.
ROW22, Bit 3	vco_bandSel<3>	
ROW22, Bit 2	vco_bandSel<2>	
ROW22, Bit 1	vco_bandSel<1>	
ROW22, Bit 0	vco_bandSel<0>	
ROW23		
ROW23, Bit 7	ICP_BiasTrim<2>	Sets charge pump current. ROW23, Bits[7:5] = 011 for normal operation.
ROW23, Bit 6	ICP_BiasTrim<1>	
ROW23, Bit 5	ICP_BiasTrim<0>	
ROW23, Bit 4	vco_offset<0>	Sets internal VCO output swing. ROW23, Bits[4:0] = 00010 for normal operation.
ROW23, Bit 3	vco_offset<1>	
ROW23, Bit 2	vco_offset<2>	
ROW23, Bit 1	vco_offset<3>	
ROW23, Bit 0	vco_offset<4>	
ROW24 (Read Only)		
ROW24, Bit 7	N/A	Not used.
ROW24, Bit 6		
ROW24, Bit 5		
ROW24, Bit 4		
ROW24, Bit 3	lockdet	Monitor for lock detect. 1 = valid lock.
ROW24, Bit 2	dn	Monitor VCO amplitude.
ROW24, Bit 1	up	Monitor VCO amplitude.
ROW24, Bit 0	center	Monitor VCO amplitude.
ROW25 (Read Only)		

Register Array Row and Bit	Internal Signal Name	Signal Function
ROW25, Bit 7	vtune_flashp<7>	VCO amplitude monitor (positive).
ROW25, Bit 6	vtune_flashp<6>	
ROW25, Bit 5	vtune_flashp<5>	
ROW25, Bit 4	vtune_flashp<4>	
ROW25, Bit 3	vtune_flashp<3>	
ROW25, Bit 2	vtune_flashp<2>	
ROW25, Bit 1	vtune_flashp<1>	
ROW25, Bit 0	vtune_flashp<0>	
ROW26 (Read Only)		
ROW26, Bit 7	vtune_flashn<7>	VCO amplitude monitor (negative).
ROW26, Bit 6	vtune_flashn<6>	
ROW26, Bit 5	vtune_flashn<5>	
ROW26, Bit 4	vtune_flashn<4>	
ROW26, Bit 3	vtune_flashn<3>	
ROW26, Bit 2	vtune_flashn<2>	
ROW26, Bit 1	vtune_flashn<1>	
ROW26, Bit 0	vtune_flashn<0>	
ROW27 (Read Only)		
ROW27, Bit 7	N/A	Not used.
ROW27, Bit 6		
ROW27, Bit 5		
ROW27, Bit 4	tempS<4>	Thermometer encoded temperature reading.
ROW27, Bit 3	tempS<3>	For ROW27, Bits[4:0], the temperature reading is as follows:
ROW27, Bit 2	tempS<2>	00000 = lowest temperature.
ROW27, Bit 1	tempS<1>	11111 = highest temperature.
ROW27, Bit 0	tempS<0>	
ROW28	N/A	Not used.
ROW29	N/A	Not used.
ROW30	N/A	Not used.
ROW31	N/A	Not used.

SYNTHESIZER SETTINGS

Table 8. Synthesizer Settings, IEEE Channels Using 154.2857 MHz Reference

Frequency (GHz)	IEEE Channel	Divider Setting, Fbdiv_Code<5:4>, ROW20, Bits[5:0]	Typical Band Setting, vco_bandSel<4:0>, ROW22, Bits[4:0]
57.24		001010	00001
57.78		001011	00010
58.32	Channel 1	001100	00010
58.86		001101	00010
59.40		001110	00011
59.94		001111	00011
60.48	Channel 2	010000	00100
61.02		010001	00100
61.56		010010	00101
62.10		010011	00101
62.64	Channel 3	010100	00101
63.18		010101	00110
63.72		010110	00110
64.26		010111	00110
64.8	Channel 4	011000	00111
65.34		011001	00111
65.88		011010	01000

Table 9. 500 MHz Channels Using 142.8571 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
56.5	010001	00001
57	010010	00001
57.5	010011	00010
58	010100	00010
58.5	010101	00010
59	010110	00011
59.5	010111	00011
60	011000	00100
60.5	011001	00100
61	011010	00101
61.5	011011	00101
62	011100	00101
62.5	011101	00110
63	011110	00110
63.5	011111	00110
64	100000	00111

Table 10. 250 MHz Channels Using 71.42857 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
56.5	0100010	00001
56.75	0100011	00001
57	0100100	00010
57.25	0100101	00010
57.5	0100110	00011
57.75	0100111	00011
58	0101000	00100
58.25	0101001	00100
58.5	0101010	00101
58.75	0101011	00101
59	0101100	00110
59.25	0101101	00110
59.5	0101110	00111
59.75	0101111	00111
60	0110000	01000
60.25	0110001	01000
60.5	0110010	01001
60.75	0110011	01001
61	0110100	01010
61.25	0110101	01010
61.5	0110110	01011
61.75	0110111	01011
62	0111000	01100
62.25	0111001	01100
62.5	0111010	01101
62.75	0111011	01101
63	0111100	01110
63.25	0111101	01110
63.5	0111110	01111
63.75	0111111	01111
64	1000000	01111

APPLICATIONS INFORMATION

For more information about the HMC6300 evaluation kit, see the *EK1HMC6350 User Guide*. The EK1HMC6350 contains all that is required to set up a simplex 60 GHz millimeterwave link using standard RF cable interfaces for baseband input and output. The kit comes with two motherboard printed circuit boards (PCBs) that provide on-board crystals, USB interface, supply regulators, and SMA cables for connectorized I/Q interfaces. Software is supplied to allow the user to read from and write to all chip level registers using graphical user interface (GUI) or to upload previously saved register settings.

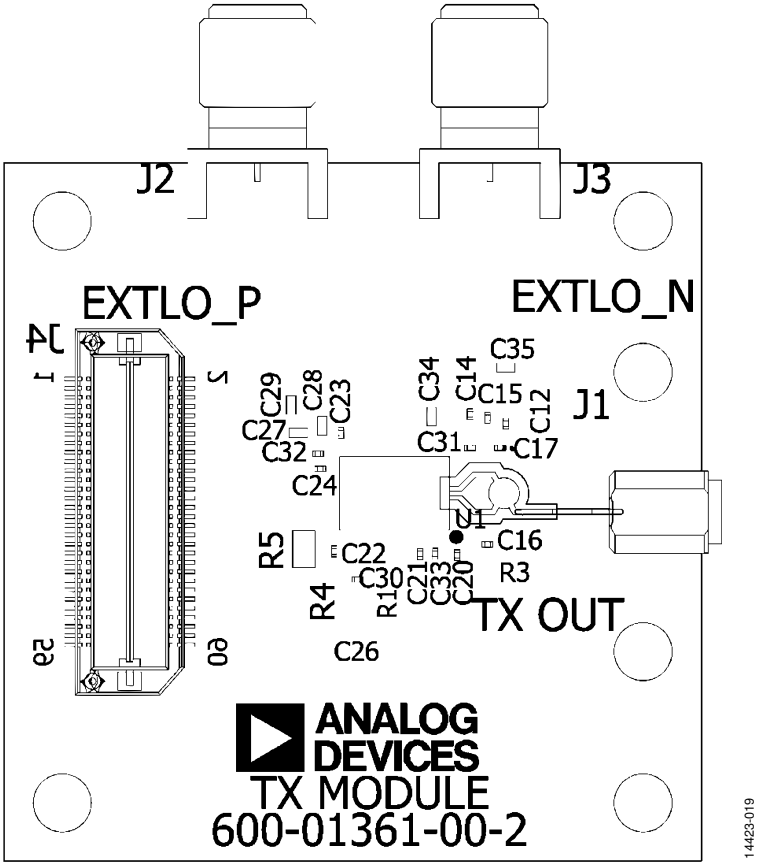

Figure 19. Evaluation PCB Daughter Board

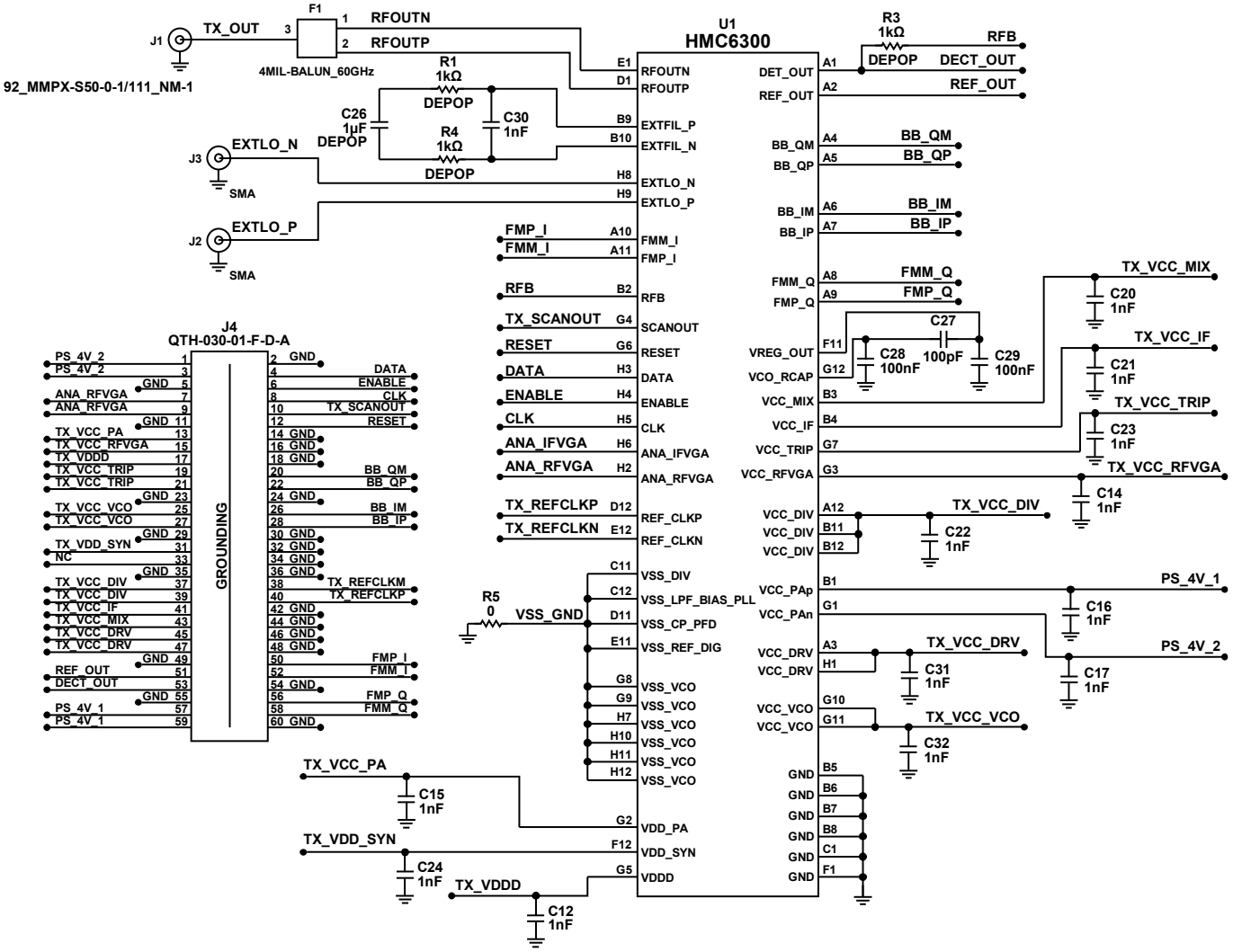

Figure 20. Evaluation Daughter Board PCB Schematic

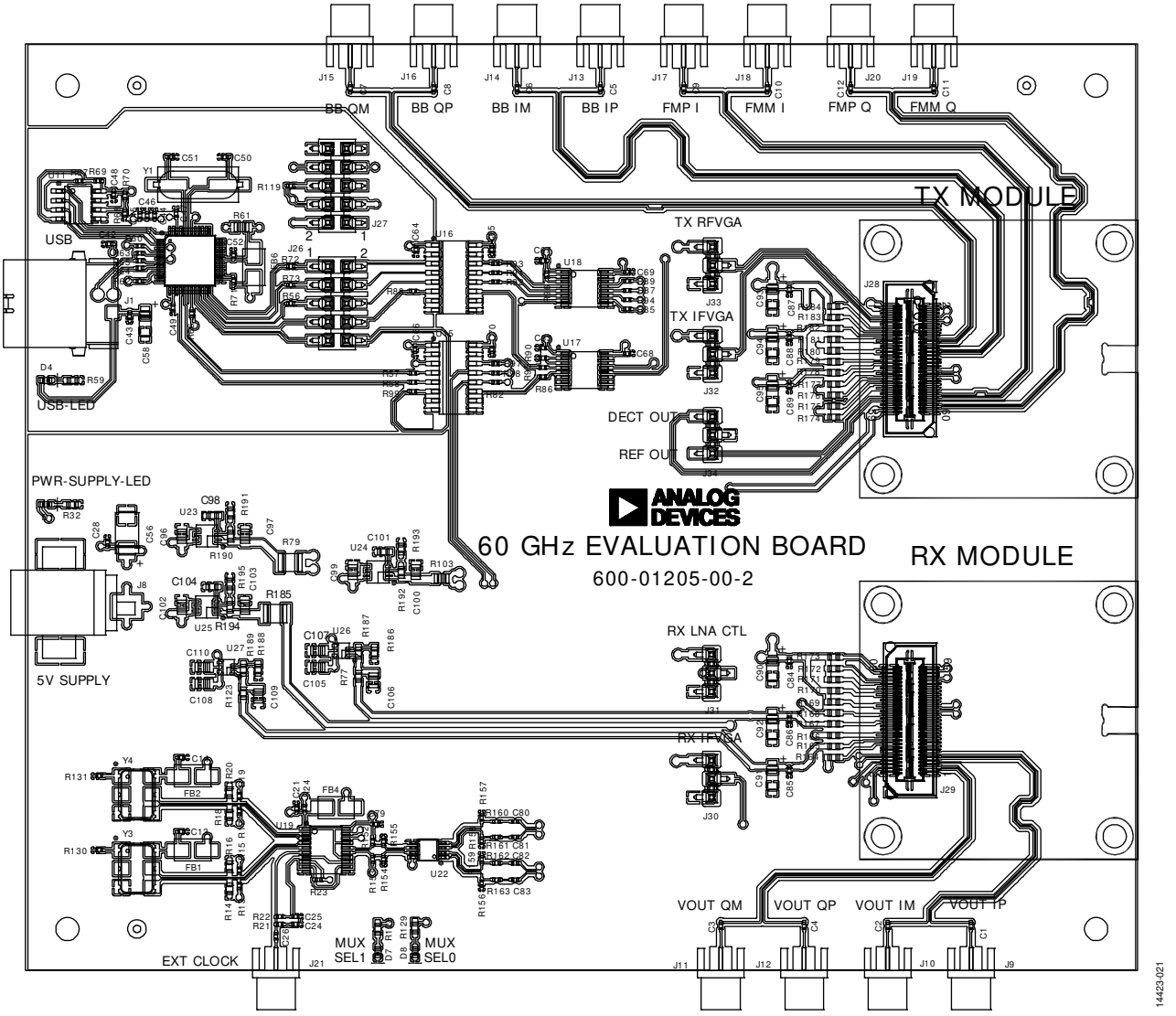

Figure 21. Evaluation PCB Motherboard