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# HMC679LC3C

v06.0514

## 26 GHz, T FLIP-FLOP w/ RESET & PROGRAMMABLE OUTPUT VOLTAGE

### Typical Applications

The HMC679LC3C is ideal for:

- Serial Data Transmission up to 26 Gbps
- High Speed Frequency Divider (up to 26 GHz)
- Broadband Test & Measurement
- RF ATE Applications

### Features

Supports Clock Frequencies up to 26 GHz

Differential or Single-Ended Operation

Fast Rise and Fall Times: 18 / 17 ps

Low Power Consumption: 270 mW typ.

Programmable Differential Output Voltage Swing: 600 - 1100 mVp-p

Propagation Delay: 95 ps

Single Supply: -3.3 V

16 Lead Ceramic 3 x 3 mm SMT Package: 9 mm$^2$

### Functional Diagram
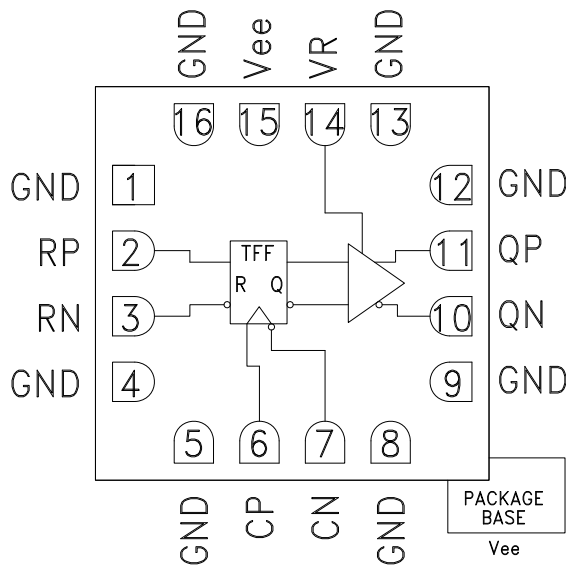


### General Description

The HMC679LC3C is a T Flip-Flop w/Reset designed to support clock frequencies as high as 26 GHz. During normal operation, with the reset pin not asserted, the output toggles from its prior state on the positive edge of the clock. This results in a divide-by-two function of the clock input. Asserting the reset pin forces the Q output low regardless of the clock edge state (asynchronous reset assertion). Reversing the clock inputs allows for negative-edge triggered applications.

All differential inputs to the HMC679LC3C are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC679LC3C also features an ouput level control pin, VR, which allows for loss compensation or signal level optimization. The HMC679LC3C operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

### Electrical Specifications, $T_A$ = +25 $^o$C, Vee = -3.3 V, VR = 0 V

| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| Power Supply Voltage | | -3.6 | -3.3 | -3.0 | V |
| Power Supply Current | | | 82 | | mA |
| Maximum Clock Rate | | | 26 | | GHz |
| Input Voltage Range | | -1.5 | | 0.5 | V |
| Input Differential Range | | 0.1 | | 2.0 | Vp-p |
| Input Return Loss | Frequency <23 GHz | | 10 | | dB |
| Output Amplitude | Single-Ended, peak-to-peak | | 550 | | mVp-p |
| | Differential, peak-to-peak | | 1100 | | mVp-p |
| Output High Voltage | | | -10 | | mV |
| Output Low Voltage | | | -560 | | mV |

For price, delivery, and to place orders: Analog Devices, Inc.,
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

# HMC679* PRODUCT PAGE QUICK LINKS

**Last Content Update: 02/23/2017**

## COMPARABLE PARTS 🗗

View a parametric search of comparable parts.

## EVALUATION KITS 🗗

- HMC679LC3C Evaluation Board

## DOCUMENTATION 🗗

**Data Sheet**

- HMC679 Data Sheet

## TOOLS AND SIMULATIONS 🗗

- HMC679 IBIS Model

## REFERENCE MATERIALS 🗗

**Quality Documentation**

- Package/Assembly Qualification Test Report: LC3, LC3B, LC3C (QTR: 2014-00376 REV: 01)
- Semiconductor Qualification Test Report: BiCMOS-C (QTR: 2013-00241)

## DESIGN RESOURCES 🗗

- HMC679 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS 🗗

View all HMC679 EngineerZone Discussions.

## SAMPLE AND BUY 🗗

Visit the product page to see pricing options.

## TECHNICAL SUPPORT 🗗

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK 🗗

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## Electrical Specifications (continued)

| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| Output Rise / Fall Time | Differential, 20% - 80% | | 18 / 17 | | ps |
| Output Return Loss | Frequency <13 GHz | | 10 | | dB |
| Random Jitter Jr | rms [1] | | | 0.2 | ps rms |
| Deterministic Jitter, Jd | peak-to-peak, $2^{15}$-1 PRBS input [2] | | 2 | | ps, p-p |
| Propagation Delay Clock to Q, td | | | 95 | | ps |
| Propagation Delay Reset to Q, tdr | | | 125 | | ps |
| VR Pin Current | VR = 0.0 V | | 2 | | mA |
| VR Pin Current | VR = +0.4 V | | | 3.5 | mA |

[1] Upper limit of random jitter, $J_R$, determined by measuring and integrating output phase noise with a sinusodal input at 5, 10, and 13.5 GHz over temperature.

[2] Deterministic jitter calculated by simultaneously measuring the jitter of a 200 mV, 12.5 GHz, $2^{15}$-1 PRBS input, and a single-ended output

### DC Current vs. Supply Voltage [1][2]
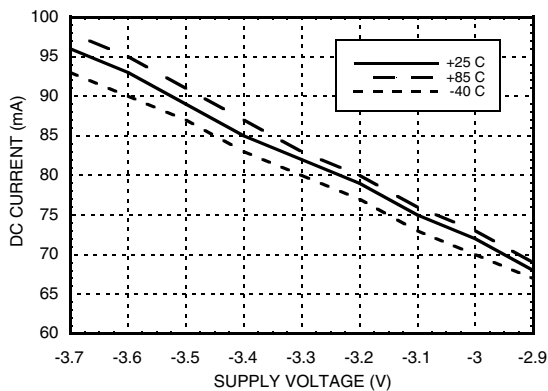


### Output Differential Voltage vs. Supply Voltage [1][2]
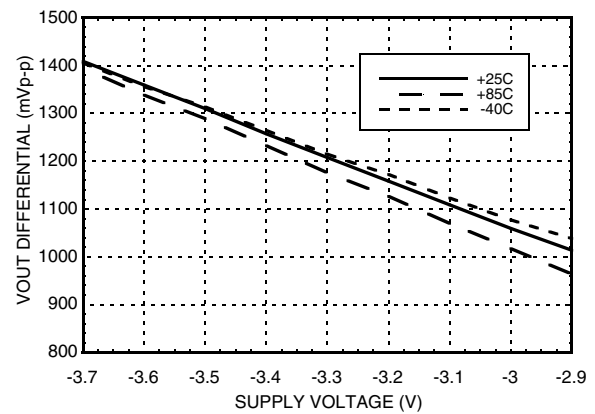


### Rise / Fall Time vs. Supply Voltage [1][3]
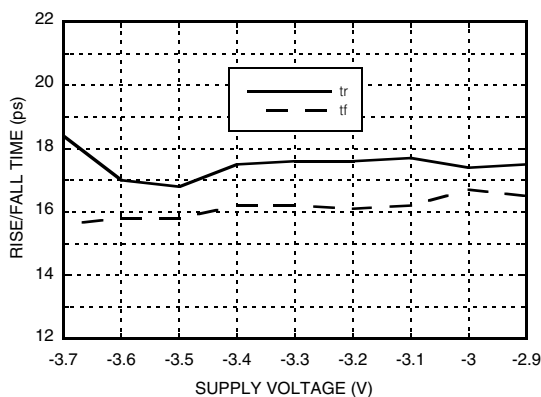


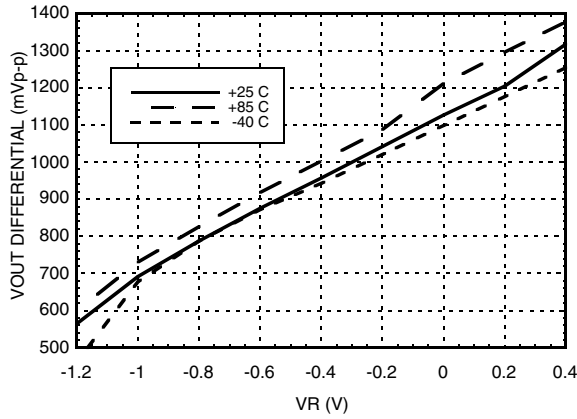### Output Differential Voltage vs. Input Frequency [1]
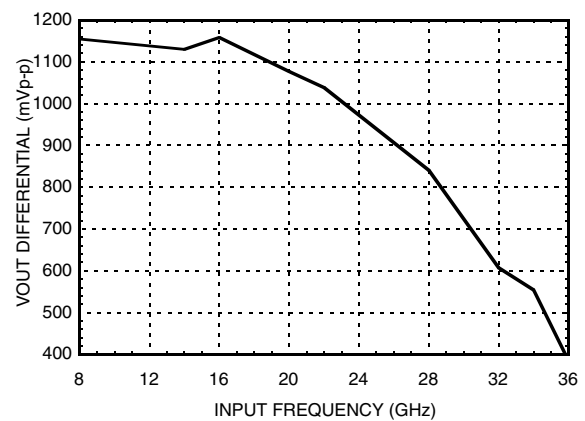


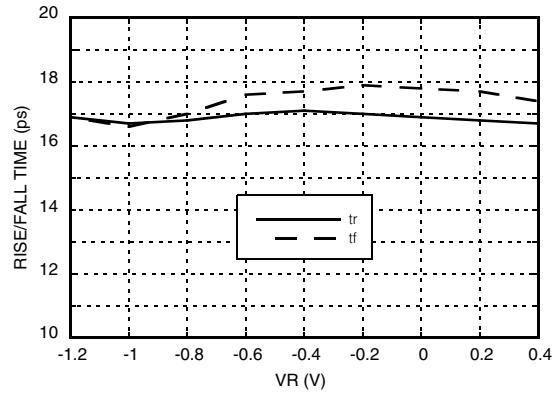[1] VR = 0.0 V          [2] Frequency = 13 GHz          [3] Frequency = 24 GHz

**ANALOG DEVICES**

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## 26 GHz, T FLIP-FLOP w/ RESET & PROGRAMMABLE OUTPUT VOLTAGE
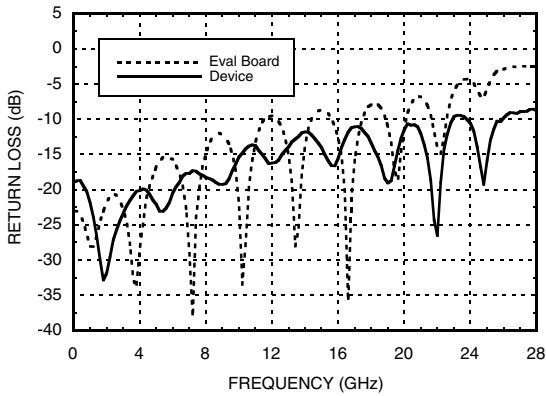
HIGH SPEED LOGIC - SMT

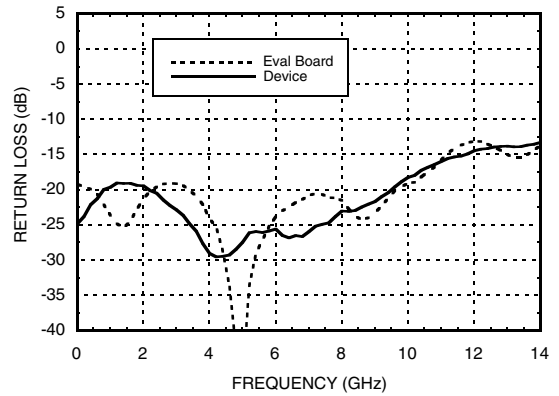### Output Differential Voltage vs. VR [2]



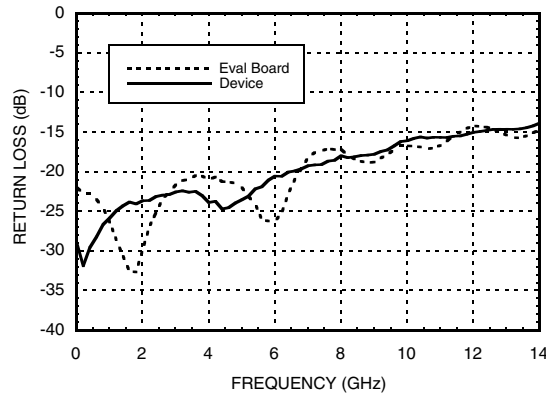### Rise / Fall Time vs. VR [3]



### Input Return Loss vs. Frequency [4]



### Output Return Loss vs. Frequency [4]



### Reset Input Return Loss vs. Frequency [4]



[1] VR = 0.0 V          [2] Frequency = 13 GHz          [3] Frequency = 24 GHz          [4] Device measured on evaluation board with single-ended, time-domain gating

**HIGH SPEED LOGIC - SMT**

## Output Waveform



[1] Test Conditions:
   Waveform generated with a CW signal source input at 26 GHz.
   Diagram data presented on a Tektronix CSA 8000.

## Timing Diagram



td = propagation delay, CK (clock) to Q
tdr = propagation delay, R (reset) to Q.

## 26 GHz, T FLIP-FLOP w/ RESET & PROGRAMMABLE OUTPUT VOLTAGE

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

### Absolute Maximum Ratings

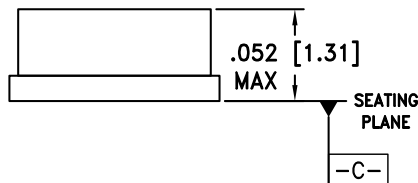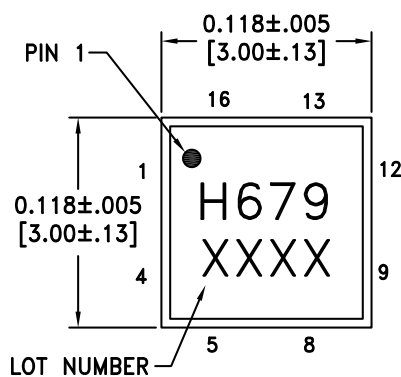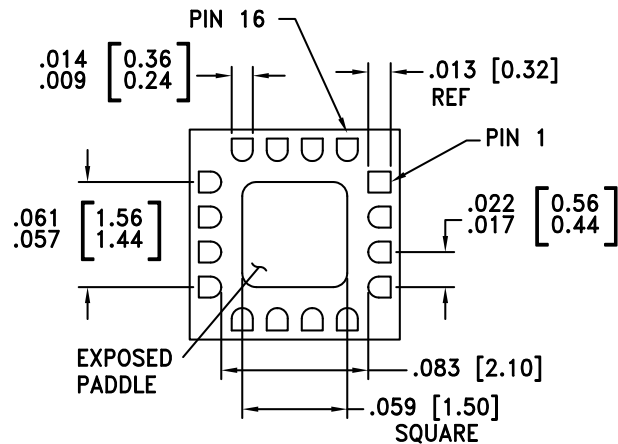| | |
|---|---|
| Power Supply Voltage (Vee) | -3.75 V to +0.5 V |
| Input Signals | -2 V to +0.5 V |
| Output Signals | -1.5 V to +1 V |
| Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C) | 0.68 W |
| Thermal Resistance ($R_{th\,l-p}$) Worst Case Junction to Package Paddle | 59 °C/W |
| Maximum Junction Temperature | 125 °C |
| Storage Temperature | -65 °C to +150 °C |
| Operating Temperature | -40 °C to +85 °C |
| ESD Sensitivity (HBM) | Class 1C |

### Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

### Package Information

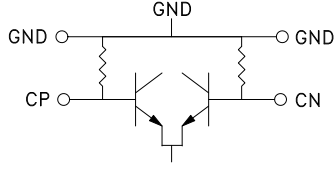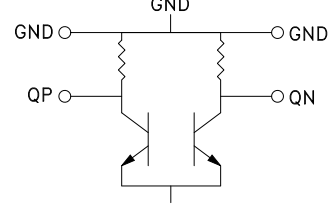| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [2] |
|---|---|---|---|---|
| HMC679LC3C | Alumina, White | Gold over Nickel | MSL3 [1] | H679 XXXX |
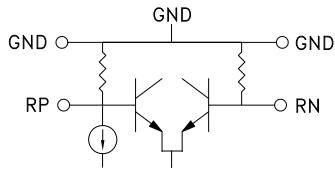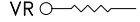
[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 4, 5, 8, 9, 12 | GND | Signal Grounds |  |
| 2, 3 | RP,RN | Differential Reset Inputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 6, 7 | CP,CN | Differential Clock Inputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 10, 11 | QN, QP | Differential Clock Outputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 13, 16 | GND | Supply Ground |  |
| 14 | VR | Output level control. Output level may be increased or decreased by applying a voltage to VR per "Output Differential vs. VR" plot. |  |
| 15, Package Base | Vee | This pin and the exposed paddle must be connected to the negative voltage supply. | |

**HIGH SPEED LOGIC - SMT**
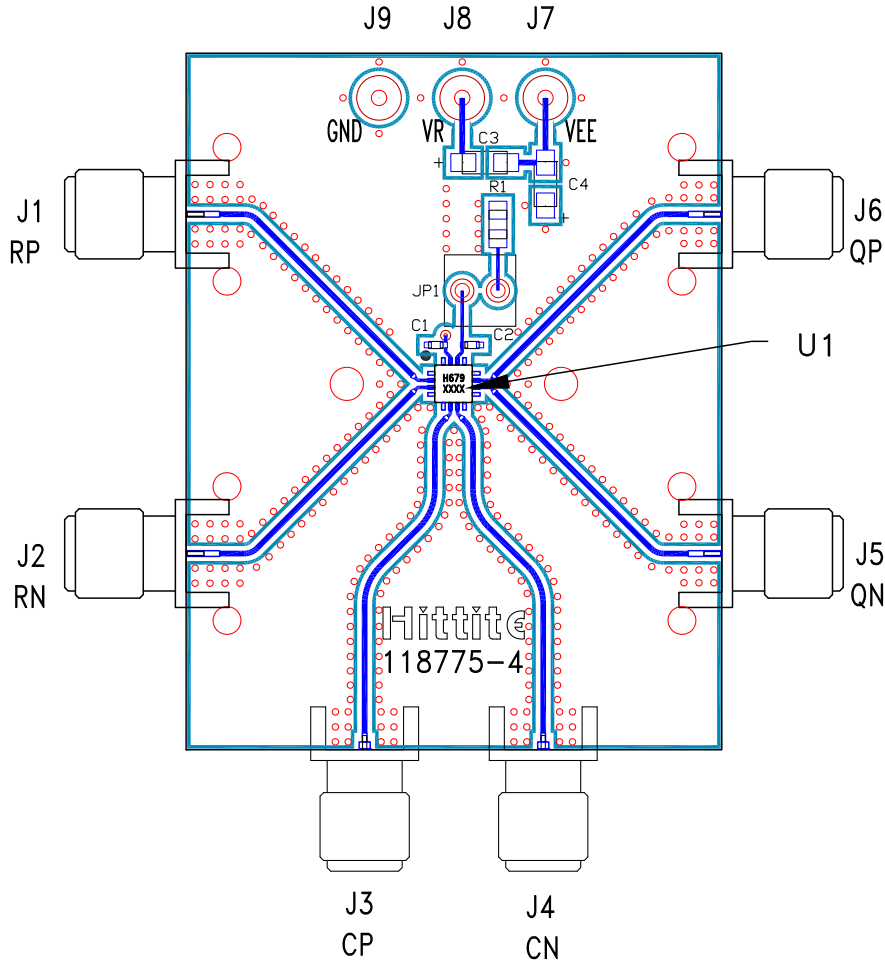
*Evaluation PCB*



## List of Materials for Evaluation PCB 123585 [1]

| Item | Description |
|------|-------------|
| J1, J2, J5, J6 | PCB Mount SMA RF Connectors |
| J3, J4 | PCB Mount 2.92mm RF Connectors |
| J7 - J9 | DC Pin |
| JP1 | 0.1" Header with Shorting Jumper |
| C1, C2 | 100 pF Capacitor, 0402 Pkg. |
| C3, C4 | 4.7 µF Capacitor, Tantalum |
| R1 | 10 Ohm Resistor, 0603 Pkg. |
| U1 | HMC679LC3C |
| PCB [2] | 118775 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

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## 26 GHz, T FLIP-FLOP w/ RESET & PROGRAMMABLE OUTPUT VOLTAGE

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### *Application Circuit*