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HMC703LP4E

v02.0813

8 GHz FRACTIONAL SYNTHESIZER

Typical Applications

The HMC703LP4E is ideal for:

- Microwave Point-to-Point Radios
- Base Stations for Mobile Radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs, WiMAX
- Communications Test Equipment
- CATV Equipment
- Automotive Sensors
- AESA - Phased Arrays
- FMCW Radar Systems

Features

Wide band: DC - 8 GHz RF Input

Best Phase Noise and Spurious in the Industry:
-112 dBc/Hz @ 8 GHz Fractional, 50 kHz Offset

Figure of Merit

-230 dBc/Hz Fractional Mode

-233 dBc/Hz Integer Mode

High PFD rate: 100 MHz

< 50 fs RMS jitter

Frequency and Phase Modulation

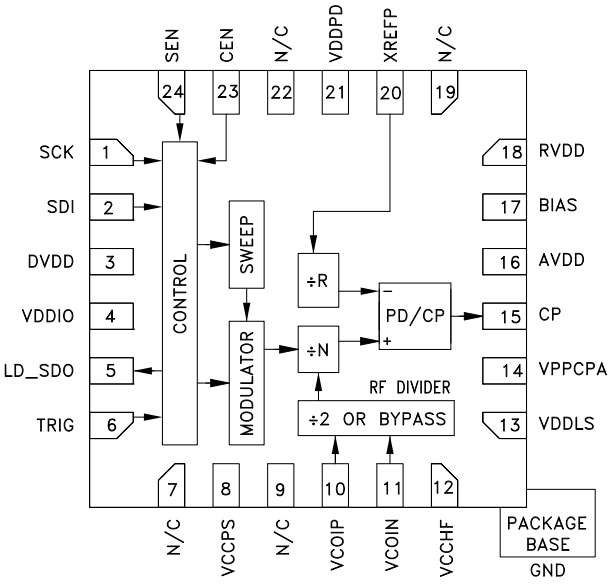
Integrated Frequency Sweeper

Triggered Frequency Hopping

External Triggering

24 Lead 4x4 mm SMT Package: 16 mm^2

Functional Diagram



General Description

The HMC703LP4E fractional synthesizer is built upon the high performance PLL platform also contained in the HMC704LP4E and Hittite's latest generation of PLL+VCO products. This platform has the best phase-noise and spurious performance in the industry - enabling higher order modulation schemes while minimizing blocker effects in high performance radios.

In addition, the HMC703LP4E offers frequency sweep and modulation features, external triggering, double-buffering, exact frequency control, phase modulation and more - while maintaining pin compatibility with the HMC700LP4E PLL.

Exact frequency mode with a 24-bit fractional modulator provides the ability to generate fractional frequencies with zero frequency error and very low channel spurious, an important feature for Digital Pre-Distortion systems.

The serial interface offers read back capability and is compatible with a wide variety of protocols.

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COMPARABLE PARTS

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EVALUATION KITS

- HMC703LP4E Evaluation Board

DOCUMENTATION

Data Sheet

- HMC703 Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: LP4, LP4B, LP4C, LP4K (QTR: 2013-00487 REV: 04)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

DESIGN RESOURCES

- HMC703 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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Table 1. Electrical Specifications

Unless otherwise specified, data is collected at 3.3 V, and 5.0 V (on charge-pump), 100 MHz reference, 50 MHz f_{PD}. Min and Max are specified across temperature range from -40 °C to 85 °C ambient.

Parameter	Conditions	Min.	Typ.	Max.	Units
RF INPUT CHARACTERISTICS	[6][7]				
RF Input Frequency Range	[1]	DC		8000	MHz
Prescaler Input Freq Range	[1]	DC		4000	MHz
Power Range	[13]	-15	-10	-3	dBm
Return Loss	[15]	-18	-12	-7	dB
REF INPUT CHARACTERISTICS					
Frequency Range (3.3V)	[1][8]	DC	50	350	MHz
Power from 50 Ω Source	[12] with 100 Ω termination off chip		6		dBm
Return Loss	[15]	-16		-8	dB
Ref Divider Range (14 bit)		1		16,383	
PHASE DETECTOR RATE	[1]				
Integer Mode		DC	50	115	MHz
Fractional Mode B		DC	50	100	MHz
Fractional Mode A		DC	50	80	MHz
CHARGE PUMP					
CP Output Current	20 µA Steps, Charge Pump Gain = CP Current/2π Amps/rad	0.02		2.5	mA
CP HiK	see "Charge Pump Gain" section		3.5	6	mA
POWER SUPPLIES					
RVDD, AVDD, VCCPS, VCCHF, VCCPD, DVDD, VDDIO		2.7	3.3	3.5	V
VDDLS, VPPCP Charge Pump	VDDLS, VPPCP must be equal	2.7	5.0	5.2	V
3.3V - Current consumption	[9] 100 kHz PD 50 MHz PD 100 MHz PD		 34 54 74	 45 70 95	 mA mA mA
5V - Current consumption	All Modes 100 kHz PD 50 MHz PD w/ CP HiK 100 MHz PD w/ CP HiK		 3 7 13	 5 12 16	 mA mA mA
Power Down Current	[10]			100	uA
BIAS Reference Voltage	Pin 12. Measured with 10 GΩ Meter	1.880	1.920	1.960	V

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Table 34. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
PHASE NOISE [14]					
Flicker Figure of Merit (FOM)[2]			-270		dBc/Hz
Floor Figure of Merit [11]	Integer HiK Mode Integer Normal Mode Fractional HiK Mode [3] Fractional Normal Mode [3]	-236 -232 -232 -228	-233 -230 -230 -227	-231 -228 -227 -225	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Flicker Noise at f_{offset}	PN_{flick} = Flicker FOM +20log(f_{vco}) -10log(f_{offset})				dBc/Hz
Phase Noise Floor at f_{vco} with f_{pd}	PN_{floor} = Floor FOM + 10log(f_{pd}) +20log(f_{vco}/f_{pd})				dBc/Hz
VCO referred Phase Noise Contribution of the PLL vs f_{offset}, f_{vco}, f_{pd}	$PN = 10\log(10^{(PNflick/10)} + 10^{(PNfloor/10)})$				dBc/Hz
Jitter	SSB 100Hz to 100MHz with HMC508LP5E VCO		50		fs
SPURIOUS	[4][5]				
Integer Boundary Spurs @~8GHz	offsets less than loop band-width, f_{pd} = 50MHz		-60	-52	dBc
LOGIC INPUTS					
Switching Theshold (Vsw)	VIH/VIL within 50 mV of Vsw	38	47	54	% VDDIO
LOGIC OUTPUT					
VOH Output High Voltage			VDDIO		V
VOL Output Low Voltage			0		V
Output impedance : Pull Up	VDDIO=3.3 V	115	150	180	Ohm
Output impedance : Pull Dn	VDDIO=3.3 V	130	135	210	Ohm
DC load				1.5	mA
Digital Output Driver Delay SCK to Digital Output Delay	1.7nsec with a 3 pF load		0.5ns+0.2ns/pF 8.2ns+0.2ns/pF		ns ns
RF Divider Range					
>4GHz Integer Mode	16 bit , Even values only	32		131,070	
< 4GHz Integer Mode	16 bit , All values	16		65,535	
> 4GHz Fractional Mode	16 bit	40.0		131,065.0	
< 4GHz Fractional Mode	16 bit	20.0		65,531.0	

[1] Frequency is guaranteed across process, voltage and temperature from -40°C to 85°C.
[2] With high charge-pump current, +12dBm 100MHz sine reference
[3] Fractional FOM degrades about 3dB/octave for prescaler input frequencies below 2GHz
[4] Using 50MHz reference with VCO tuned to within one loop bandwidth of an integer multiple of the PD frequency. Larger offsets produce better results. See the "Spurious Performance" section for more information.
[5] Measured with the HMC703LP4E evaluation board. Board design and isolation will affect performance.
[6] Internal divide-by-2 should be enabled for frequencies >4GHz
[7] At low RF Frequency, Rise and fall times should be less than 1ns to maintain performance
[8] Slew rate of greater or equal to 0.5 V/ns
[9] Current consumption depends upon operating mode and frequency of the VCO. Typical values are for fractional mode.
[10] Reference input disconnected
[11] Min/Max versus temperature and supply, under typical reference & RF frequencies and power levels
[12] Slew > 0.5V/ns is recommended , see Table 7, Figure 5, Figure 6 for more information.
[13] Operable with reduced spectral performance outside of this range.
[14] This section specifies the Phase Noise contribution of the PLL, solution phase noise with a given VCO, loop filter and reference requires a closed loop calculation using Hittite PLL Design Tool.
[15] As measured on HMC703LP4E Evaluation board, with 100Ohm external termination.

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, plots are measured with a 50 MHz PD rate, VCO near 8 GHz, RF power ≈ -10 dBm, and a Wenzel 100 MHz sinusoid reference. The operating modes in the following plots refer to Integer (int), Fractional Modes A and B, HiKcp (HiK).

Figure 1. Floor FOM vs. Mode and Temp, 2.5 mA CP Current

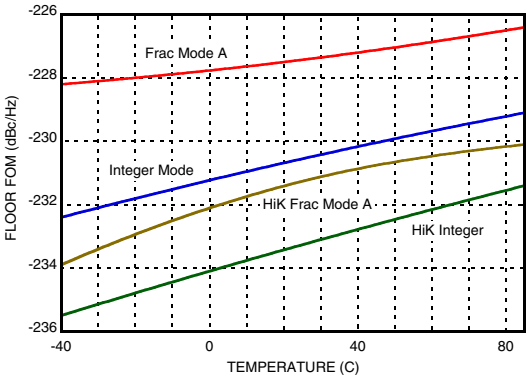


Figure 2. Flicker FOM vs. Mode and Temp, 2.5 mA CP Current

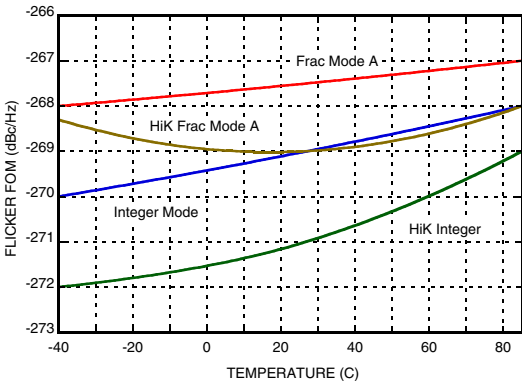


Figure 3. Floor FOM vs. Output Frequency and Mode, 2.5 mA CP Current

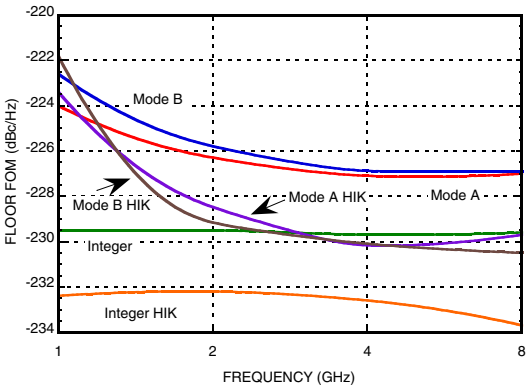


Figure 4. Flicker FOM vs. Output Frequency and Mode, 2.5 mA CP Current

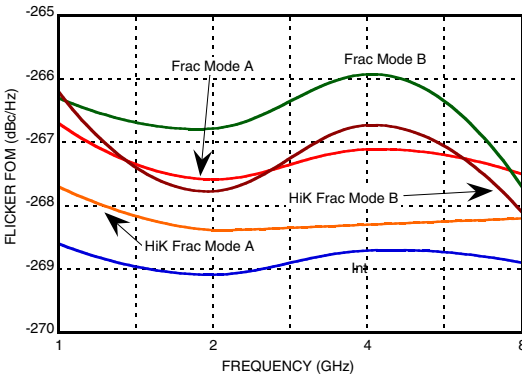


Figure 5. Floor FOM vs. Reference Power and Mode, 2.5 mA CP Current [1]

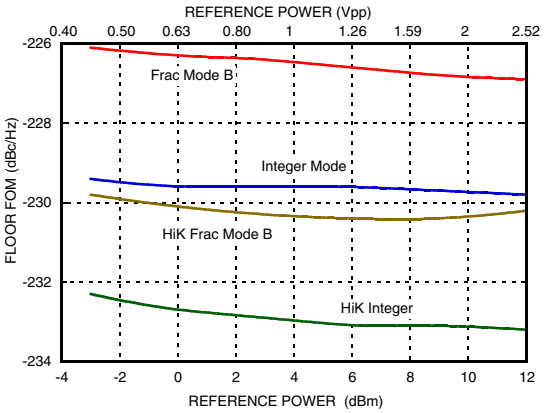
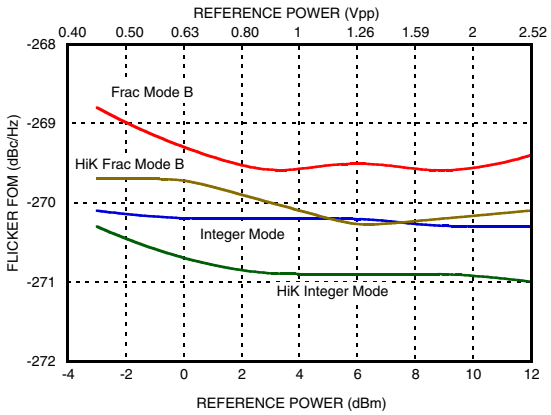


Figure 6. Flicker FOM vs. Reference Power and Mode, 2.5 mA CP Current [1]



[1] 100 MHz Sinusoidal Wenzel reference.

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Figure 7. Flicker FOM vs. CP Current, Fractional Mode B, 2.5 mA CP Current

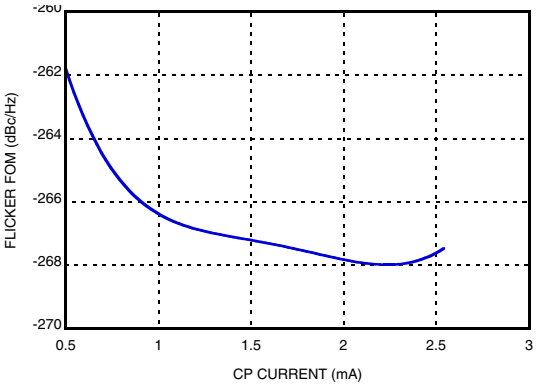


Figure 8. Floor FOM vs. CP Current, Fractional Mode B, 2.5 mA CP Current

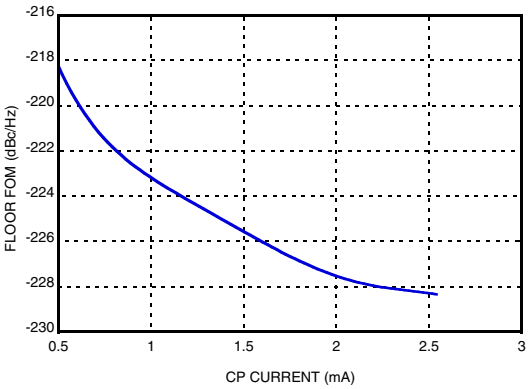


Figure 9. Flicker FOM vs. CP Voltage, CP Current = 2.5 mA [1]

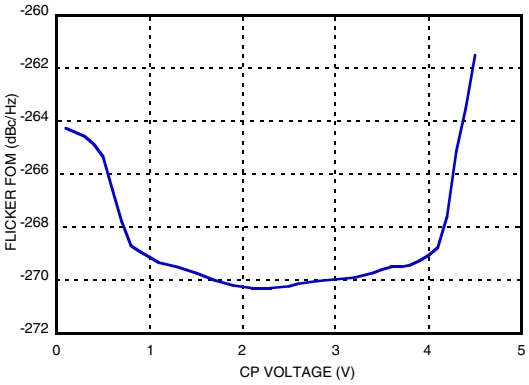


Figure 10. Floor FOM vs. CP Voltage, CP Current = 2.5 mA [1]

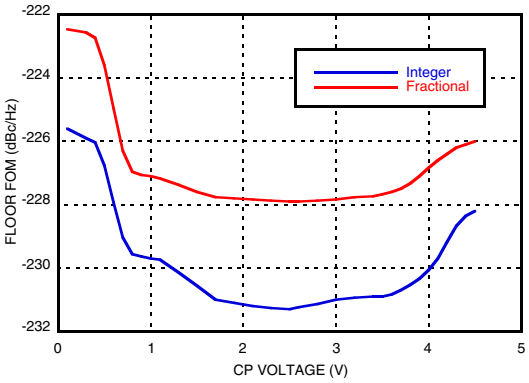


Figure 11. Flicker FOM vs. CP Voltage, HiKcp + CP Current = 6 mA [2]

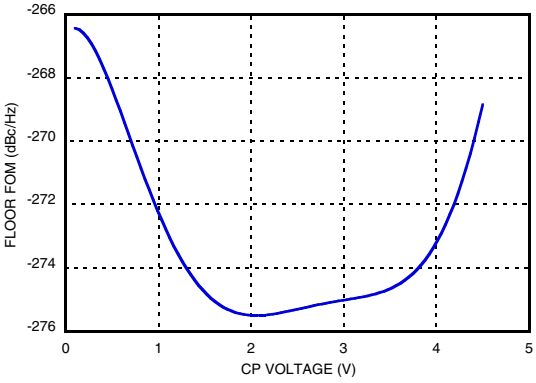
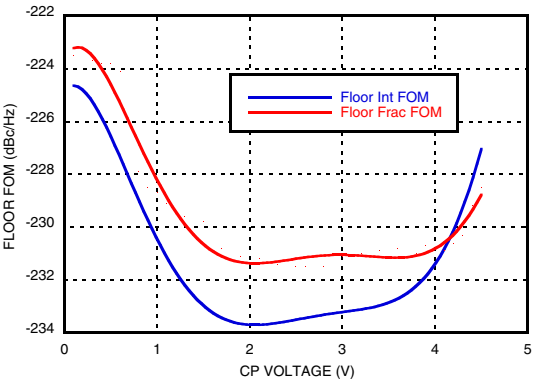


Figure 12. Floor FOM vs. CP Voltage, HiKcp + CP Current = 6 mA [2]



[2] Active Loop Filter, with DC bias point on -ve leg of op-amp swept.

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Figure 13. Typical Phase Noise & Spur Performance at 8 GHz + 200 kHz[3]

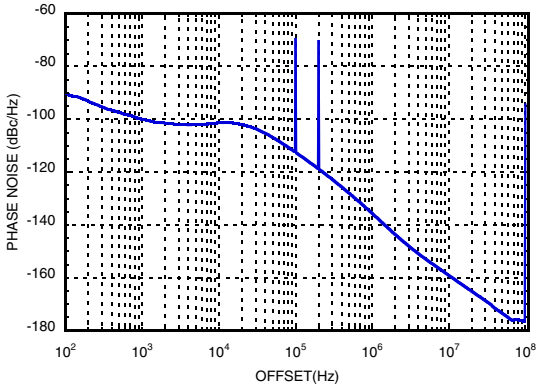


Figure 14. Fractional Performance, Exact Frequency Mode On at 8013.6 MHz [4]

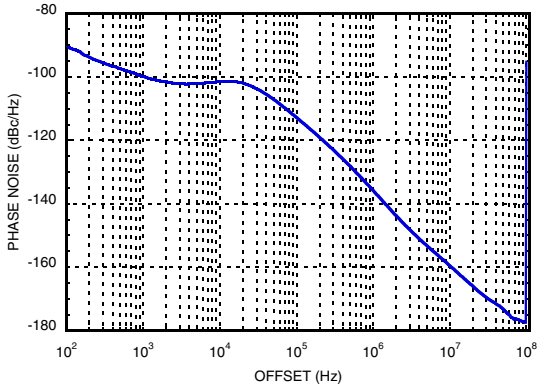


Figure 15. Integer Boundary Spur at 8 GHz + 20 kHz vs. Charge Pump Offset[5]

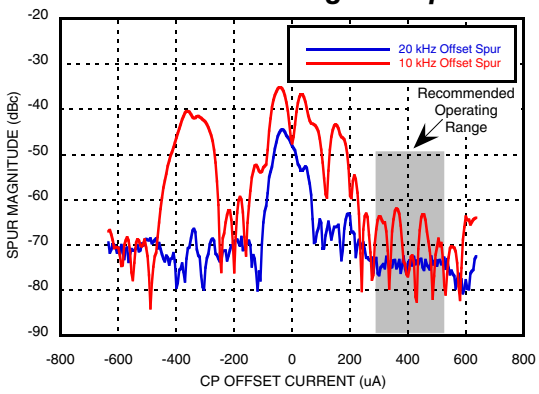


Figure 16. RF Input Limits [6]

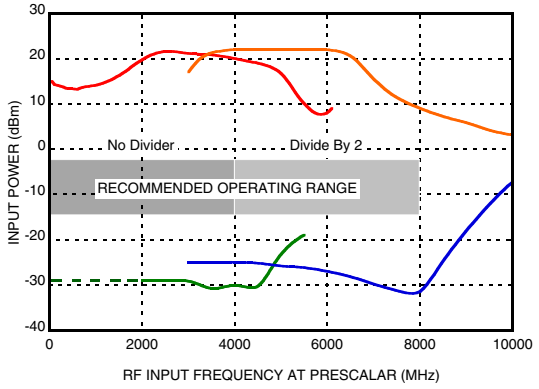


Figure 17. Modelled vs. Measured Phase Noise, Integer Mode HiK at 8 GHz [7]

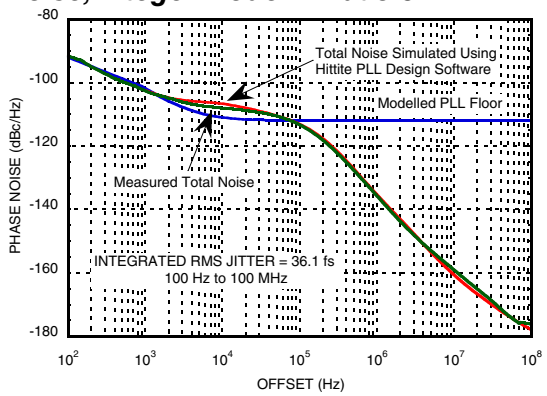
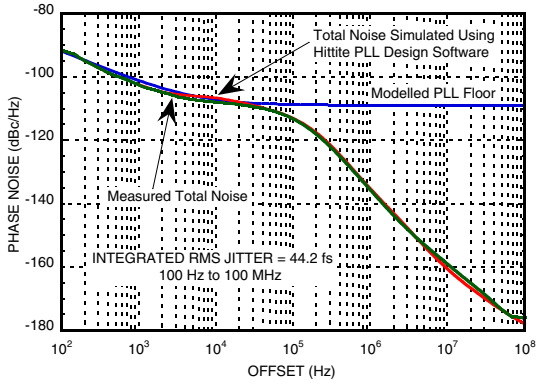


Figure 18. Modelled vs. Measured Phase Noise, Fractional Mode B, HiK at ~ 8 GHz [8]



[3] Output frequency = 8 GHz + 200 kHz using HMC508LP5E VCO, Reference Input = 100 MHz, PD frequency = 100 MHz, CP current = 2.5 mA, Fractional Mode B, 20 kHz bandwidth Loop Filter. Spur at 200kHz due to RF signal at 8GHz + 200kHz, spur at 100kHz due to prescaler input at 4GHz+100kHz. Reference feedthrough spur at 100 MHz offset.

[4] Exact Frequency Mode channel spacing 100 kHz, Fractional N, Rfout = 8013.6 MHz using HMC508LP5E VCO, Reference Input = 100 MHz, PD frequency = 100 MHz, Prescaler divide-by-2 selected. 20 kHz Loop Filter bandwidth, reference feedthrough spur at 100 MHz offset.

[5] Tuned to 8 GHz + 20 kHz, Prescaler at 4 GHz + 10 kHz, Loop bandwidth >> 20 kHz, Reference Frequency 50 MHz. Offset polarity should be positive for inverting configurations and negative otherwise.

[6] Low frequency minimum power levels not characterized. Low frequency limitation is only a function of external AC coupling capacitance signal slew rate.

[7] HiK integer mode measured at 8 GHz, Prescalar at 4 GHz, 50 MHz reference frequency.

[8] Active Fractional B Mode (Prescalar @ 4 GHz + 2.5 kHz), Reference Frequency 50 MHz.

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Figure 19. Floor FOM Near 8 GHz vs RF Input Power and Mode

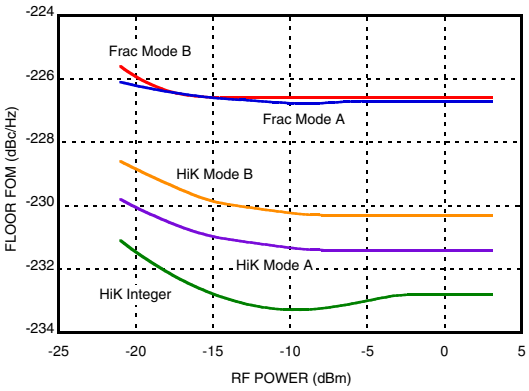


Figure 20. Flicker FOM Near 8 GHz vs. RF Input Power and Mode

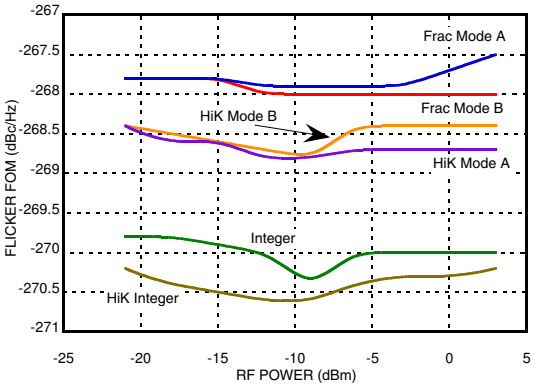


Figure 21. Reference Input Sensitivity, Square Wave, 50 Ω [9]

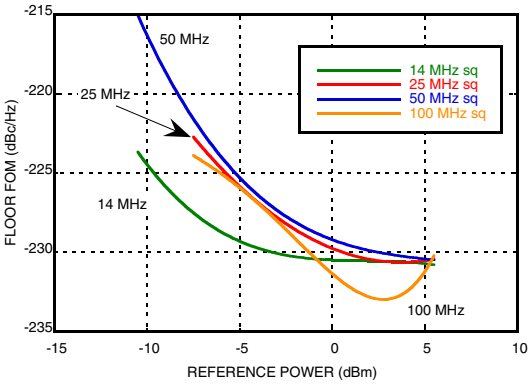


Figure 22. Reference Input Sensitivity Sinusoid Wave, 50 Ω [9]

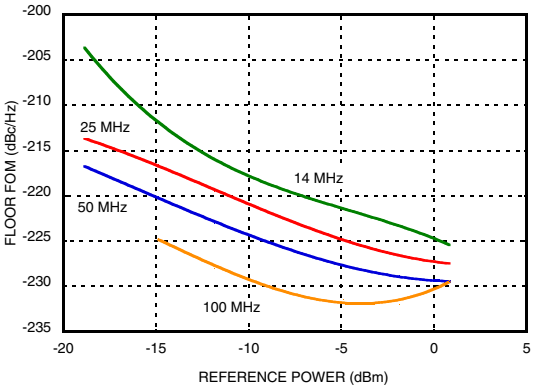


Figure 23. Reference Input Return Loss [10]

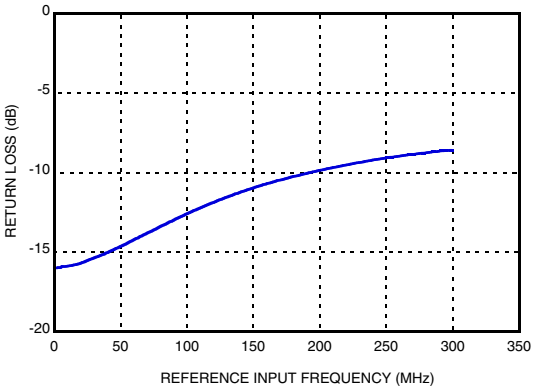
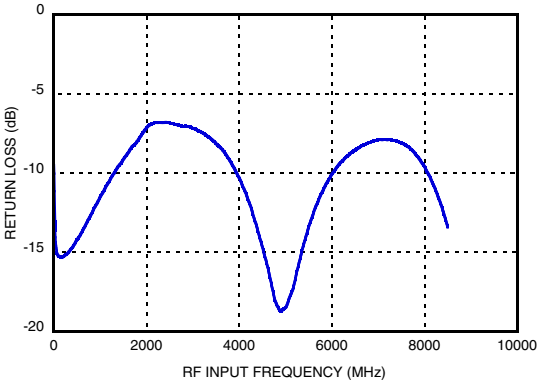


Figure 24. RF Input Return Loss [11]



[9] Measured with a 100 Ω external resistor termination, resulting in 50Ohm effective input impedance.. See "Reference Input Stage" for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[10] Measured with a 100 Ω external termination AC coupled on HMC703LP4E evaluation board, as in Figure 35.

[11] Measured with a 100 Ω external termination AC coupled on HMC703LP4E evaluation board, as in Figure 37.

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Figure 25. 2-Way Auto Sweep

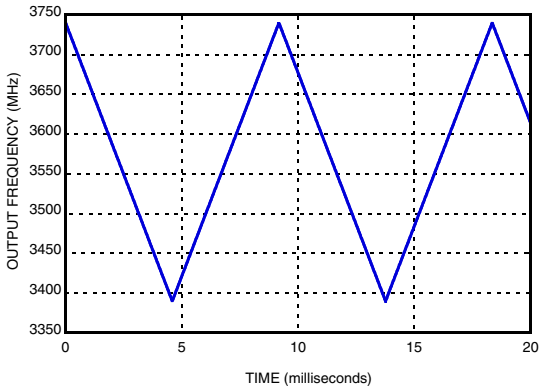

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Table 2. Pin Descriptions

Pin Number	Function	Description
1	SCK	CMOS Input: Serial port clock
2	SDI	CMOS Input: Serial port data
3	DVDD	Power Supply for digital - Nominal 3.3 V MAX 25 mA, f_{PD} dependent
4	VDDIO	Power Supply for Digital IO - 3.3 V, 8 mA MAX (only when driving LD_SDO)
5	LD_SDO	CMOS Output: General Purpose Output - Lock Detect, Serial Data Out, others, Selectable
6	TRIG	CMOS Input : External Trigger pin.
7	N/C	No Connect
8	VDDPS	Power Supply for RF Divider, Nominal 3.3 V 35 mA MAX
9	N/C	No Connect
10	VCOIP	Differential RF Inputs. Normally AC Coupled, 2 V DC bias generated internally. For Single Ended operation, RFN must be AC coupled to the ground plane, typically 100 pF ceramic. DC Bias of 2.3 V is generated internally
11	VCOIN	
12	VDDHF	Power Supply for RF Buffer, Nominal 3.3 V, 6 mA MAX
13	VDDLS	Power Supply for PFD to CP Level Shifters, Nominal 5 V, 5 mA MAX, f_{PD} dependent.
14	VDDCPA	Power Supply for charge pump, Nominal 5 V, 10 mA MAX
15	CP	Charge pump output
16	AVDD	Power supply for analog bias generation, Nominal 3.3 V, 2 mA MAX
17	BIAS	External bypass decoupling for precision bias circuits, 1.920 V +/-2 mV NOTE: BIAS ref voltage cannot drive an external load. Must be measured with 10 GΩ meter such as Agilent 34410A, normal 10 MΩ DVM will read erroneously.
18	RVDD	Power Supply for Reference path, Nominal 3.3 V. 15 mA MAX reference dependent
19	N/C	No Connect
20	XREFP	Reference Input. DC bias is generated internally. Normally AC coupled externally.
21	VDDPD	Power Supply for phase detector. Nominally 3.3 V. Decoupling for this supply is critical. 5 mA MAX, f_{PD} dependent
22	N/C	No Connect
23	CEN	CMOS Input: Hardware Chip Enable
24	SEN	CMOS Input: Serial port latch enable

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Table 3. Absolute Maximum Ratings

Parameter	Rating
Max Vdc to paddle on supply pins 3,4,8,12,16,18,21	-0.3 V to +3.6 V
VDDLS, VPPCP	-0.3 V to +5.5 V
VCOIN, VCOIP Single Ended DC	VCCHF -0.2 V
VCOIN, VCOIP Differential DC	5.2 V
VCOIN, VCOIP Single Ended AC 50Ohm	+7 dBm
VCOIN, VCOIP Differential AC 50Ohm	+13 dBm
Digital Load	1 kΩ min
Digital Input 1.4 V to 1.7 V min rise time	20 nsec
Digital Input Voltage Range	-0.25 to VDDIO+0,5 V
Thermal Resistance (Jxn to Gnd Paddle)	25 °C/W
Operating Temperature Range	-40 °C to +85 °C
Storage Temperature Range	-65 °C to + 125 °C
Maximum Junction Temperature	+150 °C
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec
ESD Sensitivity HBM	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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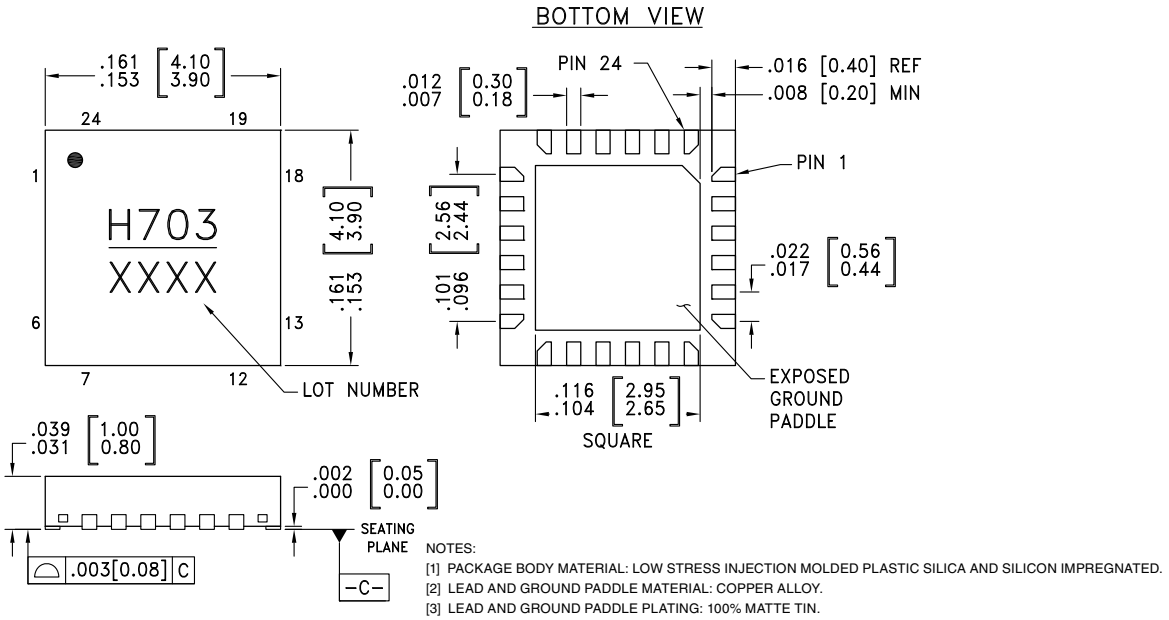
Outline Drawing



NOTES:

[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.

[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.

[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.

[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].

[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.

[6] PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.

[7] PACKAGE WARP SHALL NOT EXCEED 0.05mm

[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 4. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC703LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1[2]	H703 XXXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260°C

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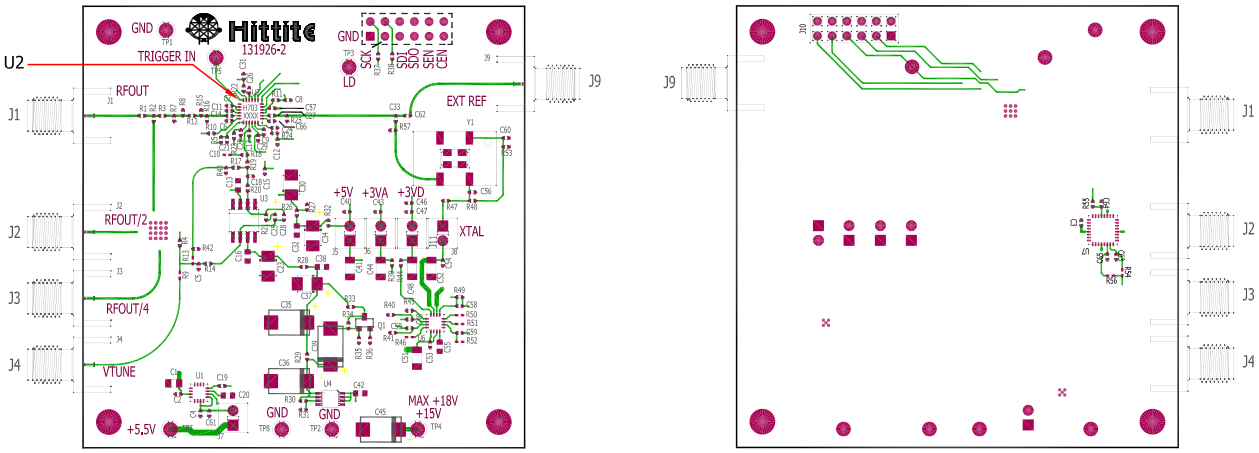
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 5. Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit	HMC703LP4E Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC703LP4E

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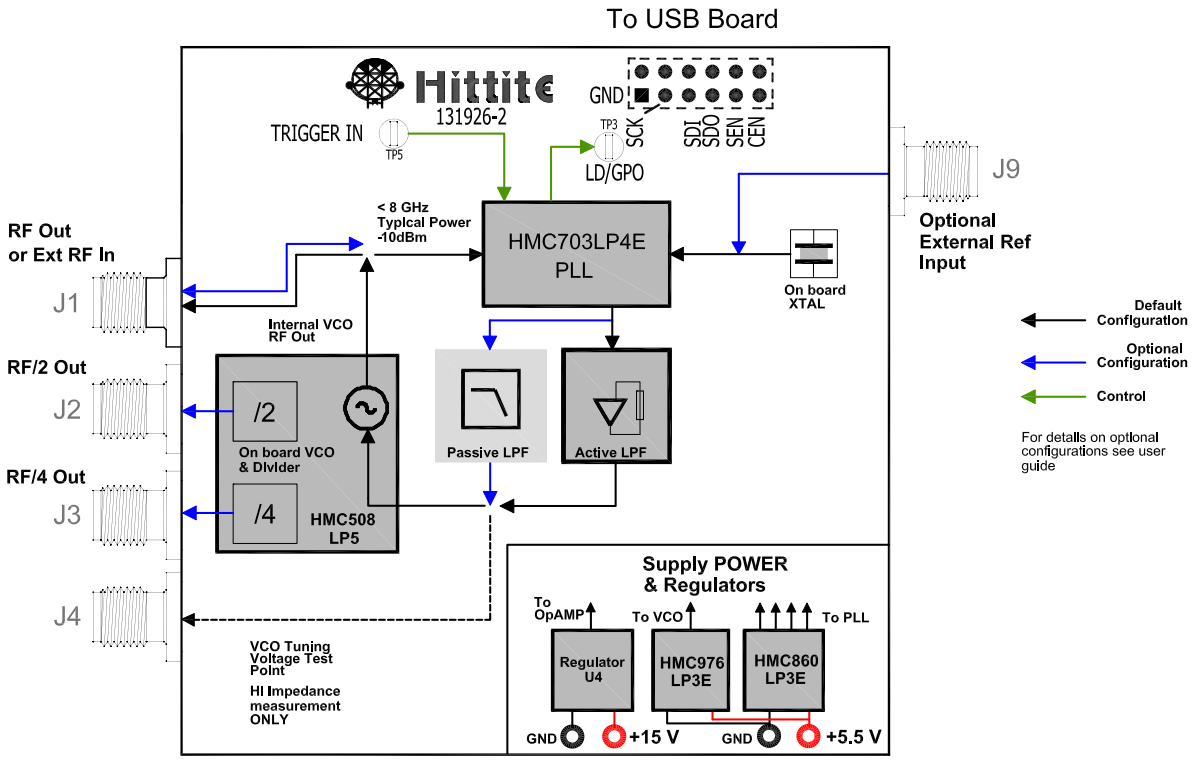
Evaluation PCB Block Diagram



Evaluation PCB Schematic

To view Evaluation PCB Schematic please visit www.hittite.com and choose HMC703LP4E from "Search by Part Number" pull down menu to view the product splash page.

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Theory Of Operation

PLL Basics

In its most trivial form, a synthesizer IC, such as the HMC703LP4E forms the heart of the control loop to multiply a low frequency reference source up to a higher frequency. The phase detector (PD) and charge-pump (CP) drive the tuning signal of a voltage-controlled oscillator in an attempt to bring the phases, at the phase-detector input, into alignment. If the loop can manage this, it means that the phase detector inputs (reference and DIV) must also be at the same frequency. Since the frequency of the DIV signal = fvco / N, this means the control loop must have forced the frequency of the VCO output must be locked to N x fpd.

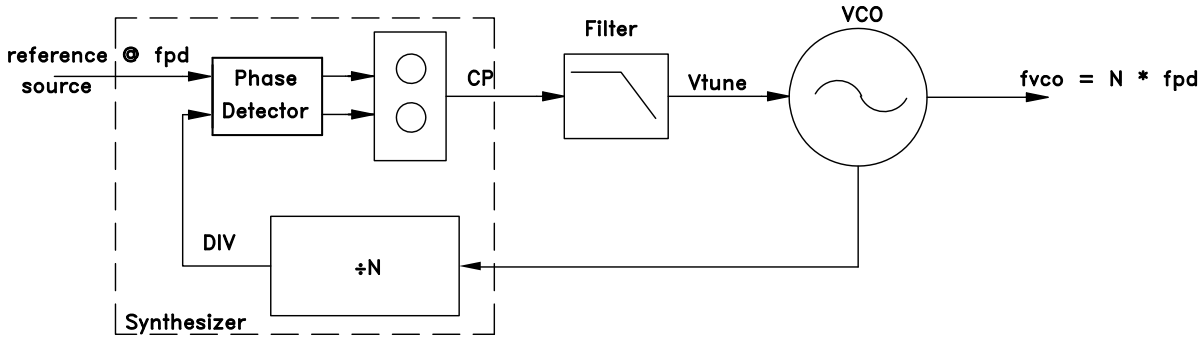

Figure 26. Typical PLL

In integer synthesizers, N can only take on discrete values (eg. 200, 201, etc.). In fractional synthesizers, such as the HMC703LP4E and others, N can also take on fractional levels, eg. N=20.4. In theory, the fractional divider normally permits higher phase-detector frequencies for a given output frequency, with associated improvements in signal quality (phase-noise). Unfortunately, fractional synthesizers suffer from imperfections which do not effect integer synthesizers. These problems can effect the phase noise, but more seriously they tend to manifest as spurious emissions - and these spurs are the most serious drawback of fractional synthesis.

Hittite's fractional synthesizer family (including the HMC703LP4E) offer drastic performance advantages over other fractional synthesizers in the industry.

The HMC703LP4E synthesizer consists of the following functional blocks:

1. Reference Path Input Buffer and 'R' Divider
2. VCO Path Input Buffer, RF Divide-by-2 and Multi-Modulus 'N' Divider
3. ΔΣ Fractional Modulator
4. Phase Detector
5. Charge Pump
6. Main Serial Port
7. Lock Detect and Register Control
8. Power On Reset Circuit

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High Performance Low Spurious Operation

The HMC703LP4E has been designed for the best phase noise and low spurious content possible in an integrated synthesizer. Spurious signals in a synthesizer can occur in any mode of operation and can come from a number of sources.

Figure of Merit, Noise Floor, and Flicker Noise Models

The phase noise of an ideal phase locked oscillator is dependent upon a number of factors:

- **a.** Frequency of the VCO, and the Phase detector
- **b.** VCO Sensitivity, kvco, VCO and Reference Oscillator phase noise profiles
- **c.** Charge Pump current, Loop Filter and Loop Bandwidth
- **d.** Mode of Operation: Integer, Fractional modulator style

The contributions of the PLL to the output phase noise can be characterized in terms of a Figure of Merit (FOM) for both the PLL noise floor and the PLL flicker (1/f) noise regions, as follows:

where:

Φ_p^2	Phase Noise Contribution of the PLL (rads²/Hz)
f_o	Frequency of the VCO (Hz)
f_{pd}	Frequency of the Phase Detector (Hz)
f_m	Frequency offset from the carrier (Hz)
F_{po}	Figure of Merit (FOM) for the phase noise floor
F_{p1}	Figure of Merit (FOM) for the flicker noise region

PLL Phase Noise Contribution

$$\Phi_p^2(f_m, f_{pd}) = \frac{F_{p1} f_0^2}{f_m} + \frac{F_{p0} f_0^2}{f_{pd}} \quad \textit{(EQ 1)}$$

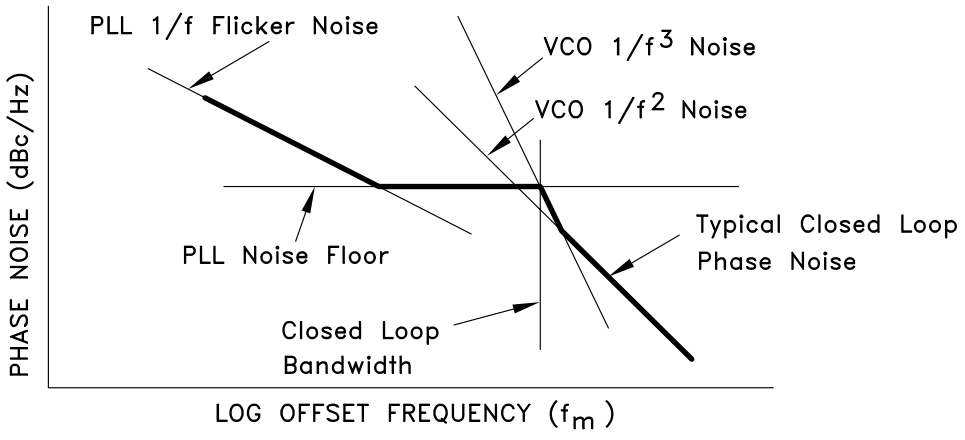

Figure 27. Figure of Merit Noise Models for the PLL

If the free running phase noise of the VCO is known, it may also be represented by a figure of merit for both $1/f^2$, F_{v2}, and the $1/f^3$, F_{v3}, regions.

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VCO Phase Noise Contribution

$$\mathcal{L}_n^2(f_m) = \frac{F_{n2} f_0^2}{f_m^2} + \frac{F_{n3} f_0^2}{f_m^3} \quad \textit{(EQ 2)}$$

The Figures of Merit are essentially normalized noise parameters for both the PLL and VCO that can allow quick estimates of the performance levels of the PLL at the required VCO, offset and phase detector frequency. Normally, the PLL IC noise dominates inside the closed loop bandwidth of the synthesizer, and the VCO dominates outside the loop bandwidth at offsets far from the carrier. Hence a quick estimate of the closed loop performance of the PLL can be made by setting the loop bandwidth equal to the frequency where the PLL and free running phase noise are equal.

The Figure of Merit is also useful in estimating the noise parameters to be entered into a closed loop design tool such as Hittite PLL Design, which can give a much more accurate estimate of the closed loop phase noise and PLL loop filter component values.

Given an optimum loop design, the approximate closed loop performance is simply given by the minimum of the PLL and VCO noise contributions.

PLL-VCO Noise

$$\mathcal{L}^2 = \min\left(\mathcal{L}_p^2, \mathcal{L}_n^2\right) \quad \textit{(EQ 3)}$$

An example of the use of the FOM values to make a quick estimate of PLL performance: Estimate the phase noise of an 8 GHz closed loop PLL with a 100 MHz reference operating in Fractional Mode B with the VCO operating at 8 GHz and the VCO divide by 2 port driving the PLL at 4 GHz. Assume an HMC509 VCO has free running phase noise in the $1/f^2$ region at 1 MHz offset of -135 dBc/Hz and phase noise in the $1/f^3$ region at 1 kHz offset of -60 dBc/Hz.

F_{v1_dB} =	-135	Free Running VCO PN at 1MHz offset
	+20*log10(1e6)	PNoise normalized to 1Hz offset
	-20*log10(8e9)	Pnoise normalized to 1Hz carrier
	= -213.1 dBc/Hz at 1Hz	VCO FOM
F_{v3_dB} =	-60	Free Running VCO PN at 1kHz offset
	+30*log10(1e3)	PNoise normalized to 1Hz offset
	-20*log10(8e9)	Pnoise normalized to 1Hz carrier
	= -168 dBc/Hz at 1Hz	VCO Flicker FOM

We can see from Figure 3 and Figure 4 respectively that the PLL FOM floor and FOM flicker parameters in fractional Mode A:

Fpo_dB = -227 dBc/Hz at 1Hz
Fp1_dB = -266 dBc/Hz at 1Hz

Each of the Figure of Merit equations result in straight lines on a log-frequency plot. We can see in the example below the resulting

PLL floor at 8 GHz = F_{po_dB} +20log10(fvco) -10log10(fpd) = -227+198 -80 = -109 dBc/Hz
PLL Flicker at 1 kHz = F_{p1_dB}+20log10(fvco)-10log10(fm) = -266 +198-30 = -98 dBc/Hz
VCO at 1 MHz = F_{v1_dB}+20log10(fvco)-20log10(fm)= -213 +198-120 = -135 dBc/Hz
VCO flicker at 1 kHz = F_{v3_dB}+20log10(fvco)-30log10(fm)= -168 +198-90 = -60 dBc/Hz

These four values help to visualize the main contributors to phase noise in the closed loop PLL. Each falls on a linear line on the log-frequency phase noise plot shown in Figure 27.

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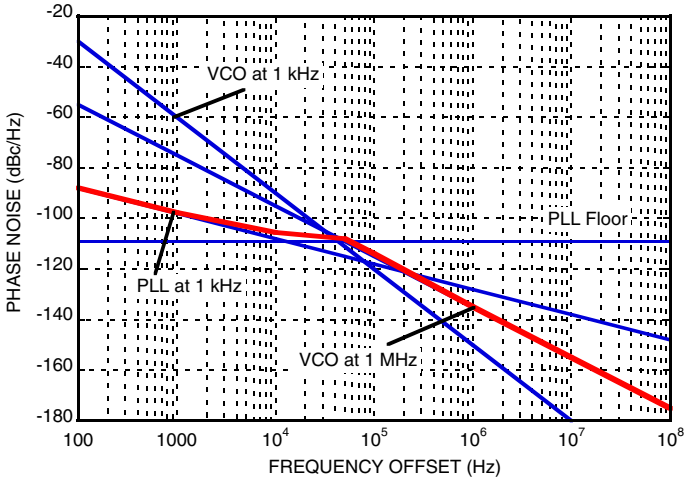

Figure 28. Figure of Merit Example

It should be noted that actual phase noise near the corner frequency of the loop bandwidth is affected by loop parameters and one should use a more complete design tool such as Hittite PLL Design for better estimates of the phase noise performance. Noise models for each of the components in Hittite PLL Design can be derived from the FOM equations or can be provided by Hittite applications engineering.

Spurious Performance

Integer Operation

The VCO always operates at an integer multiple of the PD frequency in an integer synthesizer. In general, spurious signals originating from an integer synthesizer can only occur at multiples of the PD frequency. These unwanted outputs are often simply referred to as reference sidebands.

Spurs unrelated to the reference frequency must originate from outside sources. External spurious sources can modulate the VCO indirectly through power supplies, ground, or output ports, or bypass the loop filter due to poor isolation of the filter. It can also simply add to the output of the synthesizer.

The HMC703LP4E has been designed and tested for ultra-low spurious performance. Reference spurious levels are typically below -100 dBc with a well designed board layout. A regulator with low noise and high power supply rejection, such as the HMC860LP3E, is recommended to minimize external spurious sources.

Reference spurious levels of below -100 dBc require superb board isolation of power supplies, isolation of the VCO from the digital switching of the synthesizer and isolation of the VCO load from the synthesizer. Typical board layout, regulator design, demo boards and application information are available for very low spurious operation. Operation with lower levels of isolation in the application circuit board, from those recommended by Hittite, can result in higher spurious levels.

Of course, if the application environment contains other interfering frequencies unrelated to the PD frequency, and if the application isolation from the board layout and regulation are insufficient, then the unwanted interfering frequencies will mix with the desired synthesizer output and cause additional spurs. The level of these spurs is dependant upon isolation and supply regulation or rejection (PSRR).

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Fractional Operation

Unlike an integer synthesizer, spurious signals in a fractional synthesizer can occur due to the fact that the VCO operates at frequencies unrelated to the PD frequency. Hence intermodulation of the VCO and the PD harmonics can cause spurious sidebands. Spurious emissions are largest when the VCO operates very close to an integer multiple of the PD. When the VCO operates exactly at a harmonic of the PD then, no in-close mixing products are present.

Interference is always present at multiples of the PD frequency, f_{pd}, and the VCO frequency, f_{vco}. If the fractional mode of operation is used, the difference, Δ, between the VCO frequency and the nearest harmonic of the reference, will create what are referred to as integer boundary spurs. Depending upon the mode of operation of the synthesizer, higher order, lower power spurs may also occur at multiples of integer fractions (sub-harmonics) of the PD frequency. That is, fractional VCO frequencies which are near $nf_{pd} + f_{pd}d/m$, where n, d and m are all integers and d≤m (mathematicians refer to d/m as a rational number). We will refer to $f_{pd}d/m$ as an integer fraction. The denominator, m, is the order of the spurious product. Higher values of m produce smaller amplitude spurious at offsets of mΔ and usually when m>4 spurs are very small or unmeasurable.

The worst case, in fractional mode, is when d=1, and the VCO frequency is offset from nf_{pd} by less than the loop bandwidth. This is the "in-band fractional boundary" case.

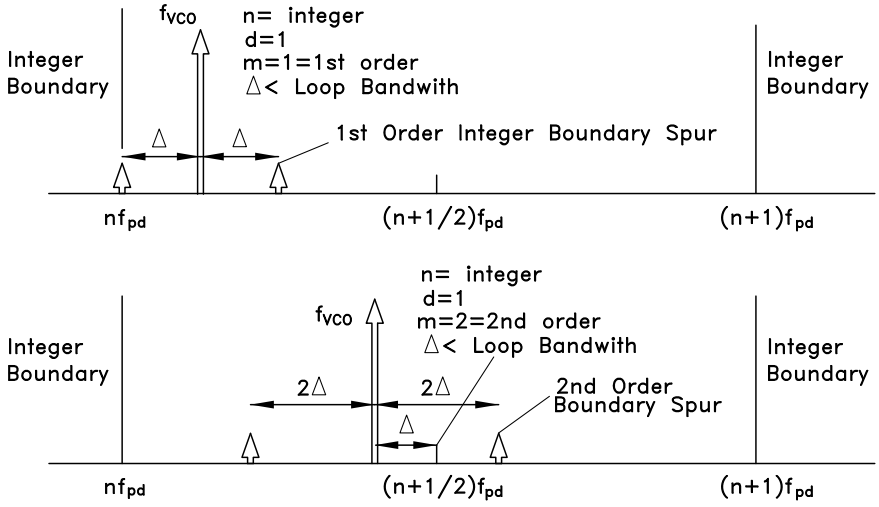

Figure 29. Fractional Spurious Example

Characterization of the levels and orders of these products is not unlike a mixer spur chart. Exact levels of the products are dependent upon isolation of the various synthesizer parts. Hittite can offer guidance about expected levels of spurious with our PLL and VCO application boards. Regulators with high power supply rejection ratios (PSRR) are recommended, especially in noisy applications.

When operating in fractional mode, charge pump and phase detector linearity is of paramount importance. Any non-linearity degrades phase noise and spurious performance. Phase detector linearity degrades when the phase error is very small and is operating back and forth between reference lead and VCO lead. To mitigate these non-linearities in fractional mode it is critical to operate the phase detector with some finite phase offset such that either the reference or VCO always leads. To provide a finite phase error, extra current sources can be enabled which provide a constant DC current path to VDD (VCO leads always) or ground (reference leads always). These current sources are called charge pump offset and they are controlled via Reg 09h. The time offset at the phase detector should be ~2.5 ns + 4 T_{ps}, where T_{ps} is the RF period at the fractional prescaler input in nanoseconds (ie. after the optional fixed divide by 2). The specific level of charge pump offset current is determined by this time offset, the comparison frequency and the charge pump current and can be calculated from:

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$$\text{Required CP Offset} = (2.5 \cdot 10^{-9} + 4T_{PS}) \cdot (F_{comparison}) \cdot I_{CP} \text{ where:} \quad \textbf{(EQ 4)}$$

T_{PS}: is the RF period at the fractional prescaler input

I_{CP}: is the full scale current setting of the switching charge pump

Note that this calculation can be performed for the center frequency of the VCO, and does not need refinement for small differences (<25%) in center frequencies. Also, operation with unreasonably large charge pump offset may cause Lock Detect to incorrectly indicate an unlocked condition. To correct, reduce the offset to recommended levels.

Another factor in Fractional spectral performance is the choice of the Delta-Sigma Modulator mode. Mode B is normally recommended, as it allows higher PD frequencies and makes it easier to filter the fractional quantization noise. For low prescaler frequencies (<1.5GHz), however, mode A can offer better in-band spectral performance. See Reg 06h[0] for DSM mode selection. Finally, all fractional synthesizers create fractional spurs at some level. Hittite offers the lowest level fractional spurious in the industry in an integrated solution.

Operational Modes

The HMC703LP4E can operate in a eight of different modes (Reg 06h[7:5]), and supports "Triggering" from 3 different sources. The modes of operation include:

"Integer Mode"

"Fractional Mode"

"Exact Frequency Mode"

Frequency Modulation "FM Mode"

Phase Modulation "PM Mode"

"Frequency Sweep Mode" (3 types)

All modes require Fractional mode to be enabled except for Integer mode. Fractional mode allows fine frequency steps. Exact Frequency mode allows precise fractional frequency steps with zero frequency error. FM and PM modes can be used for simple communications links, with data rate limitations set by the loop filter bandwidth. The PM mode also allows for precise incremental phase adjustments, which can be important in phased arrays and other systems. Frequency sweep supports built-in one-way, two-way, or user defined frequency sweeps, useful in FMCW radar applications.

Depending on the mode, the auxiliary registers Reg 0Ah, Reg 0Ch and Reg 0Dh are used for different functions, as shown in Table 6.

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Table 6. Operational Modes

Register Number	Register Name	PLL Operating Mode (SD_MODE = Reg 06h[7:5])					
		0	1	2	3	4	5 to 7
		Fractional Mode	Integer Mode	Exact Frequency Mode	FM (Frequency Modulation) Mode	PM (Phase Modulation) Mode	Ramp Mode
Function of Reg 03h	N Integer Part	Nint	N	Nint	Freq 1: Nint	Nint	Start Nint
Function of Reg 04h	N Fractional Part	Nfrac		Nfrac	Freq 1: Nfrac	Nfrac	Start Nfrac
Function of Reg 0Ah	Aux Register					Phase Step	Frequency step / reference clock
Function of Reg 0Ch	Alternate Integer				Freq 2: Nint		STOP Nint
Function of Reg 0Dh	Alternate Fractional			Channels / PD frequency	Freq 2: Nfrac		STOP Nfrac
Additional Functionality							
Double Buffer		YES	NO	YES	YES	YES	YES
On Trigger		Updates frequency, optionally initiates phase		Updates frequency, optionally initiates phase	Toggles frequency (level sensitive)	Increments / decrements phase	Proceeds to next stage of ramp

Those registers which are unused in a particular mode can take on any value, and are ignored.

Triggering

Depending on the operating mode, a trigger event is used to change frequency, FM modulate the frequency, modulate the phase, or advance the frequency ramp profile to its next state. In general the HMC703LP4E can be triggered via one of three methods. Not all modes support all trigger methods.

1. An external hardware trigger pin-6 (TRIG)
2. SPI write to TRIG BIT in Reg 0Eh[0]
3. SPI write to fractional register Reg 04h (frequency hopping triggers only).

Depending on the mode, the part is sensitive to either the rising edge, or the level of the trigger. The SPI's TRIG bit emulates the external TRIG pin, and so it must typically be written to 1 for a trigger, and then back to 0 in preparation for another trigger cycle. To use the external TRIG pin, it must be enabled via EXTTRIG_EN (Reg 06h[9]).

Fractional Mode or Exact Frequency Mode Frequency Updates

In non-modulated fractional modes (Reg 06h[7:5] = 0 or 2), if the external trigger is enabled, writes to N_{INT} and N_{frac} (Reg 03h and Reg 04h) are internally buffered and wait for an explicit trigger via either the TRIG pin or the SPI's TRIG bit before taking effect. If EXTTRIG_EN = 0, the write to N_{INT} is double-buffered, and waits for a fractional write to Reg 04h so that both N_{INT} and N_{frac} are internally recognized together. See the "Fractional Mode" section for more information on calculating the fractional multiplier for your application.

Initial Phase Control

On the HMC703LP4E, the user has control of the initial phase of the VCO via the 24-bit SEED Reg 05h. This seed phase is loaded on the 1st clock cycle following a trigger event, provided that autoseed (Reg 06h [8] = 1) is enabled. The value in Reg 05h represents the phase of the VCO. For example, if two synthesizers are triggered in parallel, but one has a SEED of 0.2 (0.2×2^{24}) and the other has a SEED of 0.7 (0.7×2^{24}), the steady state outputs of the two VCOs

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(not accounting for any mismatch) will be 180° out of phase = ((0.7-0.2) x 360°). The user can take advantage of this for phase control of the outputs of multiple synthesizers.

If phase control is not needed, the best spurious operation is achieved with the SEED set to a busy binary number, for example 50F1CDh, or B29D08h.

Note that in Exact Frequency mode with an exact step of f_{step}, if autoseed is off, there can be a delay of up to $1/f_{step}$ after a trigger before a new fractional frequency is recognized.

Frequency Tuning

Integer Mode

In integer mode the VCO step size is fixed to that of the PD frequency, f_{pd}. Integer mode typically has lower phase noise than fractional mode for a given PD operating frequency. The advantage is usually of the order of 2 to 3 dB. Integer mode, however, often requires a lower PD frequency to meet channel step size requirements. The fractional mode advantage is that higher PD frequencies can be used, hence lower phase noise can often be realized. "Charge Pump Offset" should be disabled in integer mode. In integer mode the ΔΣ modulator is shut off and the N divider (Reg 03h) may be programmed to any integer value in the range 16 to 2^{16}-1. To use the HMC703LP4E in integer mode program Reg 06h[7:5] = 1, then program the integer portion of the frequency (as per (EQ 5)), ignoring the fractional part.

There is no double buffering in integer mode, i.e. write data then trigger the frequency change later. A write to the N_{INT} register (Reg 03h) immediately starts the RF frequency hop. There is no external trigger available in this mode. If double buffering is required, use fractional mode (Reg 06h[7:5] = 0), with N_{frac} (Reg 04h) = 0, and SEED (Reg 05h) = 0.

Fractional Mode

The HMC703LP4E is placed into fractional mode by setting SD_MODE (Reg 06h[7:5]) = 0

The frequency of a locked VCO controlled by the HMC703LP4E, f_{vco}, is given by

$$f_{ps} = \frac{f_{xtal}}{R}\,(N_{int} + N_{frac}) = f_{int} + f_{frac} \qquad \textbf{(EQ 5)}$$

$$f_{vco} = k\, f_{ps} \qquad \textbf{(EQ 6)}$$

Where:

f_{ps}	is the frequency at the prescalar input after any potential RF divide by 2
f_{vco}	is the frequency at the HMC703LP4E's RF port
k	is 1 if the RF Divide by 2 is bypassed, 2 if on (Reg 08h[17])
N_{int}	is the integer division ratio, Reg 03h, an integer between 20 and 2^{16}- 1
N_{frac}	is the fractional part, from 0.0 to 0.99999...,N_{frac}=Reg 04h/2^{24}
R	is the reference path division ratio, Reg 02h
f_{xtal}	is the frequency of the reference oscillator input
f_{pd}	is the PD operating frequency, f_{xtal}/R

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As an example, suppose we want to tune a VCO to 7910 MHz. Since the input frequency is > 4 GHz, the RF divide-by-2 must be engaged, so k=2:

f_{vco}	7,910 MHz
k	2
f_{ps}	3,955 MHz
f_{xtal}	= 50 MHz
R	= 1
f_{pd}	= 50 MHz
N_{int}	= 79
N_{frac}	= 0.1
Reg 04h	= round(0.1 x 2^{24}) = round(1677721.6) = 1677722

$$f_{ps} = \frac{50e6}{1}\left(79 + \frac{1677722}{2^{24}}\right) = 3955\ MHz + 1.2\ Hz\ error \qquad \textbf{(EQ 7)}$$

$$f_{vco} = 2\ (3955 + 1.2\ Hz) = 7910\ MHz + 2.4\ Hz\ error \qquad \textbf{(EQ 8)}$$

In this example the output frequency of 7910 MHz is achieved by programming the 16-bit binary value of 79d = 4Fh = 0000 0000 0100 1111 into *intg_reg* in Reg 03h, and the 24-bit binary value of 1677722d = 19999Ah = 0001 1001 1001 1001 1001 1010 into *frac_reg* in Reg 04h. The 2.4 Hz quantization error can be eliminated using the exact frequency mode if required.

Exact Frequency Mode

The absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example a 24 bit fractional modulator has frequency resolution set by the phase detector (PD) comparison rate divided by 2^{24}. In the case of a 50 MHz PD rate, this would be approximately 2.98 Hz, or 0.0596 ppm.

In some applications it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated. In some fractional synthesizers it is necessary to shorten the length of the accumulator (the denominator or the modulus) to accommodate the exact period of the step size. The shortened accumulator often leads to very high spurious levels at multiples of the channel spacing, $f_{step} = f_{PD}$/Modulus. For example 200 kHz channel steps with a 10 MHz PD rate requires a modulus of just 50. The Hittite method achieves the exact frequency step size while using the full 24 bit modulus, thus achieving exact frequency steps with very low spurious and a high comparison rate, which maintains excellent phase noise.

Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (eg. N = 50.0,50.5,50.25,50.75 etc.). Unfortunately, some common frequencies cannot be exactly represented. For example, N_{frac} = 0.1 = 1/10 must be approximated as round((0.1 x 2^{24})/ 2^{24}) ≈ 0.100000024. At f_{PD} = 50 MHz this translates to 1.2 Hz error. HMC703LP4E exact frequency mode addresses this issue, and can eliminate quantization error by programming the $N_{channels}$ (Reg 0Dh) to 10 (in this example). More generally, this feature can be used whenever the prescaler frequency, f_{ps}, can be exactly represented on a step plan where there are an integer number ($N_{channels}$) of frequency steps across integer-N boundaries. Assuming the RF divide by 2 is disabled so that f_{ps}=f_{vco}, this holds when the VCO frequency, f_{vco} satisfies (EQ 9), shown graphically in Figure 30.

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$$f_{VCO} \bmod f_{gcd} = 0, \quad \text{where } f_{gcd} = \gcd(f_{VCO}, f_{PD}) \qquad \textit{(EQ 9)}$$
$$N_{channels} = f_{PD} / f_{gcd}, \text{ and } N_{channels} < 2^{24}$$

Where:

f_{PD} = frequency of the Phase Detector
f_{VCO} is the desired output frequency
f_N , f_N+1 are integer multiples of the Phase Detector
f_{gcd} stands for Greatest Common Divisor
eg. f_{gcd} (4000.200MHz, 50MHz)
= *200kHz*
therefore $N_{channels}$ = *50 MHz/200 kHz = 250*
f_{VCOn} are other VCO frequencies we can exactly tune to, given this f_{gcd} spacing

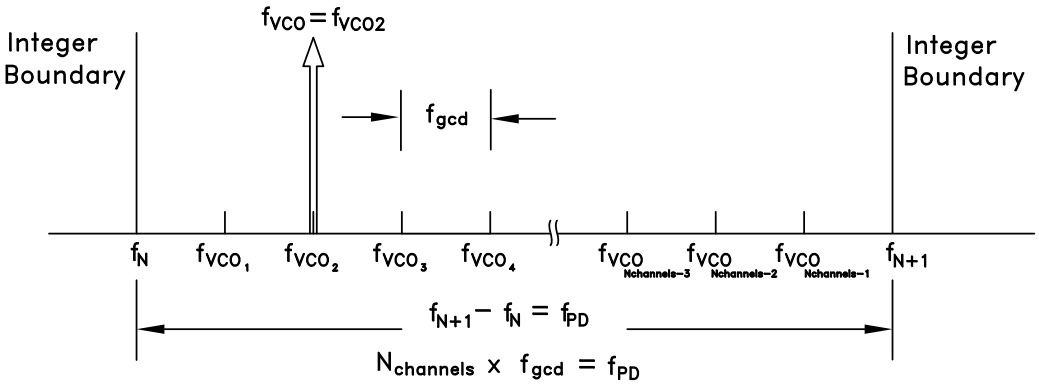

Figure 30. Exact Frequency Tuning

In the previous paragraph, it was assumed that a single frequency was to be achieved with zero error. Exact frequency mode also applies to cases where many exact frequencies are required, all of which fit on a particular channel spacing.

Example: To achieve exactly 50 kHz channel steps with a 61.44 MHz reference, calculate f_{gcd} and $N_{channels}$:

f_{PD} = 61.44 MHz
f_{step} = 50 kHz
f_{gcd} (61.44 MHz, 50 kHz)
Using the Euclidean algorithm to find the greatest common denominator:
61.440 MHz = 50 kHz x 1228 + 50 kHz
50 kHz = 40 kHz x 1 + 10 kHz
40 kHz = 10 kHz x 4 + 0 (0 remainder, algorithm complete)
f_{gcd} (61.44 MHz, 50 kHz) = 10 kHz
$N_{channels}$ = *61.44 MHz / 10 kHz = 6144*

For improved spectral performance (to keep spurs low and further out of band), it is best to keep f_{gcd} as high as possible ($N_{channels}$ as low possible) for a given application.

Using Hittite Exact Frequency Mode

To use Exact Frequency Mode, we recommend the following procedure:

1. Calculate the required f_{gcd} as either gcd(f_{VCO}, f_{PD}) or gcd(f_{PD}, f_{step}) depending on your application
2. Calculate the number of channels per integer boundary, $N_{channels}$= f_{PD} / f_{gcd} and program into Reg 0Dh
3. Set the modulator mode to Exact Frequency (SD_MODE in Reg 06h[7:5] = 2)

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Then, for each frequency of interest, f_{VCO}:

4 Calculate the approximate value of N that is required: $N = f_{VCO}/f_{PD} = N_{INT} + N_{frac}$

5. Program N_{INT} into integer register Reg 03h
   Note: There is no need to re-program N_{INT} if it has not changed from the previous set-point.
6. Program the fractional register, Reg 04h = Ceiling(N_{frac}*2^{24})
   where the ceiling function means "round up to the nearest integer."

Example: To configure HMC703LP4E for exact frequency mode with channel spacing of 50 kHz, VCO frequency = 2000.200 MHz and f_{PD} =61.44 MHz:

1. f_{gcd}(61.44 MHz, 50 kHz) = 10 kHz (as above)
2. Calculate $N_{channels}=f_{PD} / f_{gcd}$ = 6144. Program into Reg 0Dh (6144 dec = 1800 hex)
3. Set the modulator mode to Exact Frequency (SD_MODE in Reg 06h[7:5] = 2)
4. Calculate N = 2000.2 MHz / 61.44 MHz = 32.55533854 = 32 + 0.55533854
5. Program integer divisor N_{INT} (Reg 03h) = 32d = 20h
6. Program fractional divisor Reg 04h= CEILING(0.55533854 x 2^{24}) = 9,317,035 = 8E2AABh

In the above example, without exact frequency mode, there would have been a -1.2 Hz error due to quantization.

FM Mode

The HMC703LP4E PM mode supports simple FSK modulation via a level sensitive trigger. FM mode can be used for simple communications links, with data rate limitations set by the loop filter bandwidth.

The HMC703LP4E is configured to operate in FM mode by writing Reg 06h[7:5] = 3.

The FM mode allows the user to toggle between two frequencies $F_0 = N_1*f_{PD}$ and $F_1 = N_2*f_{PD}$ based on the level of the TRIG.

The following procedure is recommended to configure HMC703LP4E to FM mode:

1. Lock in fractional mode (Reg 06h[7:5]= 0) to $F_0 = f_{PD}$ x (Reg 03h.Reg 04h).
2. Program (Reg 0Ch.Reg 0Dh) for F_1.
3. Change mode to FM (Reg 06h[7:5] = 3).
4. Select the trigger source Reg 06h[9] = 1, TRIG (pin-6), or Reg 06h[9] = 0 - trigger from SPI bit Reg 0Eh[0]
5. Switch between F_0 and F_1 on a trigger state 0/1 = F_0/F_1.

It is possible to change the next frequency state between trigger events, without affecting the output - ie. write the F_0 value while on F_1, or F_1 while on F_0 .

PM Mode

The HMC703LP4E PM mode supports simple bi-phase modulation via a level sensitive trigger. PM mode also supports programmable phase steps via an edge sensitive trigger. PM modes can be used for simple communications links, with data rate limitations set by the loop filter bandwidth.

The HMC703LP4E is configured to operate in all PM mode by writing Reg 06h[7:5] = 4. In general the modulation phase step, $\Delta\theta$, in either PM mode is given by

$$\Delta\theta = \frac{x \cdot 360}{2^{24}} \quad \text{(deg)}$$

where x = Reg 0Ah.

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