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High Performance, 3.2 GHz, 14-Output Jitter Attenuator with JESD204B

Data Sheet **HMC7044**

FEATURES

- Ultralow rms jitter: 44 fs typical (12 kHz to 20 MHz) at 2457.6 MHz
- Noise floor: −156 dBc/Hz at 2457.6 MHz
- Low phase noise: −141.7 dBc/Hz at 800 kHz, 983.04 MHz output
- Up to 14 LVDS, LVPECL, or CML type device clocks (DCLKs) from PLL2
  - Maximum CLKOUTx/$\overline{\text{CLKOUTx}}$ and SCLKOUTx/$\overline{\text{SCLKOUTx}}$ frequency up to 3200 MHz
- JESD204B-compatible system reference (SYSREF) pulses
- 25 ps analog, and ½ VCO cycle digital delay independently programmable on each of 14 clock output channels
- SPI-programmable phase noise vs. power consumption
- SYSREF valid interrupt to simplify JESD204B synchronization
- Narrow-band, dual core VCOs
- Up to 2 buffered voltage controlled oscillator (VCXO) outputs
- Up to 4 input clocks in LVDS, LVPECL, CMOS, and CML modes
- Frequency holdover mode to maintain output frequency
- Loss of signal (LOS) detection and hitless reference switching
- 4× GPIOs alarms/status indicators to determine the health of the system
- External VCO input to support up to 6000 MHz
- On-board regulators for excellent PSRR
- 68-lead, 10 mm × 10 mm LFCSP package

APPLICATIONS

- JESD204B clock generation
- Cellular infrastructure (multicarrier GSM, LTE, W-CDMA)
- Data converter clocking
- Microwave baseband cards
- Phase array reference distribution

GENERAL DESCRIPTION

The HMC7044 is a high performance, dual-loop, integer-N jitter attenuator capable of performing reference selection and generation of ultralow phase noise frequencies for high speed data converters with either parallel or serial (JESD204B type) interfaces. The HMC7044 features two integer mode PLLs and overlapping on-chip VCOs that are SPI-selectable with wide tuning ranges around 2.5 GHz and 3 GHz, respectively. The device is designed to meet the requirements of GSM and LTE base station designs, and offers a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs. The HMC7044 provides 14 low noise and configurable outputs to offer flexibility in interfacing with many different components including data converters, field-programmable gate arrays (FPGAs), and mixer local oscillators (LOs).

The DCLK and SYSREF clock outputs of the HMC7044 can be configured to support signaling standards, such as CML, LVDS, LVPECL, and LVCMOS, and different bias settings to offset varying board insertion losses.

FUNCTIONAL BLOCK DIAGRAM

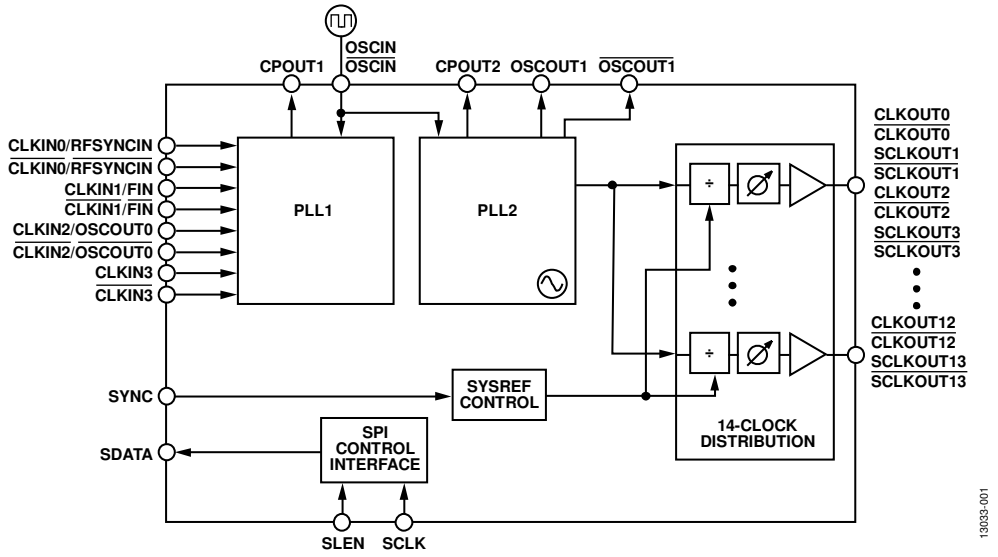

Figure 1.

Rev. B Document Feedback

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Data Sheet

- HMC7044: High Performance, 3.2 GHz, 14-Output Jitter Attenuator with JESD204B Data Sheet

User Guides

- UG-826: Evaluating the HMC7044 Dual Loop Clock Jitter Cleaner

TOOLS AND SIMULATIONS

- HMC7044 IBIS Model

REFERENCE MATERIALS

Press

- Analog Devices Clock Jitter Attenuator Optimizes JESD204B Serial Interface Functionality in Base Station Designs

Technical Articles

- Synchronizing Sample Clocks of a Data Converter Array

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- HMC7044 Material Declaration
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SPECIFICATIONS

Unless otherwise noted, f_{VCXO} = 122.88 MHz single-ended; CLKIN0/$\overline{\text{CLKIN0}}$, CLKIN1/$\overline{\text{CLKIN1}}$, CLKIN2/$\overline{\text{CLKIN2}}$, and CLKIN3/$\overline{\text{CLKIN3}}$ differential at 122.88 MHz; f_{VCO} = 2949.12 MHz; doubler is on; typical value is given for V_{CC} = 3.3 V; and T_A = 25°C. Minimum and maximum values are given over the full V_{CC} and T_A (−40°C to +85°C) variation, as listed in Table 1. Note that multifunction pins, such as CLKIN0/RFSYNCIN, are referred to either by the entire pin name or by a single function of the pin, for example, CLKIN0, when only that function is relevant.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE, V_{CC}					
VCC1_VCO	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for VCO and VCO distribution
VCC2_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 2 and Output Channel 3
VCC3_SYSREF	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for common SYSREF divider
VCC4_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 4, Output Channel 5, Output Channel 6, Output Channel 7
VCC5_PLL1	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for the LDO used in PLL1
VCC6_OSCOUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for oscillator output path
VCC7_PLL2	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for the LDO used in PLL2
VCC8_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 8, Output Channel 9, Output Channel 10, and Output Channel 11
VCC9_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 0, Output Channel 1, Output Channel 12, and Output Channel 13
TEMPERATURE					
Ambient Temperature Range, T_A	−40	+25	+85	°C	

SUPPLY CURRENT

For detailed test conditions, see Table 22 and Table 23.

Table 2.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT CONSUMPTION[3]					
VCC1_VCO		157	225	mA	
VCC2_OUT[4]		65	250	mA	Typical value is given at T_A = 25°C with two LVDS clocks at divide by 8
VCC3_SYSREF		12	37	mA	
VCC4_OUT[4]		78	500	mA	Typical value is given at 25°C with two LVPECL high performance clocks, fundamental frequency of internal VCO (f_O), 2 SYSREF clocks (off)
VCC5_PLL1		39	125	mA	
VCC6_OSCOUT		0	80	mA	
VCC7_PLL2		46	80	mA	
VCC8_OUT[4]		124	500	mA	Typical value is given at 25°C with two LVPECL high performance clocks at divide by 2, 2 SYSREF clocks (off)
VCC9_OUT[4]		65	500	mA	Typical value is given at 25°C with two LVDS clocks at divide by 8, 2 SYSREF clocks (off)
Total Current		586		mA	

[1] Maximum values are guaranteed by design and characterization.
[2] Currents include LVPECL termination currents.
[3] Maximum values are for all circuits enabled in their worst case power consumption mode, PVT variations, and accounting for peak current draw during temporary synchronization events.
[4] Typical specification applies to a normal usage profile (Profile 1 in Table 23), where PLL1 and PLL2 are locked, but very low duty cycle currents (sync events) and some optional features are disabled. This specification assumes output configurations as described in the test conditions/comments column.

DIGITAL INPUT/OUTPUT (I/O) ELECTRICAL SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT SIGNALS (RESET, SYNC, SLEN, SCLK)					
Safe Input Voltage Range[1]	−0.1		+3.6	V	
Input Load		0.3		pF	
Input Voltage					
Input Logic High (V_{IH})	1.2		V_{CC}	V	
Input Logic Low (V_{IL})	0		0.5	V	
SPI Bus Frequency			10	MHz	
DIGITAL BIDIRECTIONAL SIGNALS CONFIGURED AS INPUTS (SDATA, GPIO4, GPIO3, GPIO2, GPIO1)					
Safe Input Voltage Range[1]	−0.1		+3.6	V	
Input Capacitance		0.4		pF	
Input Resistance		50G		Ω	
Input Voltage					
Input Logic High (V_{IH})	1.22		V_{CC}	V	
Input Logic Low (V_{IL})	0		0.24	V	
Input Hysteresis		0.2		V	Occurs around 0.85 V
GPIO1 TO GPIO4 ALARM MUXING/DELAY					
Delay from Internal Alarm/Signal to General-Purpose Output (GPO) Driver		2		ns	Does not include t_{DGPO}
DIGITAL BIDIRECTIONAL SIGNALS CONFIGURED AS OUTPUTS (SDATA, GPIO4, GPIO3, GPIO2, GPIO1)					
CMOS MODE					
Logic 1 Level	1.6	1.9	2.2	V	
Logic 0 Level		0	0.1	V	
Output Drive Resistance (R_{DRIVE})		50		Ω	
Output Driver Delay (t_{DGPO})		1.5 + 42 × C_{LOAD}		ns	Approximately 1.5 ns + 0.69 × R_{DRIVE} × C_{LOAD} (C_{LOAD} in nF)
Maximum Supported DC Current[1]			0.6	mA	
OPEN-DRAIN MODE[1]					External 1 kΩ pull-up resistor
Logic 1 Level			3.6	V	3.6 V maximum permitted; specifications set by external supply
Logic 0 Level		0.13	0.28	V	Against a 1 kΩ external pull-up resistor to 3.3 V
Pull-Down Impedance		60		Ω	
Maximum Supported Sink Current			5	mA	

[1] Guaranteed by design and characterization.

PLL1 CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL1 REFERENCE INPUTS (CLKIN0/$\overline{\text{CLKIN0}}$, CLKIN1/$\overline{\text{CLKIN1}}$, CLKIN2/$\overline{\text{CLKIN2}}$, CLKIN3/$\overline{\text{CLKIN3}}$)					
Reliable Signal Swing					
Differential	0.375		1.4	V p-p	Differential, keep signal at reference input pin <2.8 V, measured at 800 MHz
Single-Ended[1]	0.375		1.4	V p-p	<250 MHz; keep signal at reference input pin <2.8 V
Common-Mode Range	0.4		2.4	V	If user supplied, on-chip V_{CM} is approximately 2.1 V
Input Impedance		100 to 2000		Ω	User selectable; differential
Return Loss		−12		dB	When terminated with 100 Ω differentially
PLL1 REFERENCE DIVIDER					
8-Bit Lowest Common Multiple (LCM) Dividers	1		255		
16-Bit R Divider (R1)	1		65,535		
PLL1 FEEDBACK DIVIDER					
16-Bit N Divider (N1)	1		65,535		
PLL1 FREQUENCY LIMITATIONS					
PLL1 REF Input Frequency (f_{REF})	0.00015		800	MHz	Minimum specification set by Phase Detector 1 (PD1) low limit
Digital LOS/LCM Frequency (f_{LCM})	0.00015		123	MHz	Typically run at about 38.4 MHz
PD1 Frequency (f_{PD1})	0.00015		50	MHz	Minimum specification = VCXO minimum frequency ÷ 65,535; 9.76 MHz typical
PLL1 CHARGE PUMP					
Charge Pump Current Range (I_{CP1})		120 to 1920		µA	I_{CP1} from 0 to 15, VCXO control voltage (V_{TUNE}) = 1.4 V
I_{CP1} Variation over Process Voltage Temperature (PVT)		±15		%	V_{TUNE} = 1.4 V
Source/Sink Current Mismatch		2		%	Source/sink mismatch at 1.4 V
Charge Pump Current Step Size		120		µA	
Charge Pump Compliance Range[1]		0.4 to 2.5		V	I_{CP} variation less than 10%
		0.1 to 2.7		V	Maintain lock in test environment
PLL1 NOISE PROFILE[1]					
Floor Figure of Merit (FOM)		−222		dBc/Hz	Normalized to 1 Hz
Flicker FOM		−252		dBc/Hz	Normalized to 1 Hz
Flicker Noise		Determined by formula[2]		dBc/Hz	At f_{OUT}, f_{OFFSET}
Noise Floor		Determined by formula[3]		dBc/Hz	At f_{OUT}, f_{PD1}
Total Phase Noise (Unfiltered)		Determined by formula[4]		dBc/Hz	
PLL1 BANDWIDTH AND ACQUISITION TIMES[1]					
Supported Loop Bandwidths (PLL1_BW)[5]	$f_{LCM}/2^{25}$		$f_{PD1}/10$	Hz	Typically PLL1 low BW is set by the application and ranges between 5 Hz and 2 kHz
PLL1 Slew Time[6]			N1/ f_{DELTA_VCXO}	sec	N1 = 10 (typical) and f_{DELTA_VCXO} = 10 kHz (typical) results in 1 ms of slew time
PLL1 Linear Acquisition Time		5/PLL1_BW		sec	When VCXO has stopped slewing to steady state (within 5°)
PLL1 Phase Error at PD1 Invalidates Lock		±2.9		ns	
PLL1 Lock Detect Timer Period (t_{LKD})[7]		4 to 2^{26}		t_{LCM}	User-selectable low phase error counts to declare lock

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL1 BEHAVIOR ON REFERENCE FAILURE[1]					
LOS Assertion Delay[7]	2 + t_{DGPO}		3 + t_{DGPO}	t_{LCM}	From missing signal edge to alarm on GPO
Erroneously Active I_{CP1} Time on Reference Failure[8]	0		8	ns	
Temporary Frequency Glitch Due to Reference Failure		0.03		ppm	I_{CP1} = 1 mA, C12 = 4.6 nF, Crystek CVPD-952 VCXO
Integrated Frequency Error Due to Reference Failure		0.016		ppm	I_{CP1} = 1 mA, C13 = 1 µF, Crystek CVPD-952 VCXO
Signal Valid Time to Clear LOS[9]	2		3	t_{LOSVAL}	
PLL1 V_{TUNE} LEAKAGE SOURCES					
Charge Pump Tristate Leakage Current		0.2		nA	
Board Level XTAL Tune Input Port		0.5		nA	Crystek CVPD-952 VCXO
Board Level Loop Filter Components		2		nA	C12 = 4.6 nF, C13 = 1 µF, R9 = 11 kΩ, C15 = unpopulated
HOLDOVER CHARACTERISTICS					
V_{TUNE} Drift Over 1 sec in Tristate Mode		2		mV	C12 = 4.6 nF, C13 = 1 µF, R9 = 11 kΩ, CVPD-950 VCXO
Holdover					
Analog-to-Digital Converter (ADC)/Digital-to-Analog Converter (DAC) Resolution		19		mV	7-bit, monotonic, no missing code
ADC/DAC Code 0 Voltage		0.28		V	
ADC/DAC Code 127 Voltage		2.71		V	
DAC Temperature Stability		0.07		mV/°C	At maximum code
ADC/DAC Integral Nonlinearity (INL)		−0.11		LSBs	Worst case across codes
Holdoff Timer Period[1, 10]	1		2^{26}	t_{LCM}	
HOLDOVER EXIT—INITIAL PHASE OFFSETS[1]					
Exit Criteria = Wait for Low Phase Error					The phase offset to make up after a transition from holdover to acquisition when using this feature
Exit Action = None		±4		ns	
Exit Criteria = Any[11]					
Exit Action = Reset Dividers	1		2	t_{VCXO}	Assumes N2 > 3 and dividers are reset upon exit; note that VCXO lags at start; value applies as the starting phase error if DAC assisted release is used
Exit Action = None			±N1	t_{VCXO}	Dividers are not reset upon exit
HOLDOVER EXIT CHARACTERISTICS[1, 12]					
DAC Assisted Release Period per Step ($t_{DACASSIST}$)	1/2		1/16	t_{LKD}	Based on lock detect timer setpoint
DAC Assisted Release Time			9	$t_{DACASSIST}$	Time from decision to leave holdover until in fully natural acquisition; assumes no interruption by LOS or user
Delay of Exit Criteria[13] = Wait for Low Phase Error[14]			N1/f_{ERR_VCXO}	sec	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER EXIT—FREQUENCY TRANSIENTS vs. MODE					
Peak Frequency Transient					
DAC Assisted Release		2		ppm	Only available if using DAC-based holdover

[1] Guaranteed by design and characterization.
[2] See the PLL1 Noise Calculations section for more information on how to calculate the flicker noise for PLL1.
[3] See the PLL1 Noise Calculations section for more information on how to calculate the noise floor for PLL1.
[4] See the PLL1 Noise Calculations section for more information on how to calculate the total phase noise (unfiltered) for PLL1.
[5] Set by external components. Set the lock detect thresholds (PLL1 Lock Detect Timer[4:0] in Register 0x0028) appropriately in the SPI.
[6] Depends on initial phase offset (worst case is proportional to N1) and VCXO excess tuning range available over the target (f_{DELTA_VCXO}). For PFD rates typical of PLL1, cycle slipping is normally insignificant.
[7] t_{LCM} is the least common multiple (LCM) of PLL1 clock input frequencies. The specification is given in multiples of t_{LCM}.
[8] If LOS triggers before the PFD edge is normally detected (more likely with high R1 values), the charge pump is more likely to disable before the next invalid comparison occurs. Otherwise, the fast tristate circuit disables the charge pump after about 4 ns (8 ns worst case) of phase error.
[9] t_{LOSVAL} is a register value that is programmable from 1, 2, 4, …, 64 t_{LCM}.
[10] If the holdoff timer is used, the finite state machine (FSM) stays in holdover after LOS of the active reference before switching clocks, giving the original clock a chance to return.
[11] t_{VCXO} is the VCXO clock period.
[12] See the PLL1 Holdover Exit section.
[13] The time required for the phases to intersect is inversely proportional to the holdover frequency error. Note that the frequency error during holdover is expected to be much smaller than is available from the tuning range of the VCXO.
[14] f_{ERR_VCXO} is the error frequency of the VCXO.

PLL2 CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL2 VCXO INPUT					
Recommended Swing					
Differential	0.2		1.4	V p-p	Differential, keep signal at OSCIN and $\overline{\text{OSCIN}}$ pins < 2.8 V
Single-Ended (<250 MHz)[1]	0.2		1.4	V p-p	Keep signal at OSCIN and $\overline{\text{OSCIN}}$ pins < 2.8 V
Common-Mode Range	1.6	2.1	2.4	V	If user supplied, on-chip V_{CM} is approximately 2.1 V
VCXO Input Slew Rate	300			mV/ns	Slew rates as low as 100 mV/ns are functional, but can degrade the phase noise plateau by about 3 dB
Input Capacitance		1.5		pF	Per side; 3 pF differential
Differential Input Resistance		100 to 1000		Ω	User selectable
Return Loss		−12		dB	When terminated with 100 Ω differential
PLL2 EXTERNAL VCO INPUT					
Recommended Input Power, AC-Coupled					
Differential	−6		6	dBm	
Single-Ended[1]	−6		6	dBm	
Return Loss		−12		dB	When terminated with 100 Ω differential
External VCO Frequency[1]	400		3200	MHz	Fundamental mode; if < 1 GHz, set the low frequency external VCO path bit (Register 0x0064, Bit 0)
	400		6000	MHz	Using external VCO ÷ 2
Common-Mode Range[1]	1.6	2.1	2.2	V	
PLL2 DIVIDERS					
12-Bit Reference Divider Range (R2)	1		4095		
16-Bit Feedback Divider Range (N2)	8		65,535		
PLL2 FREQUENCY LIMITATIONS					
VCXO Frequency (f_{VCXO})	10		500	MHz	122.88 MHz or 155 MHz are typical
VCXO Duty Cycle					
Using Doubler[1]	40		60	%	Distortion can lead to a spur at $f_{PD}/2$ offset, note that minimum pulse width > 3 ns

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Reference Doubler Input Frequency	10		175	MHz	
R2 Input Frequency	10		500	MHz	
PD2 Frequency (f_{PD2})	0.00015		250	MHz	Recommended at high end of the range for best phase noise; typically 122.88 MHz × 2
PLL2 CHARGE PUMP					
Current Range (I_{CP2})		160 to 2560		µA	I_{CP2} setting from 0 to 15 with 160 µA step size, V_{TUNE} = 1.4 V
I_{CP2} Variation over PVT		±25		%	V_{TUNE} = 1.4 V
Source/Sink Current Mismatch		2		%	Source/sink mismatch at 1.4 V
Current Step Size		160		µA	
Compliance Range		0.3 to 2.45		V	I_{CP} variation less than 10%
PLL2 NOISE PROFILE					
Floor FOM		−232		dBc/Hz	Normalized to 1 Hz
Flicker FOM		−266		dBc/Hz	Normalized to 1 Hz
FOM Variation vs. PVT		±3		dB	
FOM Degradation		3		dB	At minimum VCXO slew rate
PLL2 Flicker Noise		Determined by formula[2]		dBc/Hz	At f_{OUT}, f_{OFFSET}
PLL2 Noise Floor		Determined by formula[3]		dBc/Hz	At f_{OUT}, f_{PD2}
PLL2 Total Phase Noise (Unfiltered)		Determined by formula[4]		dBc/Hz	
PLL2 BANDWIDTH AND ACQUISITION TIMES					
Supported Loop Bandwidths (PLL2_BW)		10 to 700		kHz	Set by external components
VCO Automatic Gain Control (AGC) Settling Time[1]		10	20	ms	Time from power-up of VCO before initiating calibration; this applies to the 100 nF/1 µF configuration of external decoupling capacitors on the VCO supply network
VCO Calibration Time[5]		2694		t_{PD2}	N2 from 8 to 31
		779		t_{PD2}	N2 from 32 to 256
		214		t_{PD2}	N2 from 256 to 4095
		139		t_{PD2}	N2 > 4095
Temperature Range Postcalibration[1]	−40		+85	°C	Maintains lock from any temperature to any temperature
PLL2 Linear Acquisition Time		5/PLL2_BW		sec	After VCXO has stopped slewing to steady state
PLL2 Lock Detect Timer Period[5]		512		t_{PD2}	Low phase error counts to declare lock

[1] Guaranteed by design and characterization.
[2] See the PLL2 Noise Calculations section for more information on how to calculate the flicker noise for PLL2.
[3] See the PLL2 Noise Calculations section for more information on how to calculate the noise floor for PLL2.
[4] See the PLL2 Noise Calculations section for more information on how to calculate the total phase noise (unfiltered) for PLL2.
[5] t_{PD2} is the period of Phase Detector 2.

VCO CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE CONTROLLED OSCILLATOR (VCO)					
Frequency Tuning Range, On-Board VCOs[1]	2150		2880	MHz	Low VCO typical coverage
	2650		3550	MHz	High VCO typical coverage
	2400		3200	MHz	Guaranteed frequency coverage[2]
Tuning Sensitivity		38 to 44		MHz/V	Low frequency VCO at 2457.6 MHz
		35 to 40		MHz/V	High frequency VCO at 2949.12 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OPEN-LOOP VCO PHASE NOISE					
f_{OUT} = 2457.6 MHz					
f_{OFFSET} = 100 kHz		−109		dBc/Hz	High performance mode, does not include floor contribution due to output network
f_{OFFSET} = 800 kHz		−134		dBc/Hz	
f_{OFFSET} = 1 MHz		−136		dBc/Hz	
f_{OFFSET} = 10 MHz		−156		dBc/Hz	
Normalized Phase Noise Variation vs. Frequency		±2		dB	Sweep across both VCOs, all bands; normalize to 2457.6 MHz
Phase Noise Variation vs. Temperature		±2		dB	
Phase Noise Degradation in Low Performance Mode		2		dB	

[1] Guaranteed by design and characterization.
[2] Although the device covers this range without any gaps, for frequencies between ~2700 Hz and 2900 Hz, using a different VCO core to synthesize the frequency can be required as process parameters shift. Features are built into the HMC7044 to determine which core is selected for a given frequency that can fall in this range, but it can require software to configure these circuits appropriately.

CLOCK OUTPUT DISTRIBUTION CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK OUTPUT SKEW					
CLKOUTx/$\overline{\text{CLKOUTx}}$ to SCLKOUTx/$\overline{\text{SCLKOUTx}}$ Skew within One Clock Output Pair		15		|ps|	Same pair, same type termination and configuration
Any CLKOUTx/$\overline{\text{CLKOUTx}}$ to Any SCLKOUTx/$\overline{\text{SCLKOUTx}}$		30		|ps|	Any pair, same type termination and configuration
CLOCK OUTPUT DIVIDER					
12-Bit Divider Range	1		4094		1, 3, 5, and all even numbers up to 4094
SYSREF CLOCK OUTPUT DIVIDER					
12-Bit Divider Range	1		4094		1, 3, 5 and all even numbers up to 4094; pulse generator behavior is only supported for divide ratios ≥ 32
CLOCK OUTPUT ANALOG FINE DELAY					
Analog Fine Delay					
Adjustment Range[1]	135		670	ps	24 delay steps, f_{CLKOUT} = 983.04 MHz
Resolution		25		ps	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Maximum Analog Fine Delay Frequency[1]		3200		MHz	
CLOCK OUTPUT COARSE DELAY (FLIP FLOP BASED)					
Coarse Delay Adjustment Range	0		17	½ VCO period	17 delay steps in ½ VCO period
Coarse Delay Resolution		169.54		ps	f_{VCO} = 2949.12 MHz
Maximum Frequency Coarse Delay[1]		3200		MHz	
CLOCK OUTPUT COARSE DELAY (SLIP BASED)					
Coarse Delay					
Adjustment Range		1 to ∞		VCO period	
Resolution		339.08		ps	f_{VCO} = 2949.12 MHz
Maximum Frequency Coarse Delay		1600		MHz	

[1] Guaranteed by design and characterization.

SPUR CHARACTERISTICS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SPUR PERFORMANCE					
At 122.88 MHz and Its Harmonics		−70		dBc	

NOISE AND JITTER CHARACTERISTICS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOSED-LOOP PHASE NOISE—WIDE LOOP FILTER					For best integrated noise
SSB Phase Noise					
At 2457.6 MHz[1]					
		−98.0		dBc/Hz	Offset = 100 Hz
		−111.1		dBc/Hz	Offset = 1 kHz
		−119.8		dBc/Hz	Offset = 10 kHz
		−125.2		dBc/Hz	Offset = 100 kHz
		−126.9		dBc/Hz	Offset = 300 kHz
		−131.3		dBc/Hz	Offset = 1 MHz
		−150.0		dBc/Hz	Offset = 5 MHz
		−154.0		dBc/Hz	Offset = 10 MHz
		−156.3		dBc/Hz	Offset = 100 MHz
		44.0		fs	Integrated jitter = 12 kHz to 20 MHz
At 614.4 MHz[1]					
		−110.4		dBc/Hz	Offset = 100 Hz
		−122.8		dBc/Hz	Offset = 1 kHz
		−131.3		dBc/Hz	Offset = 10 kHz
		−136.6		dBc/Hz	Offset = 100 kHz
		−138.3		dBc/Hz	Offset = 300 kHz
		−142.7		dBc/Hz	Offset = 1 MHz
		−157.6		dBc/Hz	Offset = 5 MHz
		−158.8		dBc/Hz	Offset = 10 MHz
		−159.2		dBc/Hz	Offset = 100 MHz
		50.0		fs	Integrated jitter = 12 kHz to 20 MHz
CLOSED-LOOP PHASE NOISE—NARROW LOOP FILTER					For best 800 kHz offset
SSB Phase Noise					
At 2949.12 MHz[2]					
		−100.9		dBc/Hz	Offset = 100 Hz
		−103.8		dBc/Hz	Offset = 1 kHz
		−106.9		dBc/Hz	Offset = 10 kHz
		−109.9		dBc/Hz	Offset = 100 kHz
		−132.3		dBc/Hz	Offset = 800 kHz
		−134.5		dBc/Hz	Offset = 1 MHz
		−152		dBc/Hz	Offset = 10 MHz
		−155.3		dBc/Hz	Offset = 100 MHz
		108		fs	Integrated jitter = 12 kHz to 20 MHz
At 983.04 MHz[2]					
		−110.4		dBc/Hz	Offset = 100 Hz
		−113.3		dBc/Hz	Offset = 1 kHz
		−116.4		dBc/Hz	Offset = 10 kHz
		−119.4		dBc/Hz	Offset = 100 kHz
		−141.7		dBc/Hz	Offset = 800 kHz
		−143.7		dBc/Hz	Offset = 1 MHz
		−157.1		dBc/Hz	Offset = 10 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
		−157.1		dBc/Hz	Offset = 100 MHz
		102		fs	Integrated jitter 12 kHz to 20 MHz
OUTPUT NETWORK FLOOR FOM					
CML with 100 Ω Internal Termination (CML100)					
Fundamental Mode		−250		dBc/Hz	High performance
Divide by 1 to Divide by N		−248		dBc/Hz	High performance
Divide by 1 to Divide by N		−247		dBc/Hz	Low power (4 dB less power)
LVPECL					
Fundamental Mode		−250		dBc/Hz	
Divide by 1 to Divide by N		−247		dBc/Hz	
LVDS					
Divide by 1 to Divide by N		−244		dBc/Hz	High performance
Divide by 1 to Divide by N		−243		dBc/Hz	Low power (4 dB less power)
PHASE NOISE DEGREDATION DUE TO HARMONICS[3]					
Fundamental Only		0.00		dB	
Third Harmonic		0.25		dB	
Third and Fifth Harmonics		0.40		dB	
Third, Fifth, and Seventh Harmonics		0.50		dB	
Third, Fifth, Seventh, and Ninth Harmonics		0.53		dB	
Third Through 61st Harmonics		0.64		dB	
PHASE NOISE FLOOR AND JITTER					
Phase Noise Floor at f_{OUT}		Determined by formula[4]		dBc/Hz	
Jitter Density of Floor at f_{OUT}		Determined by formula[5]		sec/√Hz	
RMS Additive Jitter Due to Floor		Determined by formula[6]		sec	From f_{OUT} and output channel FOM

[1] PLL2 locked at 122.88 MHz × 2 × 10, wide (600 kHz) loop filter for best 12 kHz to 20 MHz jitter, CML100 high performance output buffer.
[2] PLL2 locked at 122.88 MHz × 2 × 12, narrow loop for best 800 Hz offset, CML100 high performance output buffer.
[3] When the harmonics of the signal are captured in the measurement bandwidth of the receiving instrument/circuit, the noise power of those harmonics can fold and influence the overall noise. Their presence causes a decibel for decibel influence. For example, if the third harmonic is at −10 dBc, there is an additional noise contributor of 10 dB lower than the fundamental at all offsets that folds in-band and causes a 0.2 dB hit overall. The influence of the harmonics factoring into the degradation is primarily a function of the frequency of the buffer bandwidth relative to the third, fifth, and seventh harmonics. As the output frequency reduces, more harmonics fall into the observation bandwidth, and the degradation worsens, but only slightly. This effect produces a penalty of 0.65 dB maximum if harmonics up to the 61st harmonic is included.
[4] See the Phase Noise Floor and Jitter section for more information on how to calculate the phase noise floor.
[5] See the Phase Noise Floor and Jitter section for more information on how to calculate the jitter density of floor.
[6] See the Phase Noise Floor and Jitter section for more information on how to calculate the rms additive jitter due to floor.

CLOCK OUTPUT DRIVER CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML MODE (LOW POWER)					R_L = 100 Ω, 9.6 mA
−3 dB Bandwidth		1950		MHz	Differential output voltage = 980 mV p-p diff
Output Rise Time		175		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		145		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		185		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		145		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		1390		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		1360		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Common-Mode Output Voltage		V_{CC} − 1.05		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
CML MODE (HIGH POWER)					R_L = 100 Ω, 14.5 mA
3 dB Bandwidth		1400		MHz	Differential output voltage = 1410 mV p-p diff
Output Rise Time		250		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		165		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		255		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		170		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		2000		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		1800		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Common-Mode Output Voltage		V_{CC} − 1.6		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
LVPECL MODE					R_L = 150 Ω, 4.8 mA
3 dB Bandwidth		2400		MHz	Differential output voltage = 1240 mV p-p diff
Output Rise Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		130		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		130		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		1760		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		1850		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Common-Mode Output Voltage		V_{CC} − 1.3		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
LVDS MODE (LOW POWER)					1.75 mA
Maximum Operating Frequency		600		MHz	Differential output voltage = 400 mV p-p diff
Output Rise Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		100		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		95		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		390		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
Common-Mode Output Voltage		1.1		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
LVDS MODE (HIGH POWER)					3.5 mA
Maximum Operating Frequency		1700		MHz	Differential output voltage = 650 mV p-p diff
Output Rise Time		145		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		105		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		145		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		100		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		750		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		730		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Common-Mode Output Voltage		1.1		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
CMOS MODE					
Maximum Operating Frequency		600		MHz	Single-ended output voltage = 940 mV p-p diff
Output Rise Time		425		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
Output Fall Time		420		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Output Voltage					
High		V_{CC} − 0.07		V	Load current = 1 mA
		V_{CC} − 0.5		V	Load current = 10 mA
Output		0.07		V	Load current = 1 mA
		0.5		V	Load current = 10 mA

[1] Guaranteed by design and characterization.

ABSOLUTE MAXIMUM RATINGS

Table 11.

Parameter	Rating
VCC1_VCO, VCC2_OUT, VCC3_SYSREF, VCC4_OUT, VCC5_PLL1, VCC6_OSCOUT, VCC7_PLL2, VCC8_OUT, VCC9_OUT	−0.3 V to +3.6 V
Maximum Junction Temperature (T_J)	125°C
Maximum Peak Reflow Temperature	260°C
Thermal Resistance (Channel to Ground Paddle)	7°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity Level	
Human Body Model	Class 1C
Charged Device Model[1]	Class 3

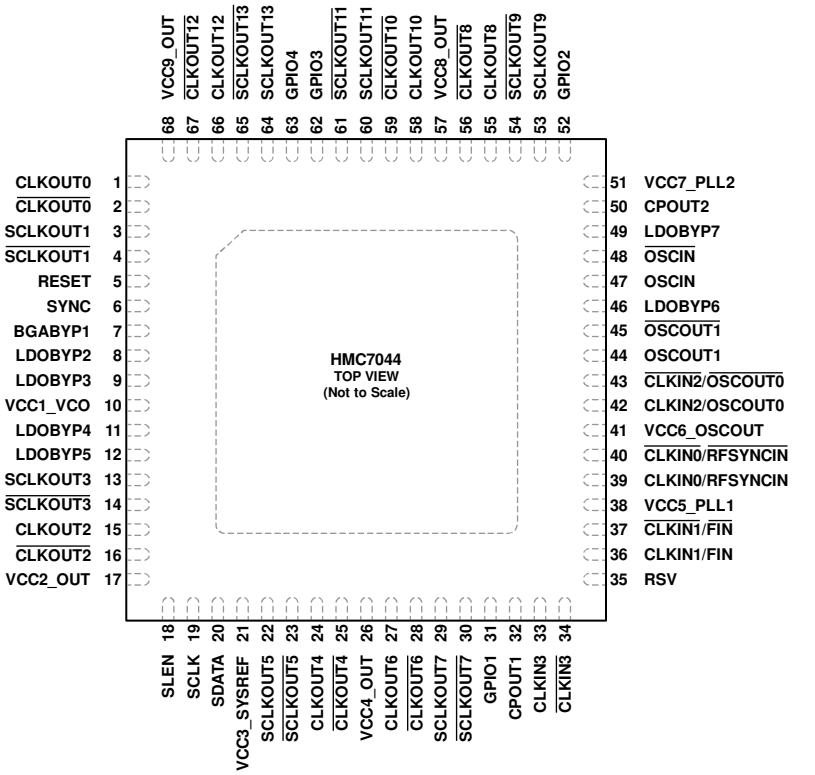
[1] Per JESD22-C101-F (CDM) standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. CONNECT THE EXPOSED PAD TO A HIGH QUALITY RF/DC GROUND.

Figure 2. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	CLKOUT0	O	True Clock Output Channel 0. Default DCLK profile.
2	$\overline{\text{CLKOUT0}}$	O	Complementary Clock Output Channel 0. Default DCLK profile.
3	SCLKOUT1	O	True Clock Output Channel 1. Default SYSREF profile.
4	$\overline{\text{SCLKOUT1}}$	O	Complementary Clock Output Channel 1. Default SYSREF profile.
5	RESET	I	Device Reset Input. Active high. For normal operation, set RESET to 0.
6	SYNC	I	Synchronization Input. This pin is used for multichip synchronization. If not used, set SYNC to 0.
7	BGABYP1		Band Gap Bypass Capacitor Connection. Connect a 4.7 µF capacitor to ground. This pin affects all internally regulated supplies.
8	LDOBYP2		LDO Bypass 2. Connect a 4.7 µF capacitor to ground. The internal digital supply is 1.8 V. This pin is the LDO bypass for the PLL1, PLL2, and SYSREF sections.
9	LDOBYP3		LDO Bypass 3. Connect a 4.7 µF capacitor to ground. This pin is the 2.8 V supply to PLL1, Phase Frequency Detector 1 (PFD1), Charge Pump 1 (CP1), RF synchronization (RFSYNC), and Pin 36 buffers.
10	VCC1_VCO	P	3.3 V Supply for VCO and VCO Distribution.
11	LDOBYP4		LDO Bypass 4. Connect a 1 µF capacitor to ground. This pin is the first stage regulator for the VCO supply.
12	LDOBYP5		LDO Bypass 5. Connect a 100 nF capacitor to LDOBYP4. This pin is the VCO core supply voltage.
13	SCLKOUT3	O	True Clock Output Channel 3. Default SYSREF profile.
14	$\overline{\text{SCLKOUT3}}$	O	Complementary Clock Output Channel 3. Default SYSREF profile.
15	CLKOUT2	O	True Clock Output Channel 2. Default DCLK profile.
16	$\overline{\text{CLKOUT2}}$	O	Complementary Clock Output Channel 2. Default DCLK profile.
17	VCC2_OUT	P	Power Supply for Clock Group 1 (Southwest)—Channel 2 and Channel 3. See the Clock Grouping, Skew, and Crosstalk section.
18	SLEN	I	SPI Latch Enable.

Pin No.	Mnemonic	Type[1]	Description
19	SCLK	I	SPI Clock.
20	SDATA	I/O	SPI Data.
21	VCC3_SYSREF	P	Power Supply for Common SYSREF Divider.
22	SCLKOUT5	O	True Clock Output Channel 5. Default SYSREF profile.
23	$\overline{\text{SCLKOUT5}}$	O	Complementary Clock Output Channel 5. Default SYSREF profile.
24	CLKOUT4	O	True Clock Output Channel 4. Default DCLK profile.
25	$\overline{\text{CLKOUT4}}$	O	Complementary Clock Output Channel 4. Default DCLK profile.
26	VCC4_OUT	P	Power Supply for Clock Group 2 (South)—Channel 4, Channel 5, Channel 6, and Channel 7. See the Clock Grouping, Skew, and Crosstalk section.
27	CLKOUT6	O	True Clock Output Channel 6. Default DCLK profile.
28	$\overline{\text{CLKOUT6}}$	O	Complementary Clock Output Channel 6. Default DCLK profile.
29	SCLKOUT7	O	True Clock Output Channel 7. Default SYSREF profile.
30	$\overline{\text{SCLKOUT7}}$	O	Complementary Clock Output Channel 7. Default SYSREF profile.
31	GPIO1	I/O	Programmable General-Purpose Input/Output 1.
32	CPOUT1	O	PLL1 Charge Pump Output.
33	CLKIN3	I	True Reference Clock Input 3 of PLL1.
34	$\overline{\text{CLKIN3}}$	I	Complementary Reference Clock Input 3 of PLL1.
35	RSV	R	Reserved Pin. This pin must be tied to ground.
36	CLKIN1/FIN	I	True Reference Clock Input 1 of PLL1/External VCO Input for External VCO Mode.
37	$\overline{\text{CLKIN1}}$/$\overline{\text{FIN}}$	I	Complementary Reference Clock Input 1 of PLL1/Complementary External VCO Input for External VCO Mode.
38	VCC5_PLL1	P	Power Supply for LDO, Used for PLL1.
39	CLKIN0/RFSYNCIN	I	True Reference Clock Input 0 of PLL1/RF Synchronization Input with Deterministic Delay.
40	$\overline{\text{CLKIN0}}$/$\overline{\text{RFSYNCIN}}$	I	Complementary Reference Clock Input 0 of PLL1/Complementary RF Synchronization Input with Deterministic Delay.
41	VCC6_OSCOUT	P	Power Supply for Oscillator Output Path.
42	CLKIN2/OSCOUT0	I/O	True Reference Clock Input 2 (Bidirectional Pin) of PLL1/Buffered Output 0 of Oscillator Input.
43	$\overline{\text{CLKIN2}}$/$\overline{\text{OSCOUT0}}$	I/O	Complementary Reference Clock Input 2 (Bidirectional Pin) of PLL1/Complementary Buffered Output 0 of Oscillator Input.
44	OSCOUT1	O	True Buffered Output 1 of Oscillator Input.
45	$\overline{\text{OSCOUT1}}$	O	Complementary Buffered Output 1 of Oscillator Input.
46	LDOBYP6		LDO Bypass, Connect a 4.7 µF capacitor to ground. This pin is the LDO bypass for R2, N2, Phase Frequency Detector 2 (PFD2), Charge Pump 2 (CP2), and the PLL2 loop filter.
47	OSCIN	I	True Feedback Input to PLL1. This pin is a reference input to PLL2.
48	$\overline{\text{OSCIN}}$	I	Complementary Feedback Input to PLL1. This pin is a reference input to PLL2.
49	LDOBYP7		LDO Bypass. Connect a 4.7 µF capacitor to ground. This pin is the LDO bypass for the VCXO buffer and frequency doubler oscillator output divider.
50	CPOUT2	I/O	PLL2 Charge Pump Output.
51	VCC7_PLL2	P	Power Supply for LDO for PLL2.
52	GPIO2	I/O	Programmable General-Purpose Input/Output 2.
53	SCLKOUT9	O	True Clock Output Channel 9. Default SYSREF profile.
54	$\overline{\text{SCLKOUT9}}$	O	Complementary Clock Output Channel 9. Default SYSREF profile.
55	CLKOUT8	O	True Clock Output Channel 8. Default DCLK profile.
56	$\overline{\text{CLKOUT8}}$	O	Complementary Clock Output Channel 8. Default DCLK profile.
57	VCC8_OUT	P	Power Supply for Clock Group 3 (North)—Channel 8, Channel 9, Channel 10, and Channel 11. See the Clock Grouping, Skew, and Crosstalk section.
58	CLKOUT10	O	True Clock Output Channel 10. Default DCLK profile.
59	$\overline{\text{CLKOUT10}}$	O	Complementary Clock Output Channel 10. Default DCLK profile.
60	SCLKOUT11	O	True Clock Output Channel 11. Default SYSREF profile.
61	$\overline{\text{SCLKOUT11}}$	O	Complementary Clock Output Channel 11. Default SYSREF profile.
62	GPIO3	I/O	Programmable General-Purpose Input/Output 3. Sleep input by default.
63	GPIO4	I/O	Programmable General-Purpose Input/Output 4. Pulse generator request by default.
64	SCLKOUT13	O	True Clock Output Channel 13. Default SYSREF profile.

Pin No.	Mnemonic	Type[1]	Description
65	$\overline{\text{SCLKOUT13}}$	O	Complementary Clock Output Channel 13. Default SYSREF profile.
66	CLKOUT12	O	True Clock Output Channel 12. Default DCLK profile.
67	$\overline{\text{CLKOUT12}}$	O	Complementary Clock Output Channel 12. Default DCLK profile.
68	VCC9_OUT	P	Power Supply for Clock Group 0 (Northwest)—Channel 0, Channel 1, Channel 12, and Channel 13. See the Clock Grouping, Skew, and Crosstalk section.
	EP		Exposed Pad. Connect the exposed pad to a high quality RF/dc ground.

[1] O is output, I is input, P is power, and I/O is input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, PFD PLL1 = 7.68 MHz, PFD PLL2 = 122.88 MHz × 2; I_{CP1} = 1.92 mA, I_{CP2} = 2.56 mA (wide loop), I_{CP2} = 1.12 mA (narrow loop), PLL1 loop BW ~ 70 Hz, PLL2 wide loop BW ≈ 650 kHz, PLL2 narrow loop BW ≈ 215 kHz, PLL2 narrow loop filter = 1.1 nF | 160 Ω × 33 nF; PLL2 wide loop filter = 150 pF | 430 Ω × 4.7 nF; PLL1 loop filter = 4.7 nF | 10 µF × 1.2 kΩ.

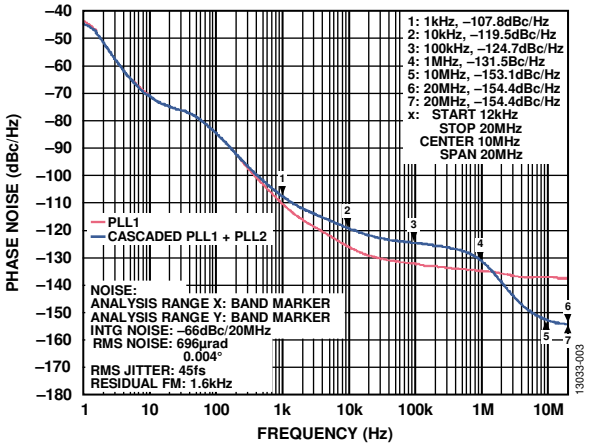


Figure 3. Cascaded Phase Noise at 2457.6 MHz, PLL2 Wide Loop Bandwidth

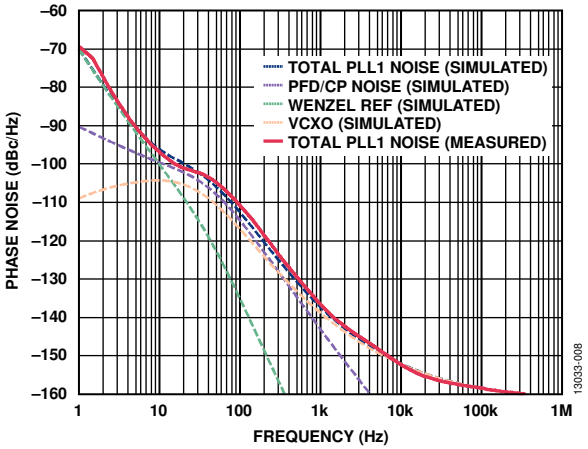


Figure 6. Closed-Loop Phase Noise at 122.88 MHz, PLL1 Measurement vs. Simulated, Clean Reference Source, ~70 Hz Loop Bandwidth 80° Phase Margin

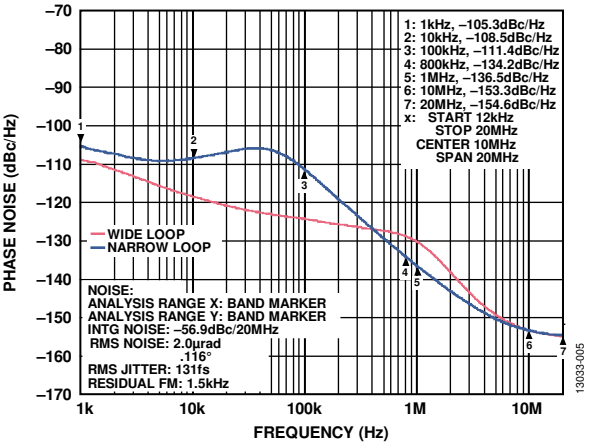


Figure 4. Phase Noise at 2457.6 MHz, Narrow vs. PLL2 Wide Loop Bandwidth

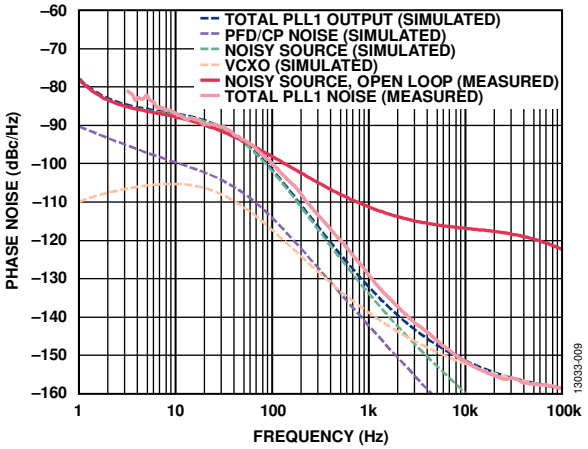


Figure 7. Closed-Loop Phase Noise at 122.88 MHz, PLL1 Measurement vs. Simulated, Noisy Reference Source, ~70 Hz Loop Bandwidth, 80° Phase Margin

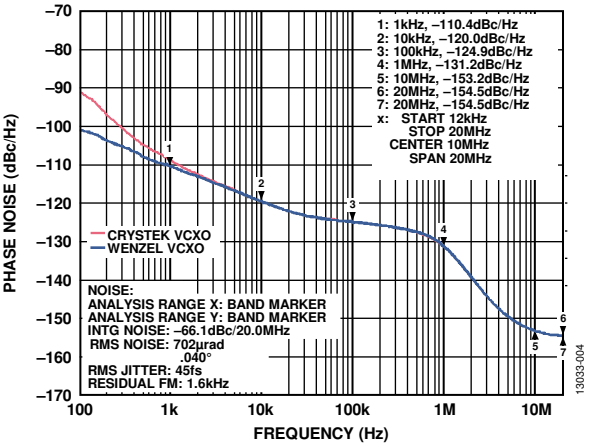


Figure 5. PLL2 Phase Noise vs. Frequency, VCXO Quality at 2457.6 MHz, Wide Loop Bandwidth

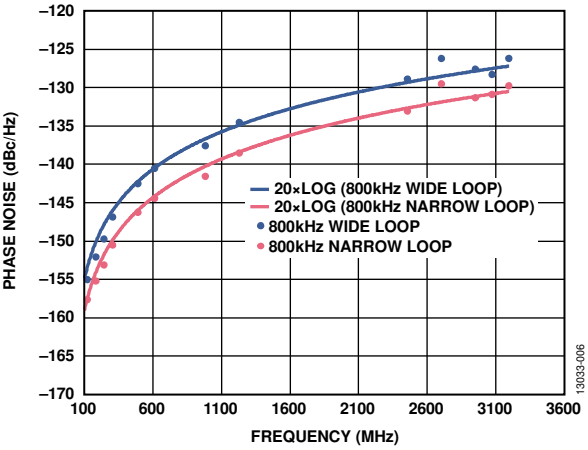


Figure 8. Phase Noise vs. Frequency at Common Output Frequencies

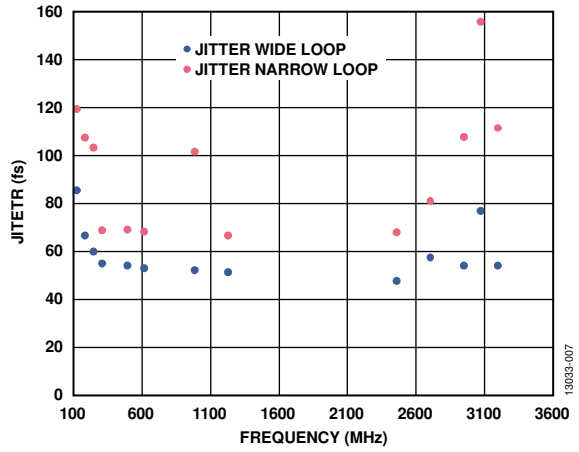


Figure 9. 12 kHz to 20 MHz Jitter vs. Frequency, Wide Loop and Narrow Loop at Common Output Frequencies

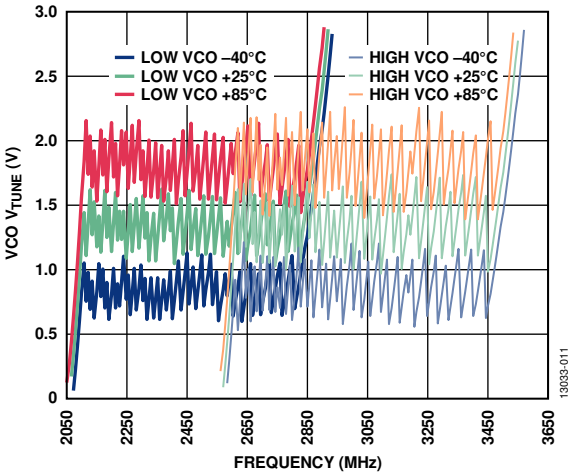


Figure 12. VCO V_{TUNE} vs. Frequency

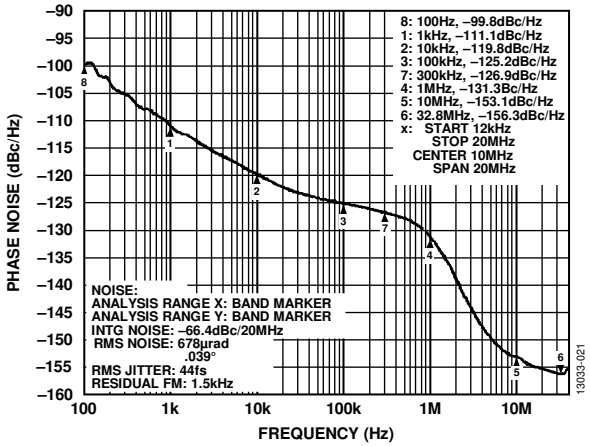


Figure 10. Phase Noise, CLKOUTx/$\overline{\text{CLKOUTx}}$ = 2457.6 MHz, Optimized for Best Integrated Jitter (12 kHz to 20 MHz)

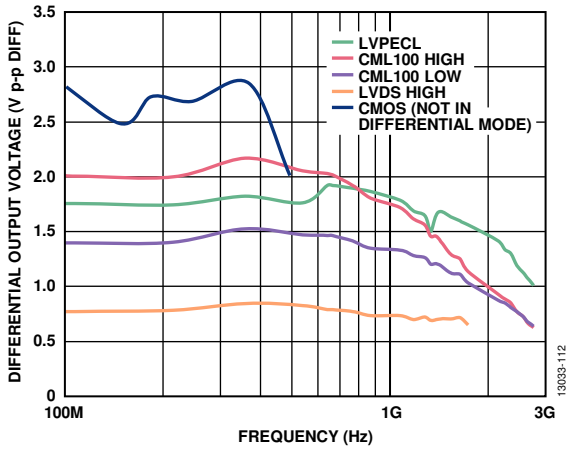


Figure 13. Differential Output Voltage vs. Frequency at Different Modes

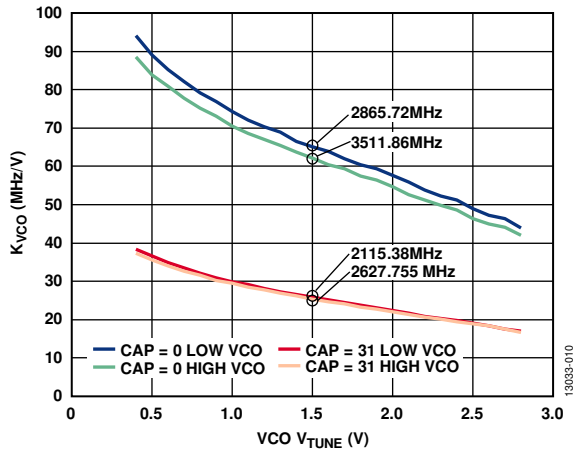


Figure 11. VCO Gain (K_{VCO}) vs. VCO V_{TUNE}

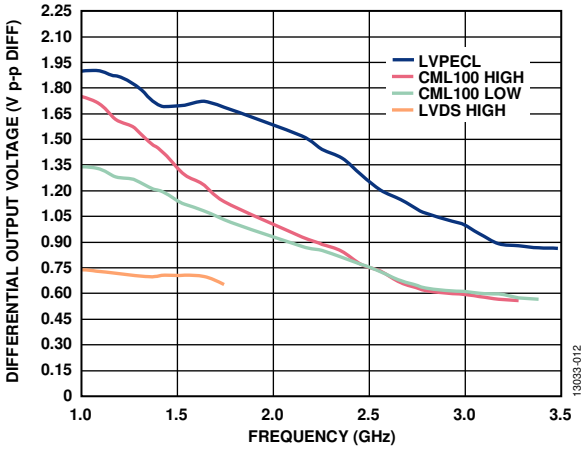


Figure 14. Differential Output Voltage vs. Frequency at Different Modes

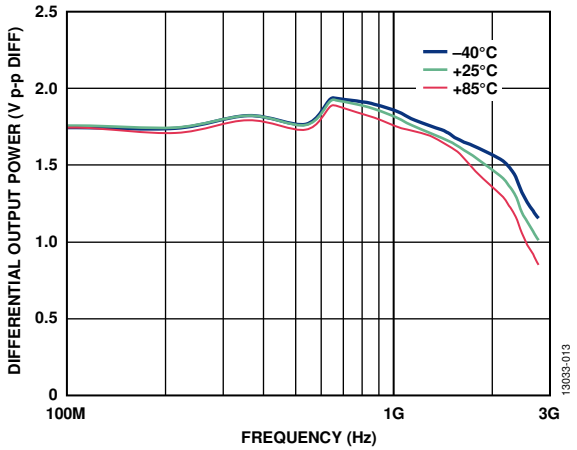


Figure 15. LVPECL Differential Output Voltage vs. Frequency at Different Temperatures

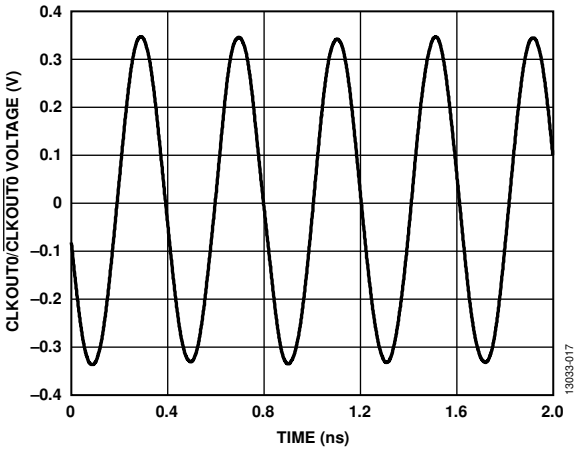


Figure 16. Differential CLKOUT0/$\overline{\text{CLKOUT0}}$ at 2457 MHz, LVPECL

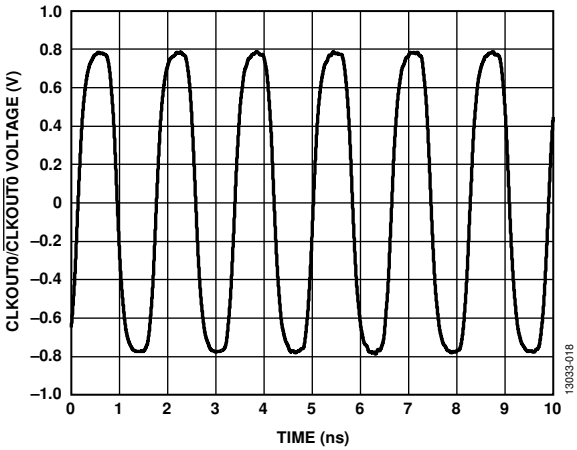


Figure 17. Differential CLKOUT0/$\overline{\text{CLKOUT0}}$ Voltage at 614.4 MHz, LVPECL

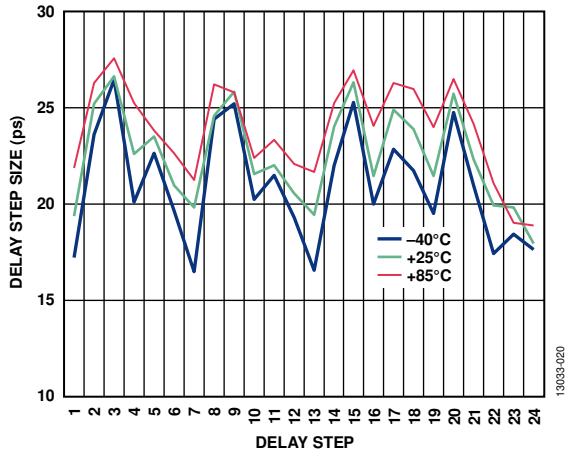


Figure 18. Analog Delay Step Size vs. Delay Step over Temperature, LVPECL at 1474.56 MHz

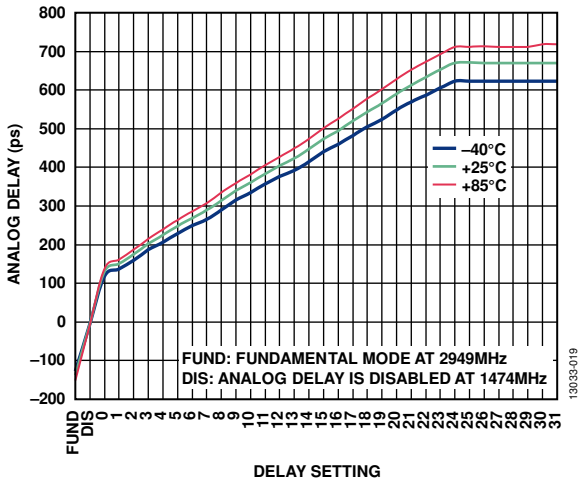


Figure 19. Analog Delay vs. Delay Setting over Temperature, LVPECL at 1474.56 MHz

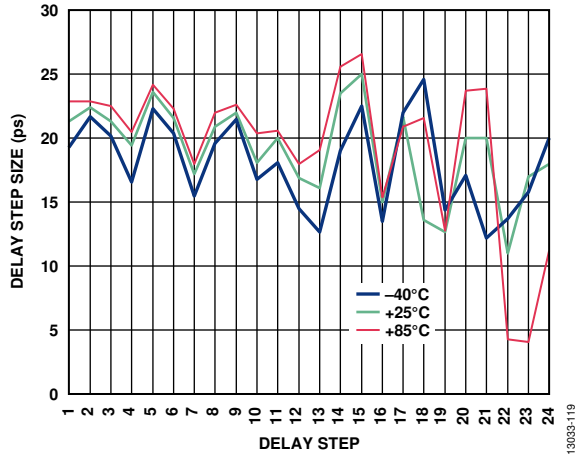


Figure 20. Analog Delay Step Size vs Delay Step over Temperature, LVPECL at 3072 MHz with Digital Delay = 0

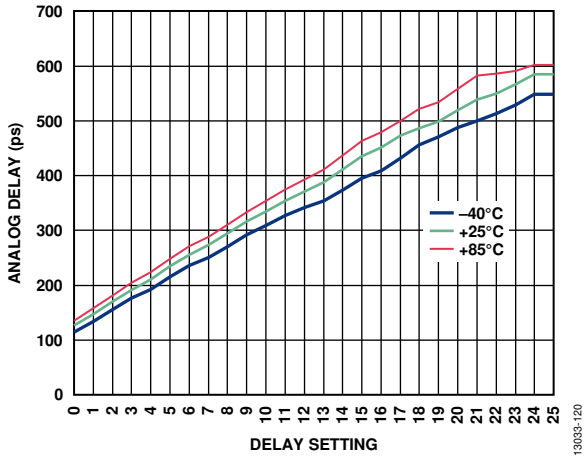


Figure 21. Analog Delay vs. Delay Setting over Temperature, LVPECL at 3072 MHz with Digital Delay = 0

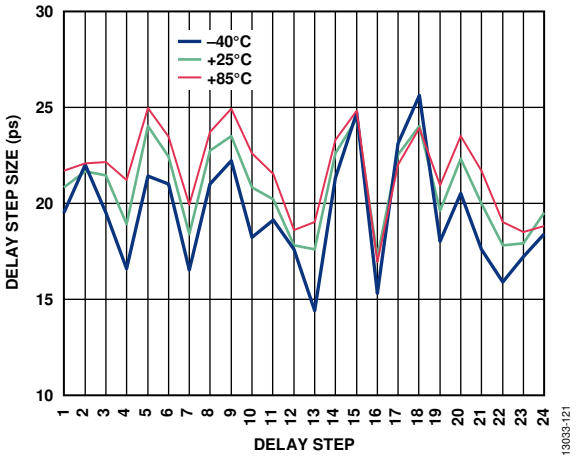


Figure 22. Analog Delay Step Size vs Delay Step over Temperature, LVPECL at 3072 MHz with Digital Delay = 1

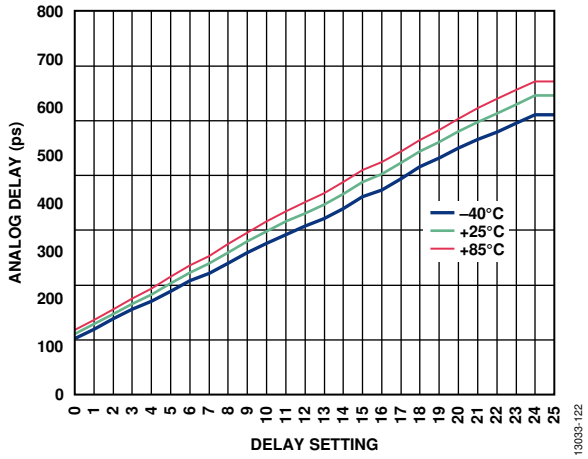


Figure 23. Analog Delay vs. Delay Setting over Temperature, LVPECL at 3072 MHz with Digital Delay = 1

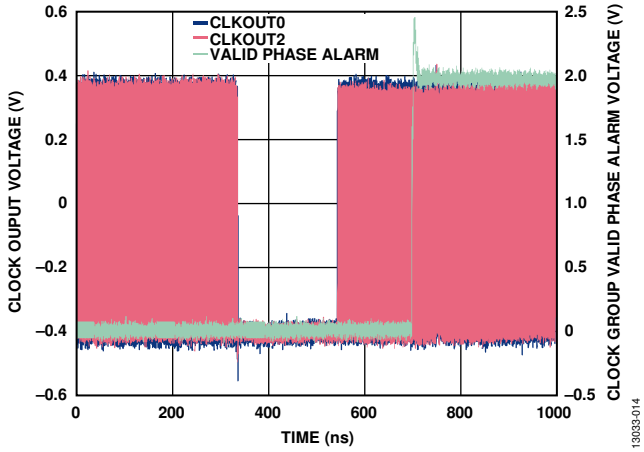


Figure 24. Output Channel Synchronization Before and After Rephase

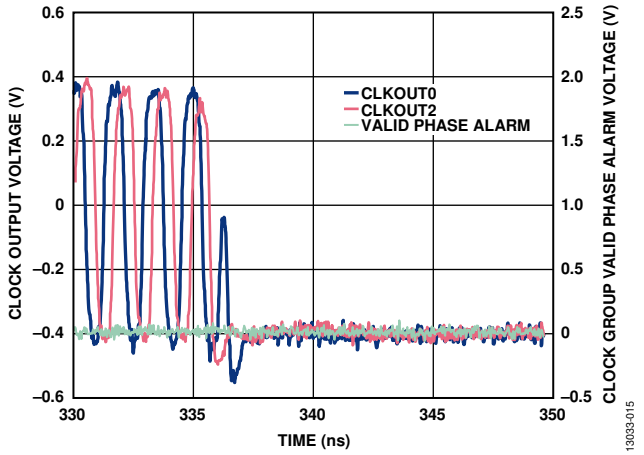


Figure 25. Output Channel Synchronization Before Rephase

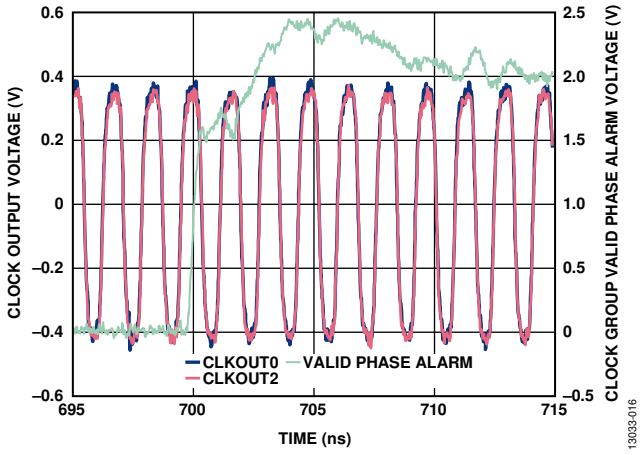


Figure 26. Output Channel Synchronization After Rephase

TYPICAL APPLICATION CIRCUITS

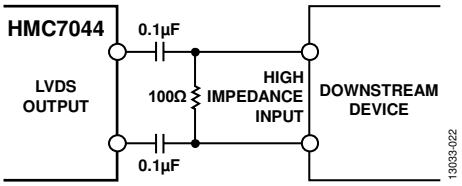


Figure 27. AC-Coupled LVDS Output Driver

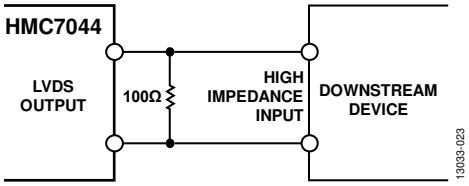


Figure 31. DC-Coupled LVDS Output Driver

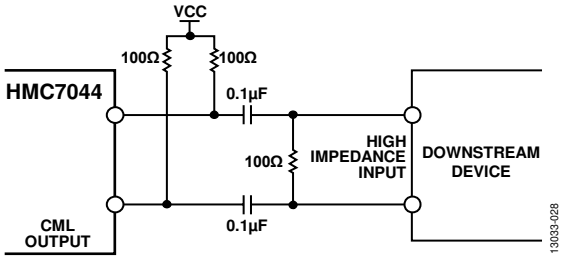


Figure 28. AC-Coupled CML (Configured High-Z) Output Driver

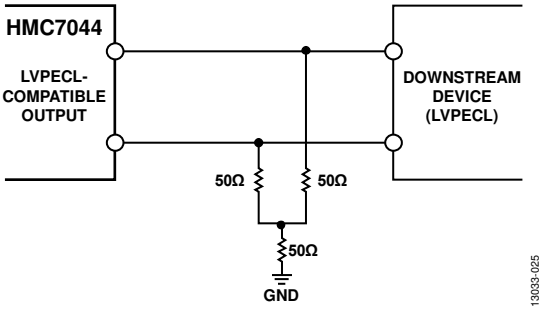


Figure 32. DC-Coupled LVPECL Output Driver

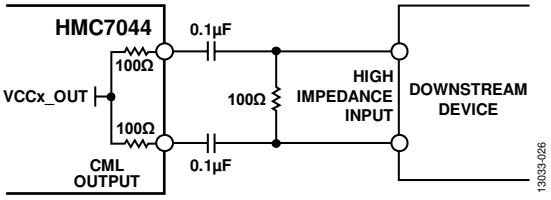


Figure 29. AC-Coupled CML (Internal) Output Driver

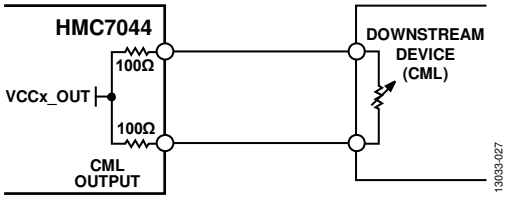


Figure 33. DC-Coupled CML (Internal) Output Driver

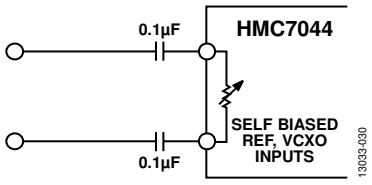


Figure 30. CLKIN0/$\overline{\text{CLKIN0}}$, CLKIN1/$\overline{\text{CLKIN1}}$, CLKIN2/$\overline{\text{CLKIN2}}$, CLKIN3/$\overline{\text{CLKIN3}}$, and OSCIN/$\overline{\text{OSCIN}}$ Input, Differential Mode

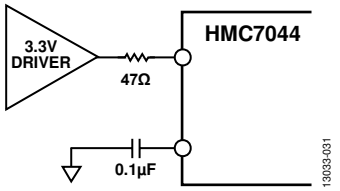


Figure 34. CLKIN0, CLKIN1, CLKIN2, CLKIN3, and OSCIN Input, Single-Ended Mode

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to the energy of the sine wave in the frequency domain spreading out, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Phase Noise

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted, which makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted, which makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

The HMC7044 is a high performance, dual-loop, integer N jitter attenuator capable of performing frequency translation, reference selection, and generation of ultralow phase noise references for high speed data converters with either parallel or serial (JESD204B type) interfaces. The device is designed to meet the requirements of demanding base station designs, and offers a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs.

The HMC7044 uses a dual-loop architecture, where two integer mode PLLs are connected in series to form a jitter attenuating clock multiplier unit. The high performance dual-loop topology of the HMC7044 enables the wireless/RF system designer to attenuate the incoming jitter of a primary system reference clock (for example, Common Public Radio Interface™ (CPRI) source) and generate low phase noise, high frequency clocks to drive data converter sample clock inputs. The HMC7044 provides 14 low noise and configurable outputs to offer flexibility in interfacing with many different components in an RF transceiver system, such as data converters, local oscillators, transmit/receive modules, FPGAs, and digital front-end (DFE) ASICs.

The first PLL in the HMC7044 is designed for low bandwidth configuration using appropriately selected external loop filter components, and internal charge pump bias settings to achieve less than a few hundred Hz bandwidth, typically. The exact bandwidth roll-off points depend on the frequency spectrum of noise that must be attenuated in the system. The first PLL locks an external VCXO and provides the clock holdover functions and the reference frequency to the high performance second PLL loop. The combination of the loops provides an excellent clock generation unit with the capability to attenuate incoming reference clock jitter. The second PLL loop features two overlapping on-chip VCOs that are SPI selectable with center frequencies at 2.5 GHz and 3 GHz, respectively. Both VCOs are designed to have wide tuning ranges for broad output frequency coverage. The desired output frequency is set by the chosen VCXO frequency, VCO core (higher or lower frequency core), and the programmed second PLL feedback divider and output channel divider values.

The HMC7044 generates up to seven DCLK and SYSREF clock pairs per the JESD204B interface requirements. The system designer can generate a lower number of DCLK and SYSREF pairs, and configure the remaining output signal paths as desired, either as DCLKs or additional SYSREFs or other reference clocks with independent phase and frequency adjustment. Frequency adjustment can be accomplished by selecting the appropriate output divider values. One of the unique features of the HMC7044 is the independent flexible phase management of each of the 14 channels. Using a combination of divider slip-based, digital/coarse and analog/fine delay adjustments, each channel can be programmed to have a different phase offset. The phase adjustment capability allows the designer to offset board flight time delay variations, data converter sample window matching, and meet JESD204B synchronization challenges. The output signal path design of the HMC7044 is implemented to ensure both linear phase adjustment steps and minimal noise perturbation when phase adjustment circuits are turned on.

One of the key challenges in JESD204B system design is ensuring the synchronization of data converter frame alignment across the system, from the FPGA or DFE to ADCs and DACs through a large clock tree that can comprise multiple clock generation and distribution ICs. The HMC7044 is specifically designed to offer features to address this challenge. Using the SYSREF valid interrupt feature, the wait time latency can be reduced in the FPGAs. The HMC7044 raises this flag through its GPO port when all counters are set and outputs are at the desired phases. Additionally, an external reference-based synchronization feature (SYNC via PLL2 or RF SYNC only in fanout mode) synchronizes multiple devices, that is, it ensures that all clock outputs start with same rising edge. This operation is achieved by rephasing the SYSREF control unit deterministically, and then restarting the output dividers with this new desired phase.

Offering excellent crosstalk, frequency isolation, and spurious performance, the device generates independent frequencies in both single-ended and differential formats. The four input reference options allows up to three backup frequency sources, with hitless switching and holdover capabilities, supporting system redundancy and uninterrupted operation on reference data and clock failures. The device also features dedicated oscillator fanout mode for best clock isolation, which generates multiple copies of the VCXO clock to be distributed across the board with excellent frequency isolation.

Both the DCLK and SYSREF clock outputs can be configured to support different signaling standards, including CML, LVDS, LVPECL, and LVCMOS, and different bias conditions to offset varying board insertion losses. The outputs can also be programmed for ac or dc coupling and 50 Ω or 100 Ω internal and external termination options.

The HMC7044 is programmed via a 3-wire serial port interface (SPI) and powers up with a default configuration that generates valid output frequencies within the VCO tuning ranges regardless of whether a reference clock exists.

The HMC7044 is offered in a 68-lead, 10 mm ×10 mm, LFCSP package with the exposed pad to ground.

Note that, throughout this data sheet, multifunction pins, such as CLKIN0/RFSYNCIN, are referred to either by the entire pin name or by a single function of the pin, for example, CLKIN0, when only that function is relevant.

DETAILED BLOCK DIAGRAM

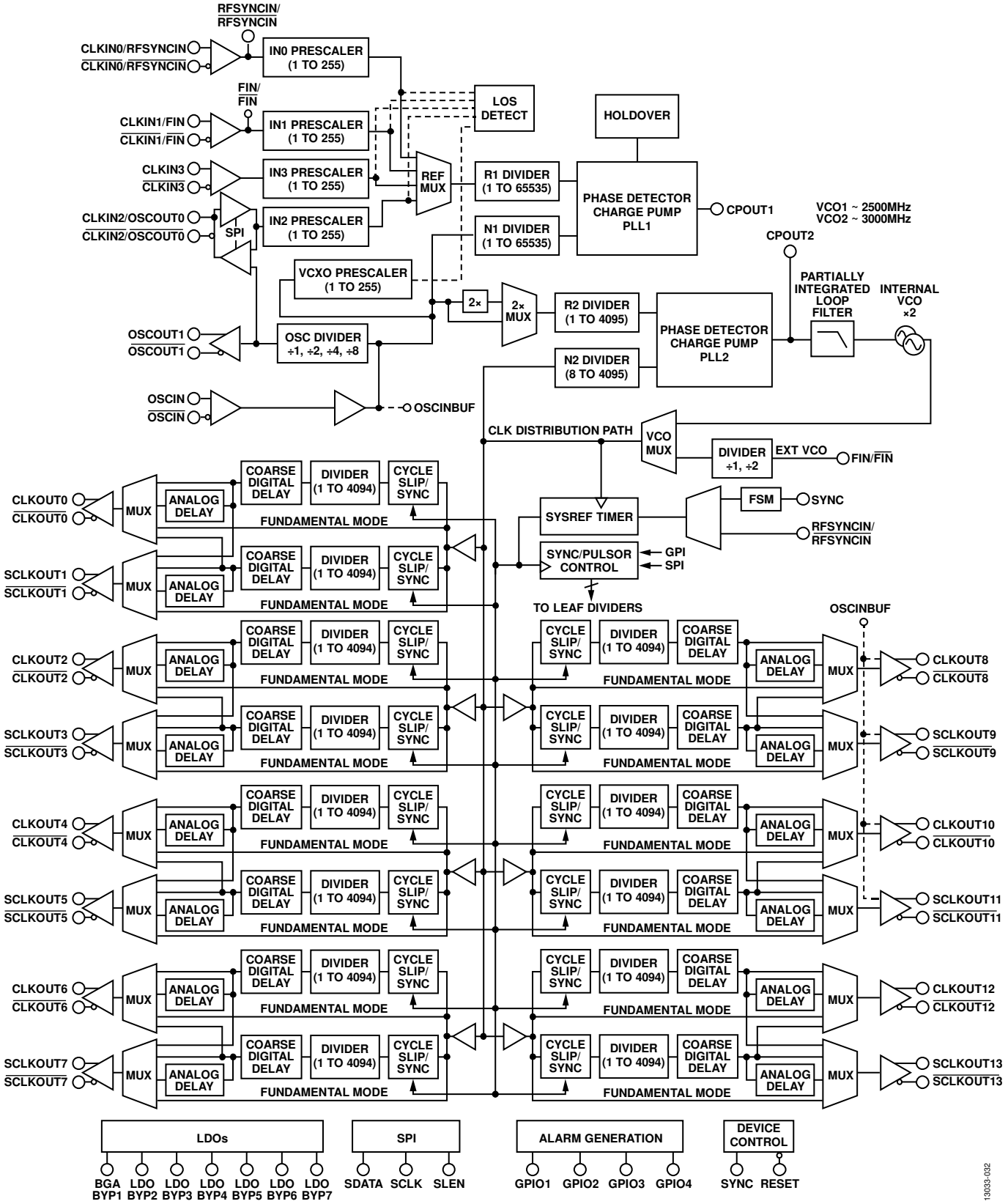


Figure 35. Top Level Diagram