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HMC704LP4E

v04.0215

8 GHz FRACTIONAL-N PLL

Typical Applications

The HMC704LP4E is ideal for:

- Microwave Point-to-Point Radios
- Base Stations for Mobile Radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs, WiMAX
- Communications Test Equipment
- CATV Equipment
- Automotive

Features

Wide band: DC - 8 GHz RF Input, 4 GHz 19-bit Prescaler

Industry Leading Phase Noise & Spurious: -112 dBc/Hz @ 8 GHz Fractional, 50 kHz Offset

Figure of Merit

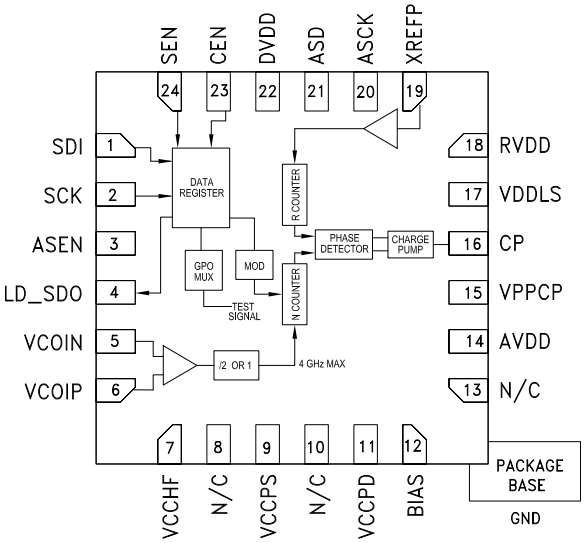
-230 dBc/Hz Fractional Mode

-233 dBc/Hz Integer Mode 100 MHz PFD

High PFD rate: 100 MHz

24 Lead 4x4 mm SMT Package: 16 mm^2

Functional Diagram



General Description

The HMC704LP4E has been designed for the best phase noise and lowest spurious content possible in an integrated PLL.

Fabricated in a SiGe BiCMOS process, this Fractional-N PLL consists of a very low noise digital phase detector, VCO divider, reference divider and a precision controlled charge pump.

Ultra low in-close phase noise and low spurious allows wide loop bandwidths for faster frequency hopping and low micro-phonics.

Exact frequency mode with 24-bit fractional modulator provides the ability to generate fractional frequencies with zero frequency error, an important feature for Digital Pre-Distortion systems.

The serial interface offers read back capability and is compatible with a wide variety of protocols.

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HMC704* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC704LP4E Evaluation Board

DOCUMENTATION

Data Sheet

- HMC704LP4E: 8 GHZ Fractional-N PLL Data Sheet

TOOLS AND SIMULATIONS

- ADIsimFrequency Planner Tool
- ADIsimPLL™

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: LP4, LP4B, LP4C, LP4K (QTR: 2013-00487 REV: 04)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

Technical Articles

- Wideband Phase-Locked Loops with Integrated Voltage Controlled Oscillators

DESIGN RESOURCES

- HMC704 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC704 EngineerZone Discussions.

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Table 1. Electrical Specifications

VDDCP, VPPCP = 5V+/-4%; RVDD, AVDD, DVDD, VDDPD, VCCPS = 3.3V +/-10%; AGND = DGND = 0V

Parameter	Conditions	Min.	Typ.	Max.	Units
RF INPUT CHARACTERISTICS	[6][7]				
RF Input Frequency Range	[1]	DC		8000	MHz
Prescaler Input Freq Range	[1]	DC		4000	MHz
Power Range	[13]	-15	-7	-3	dBm
Impedance	100 Ohms each leg||3pF		100||3		Ohms||pF
REF INPUT CHARACTERISTICS					
Frequency Range (3.3V)	[1][8]	DC	50	350	MHz
Power from 50Ohm Source	[12]		6		dBm
Impedance			100||3		Ohms||pF
Ref Divider Range (14 bit)		1		16,383	
PHASE DETECTOR RATE	[1][12]				
Integer Mode		DC	50	115	MHz
Fractional Mode A		DC	50	80	MHz
Fractional Mode B		DC	50	100	MHz
CHARGE PUMP					
Output Current	20uA Steps	0.02		2.5	mA
POWER SUPPLIES					
RVDD, AVDD, VCCPS, VCCHF, VCCPD - Analog supply	All should be equal	3.0	3.3	3.5	V
DVDD - Digital supply		3.0	3.3	3.5	V
VDDLS, VPPCP Charge Pump	VDDLS, VPPCP must be equal	3.0	5.0	5.2	V
3.3V - Current consumption	[9]	38	52	58	mA
5V - Current consumption	All Modes	2	6	7	mA
Power Down Current	[10]			100	uA
BIAS Reference Voltage	Pin 12. Measured with 10GOhm Meter	1.880	1.920	1.960	V
PHASE NOISE					
Flicker Figure of Merit (FOM)[2]			-266		dBc/Hz
Floor Figure of Merit [11]	Integer HiK Mode Integer Normal Mode Fractional HiK Mode [3] Fractional Normal Mode [3]	-236 -232 -232 -228	-233 -230 -230 -227	-231 -228 -227 -225	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Flicker Noise at f_{offset}	PN_{flick} = Flicker FOM +20log(f_{vco}) -10log(f_{offset})				dBc/Hz
Phase Noise Floor at f_{vco} with f_{pd}	PN_{floor} = Floor FOM + 10log(f_{pd}) +20log(f_{vco}/f_{pd})				dBc/Hz
Total Phase Noise vs f_{offset}, f_{vco}, f_{pd}	PN = 10log(10$^{(PNflick/10)}$ + 10$^{(PNfloor/10)}$)				dBc/Hz
Jitter	SSB 100Hz to 50kHz		50		fs
SPURIOUS	[4][5]				
Integer Boundary Spurs @~8GHz	offsets less than loop bandwidth, f_{pd} = 50MHz		-60	-52	dBc

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Table 1. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
LOGIC INPUTS					
Switching Threshold (Vsw)	VIH/VIL within 50mV of Vsw	38	47	54	% DVDD
LOGIC OUTPUTS					
VOH Output High Voltage				VDD-0.4	V
VOL Output Low Voltage		0.4			V
Digital Output Driver Delay SCK to Digital Output Delay				0.5ns+0.2ns/pF 8.2ns+0.2ns/pF	ns ns
RF divider 8GHz Integer Mode	19 bit , Even values Only	32		1,048,574	
RF divider 4GHz Integer Mode	19 bit , All values	16		524,287	
RF divider 8GHz Fractional Mode	19 bit , Even values Only	40		1,048,566	
RF divider 4GHz Fractional Mode	19 bit , All values	20		524,283	

[1] Frequency is guaranteed across process, voltage and temperature from -40°C to 85°C.
[2] With high charge-pump current, +12dBm 100MHz sine reference
[3] Fractional FOM degrades about 3dB/octave for prescaler input frequencies below 2GHz
[4] Using 50MHz reference with VCO tuned to within one loop bandwidth of an integer multiple of the PD frequency. Larger offsets produce better results. See the “Spurious Performance” section for more information.
[5] Measured with the HMC704LP4E evaluation board. Board design and isolation will affect performance.
[6] Internal divide-by-2 must be enabled for frequencies >4GHz
[7] At low RF Frequency, Rise and fall times should be less than 1ns to maintain performance
[8] Slew rate of greater or equal to 0.5ns/V
[9] Current consumption depends upon operating mode and frequency of the VCO
[10] Reference input disconnected
[11] Min/Max versus temperature and supply, under typical reference & frequencies & RF power levels
[12] Slew > 0.5V/ns is recommended , see Table 6 for more information
[13] Operable with reduced spectral performance up to +7 dBm

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, plots are measured with a 50 MHz PD rate, VCO near 8 GHz. The operating modes in the following plots refer to Integer (int), Fractional Modes A and B, HiKcp (HiK) or Active (act) configurations.

Figure 1. Floor FOM vs. Mode and Temp

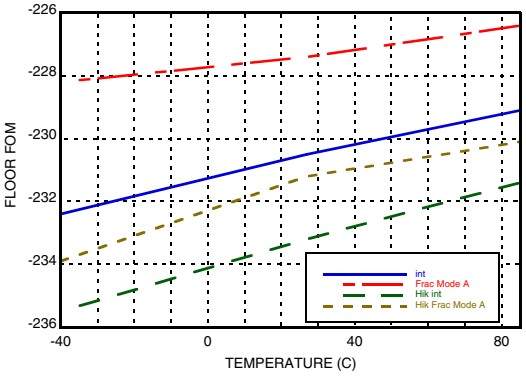

Figure 2. Flicker FOM vs. Mode and Temp

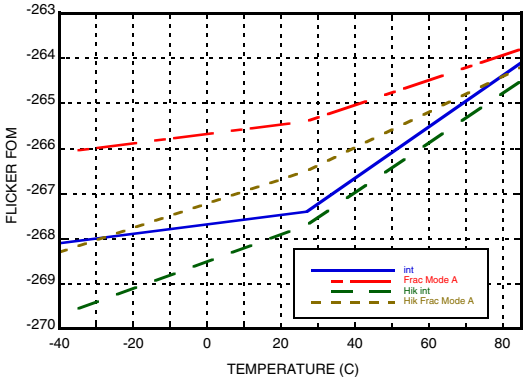

Figure 3. Floor FOM vs. Output Frequency and Mode

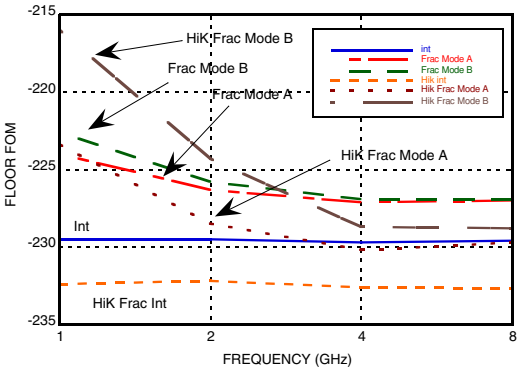

Figure 4. Flicker FOM vs. Output Frequency and Mode

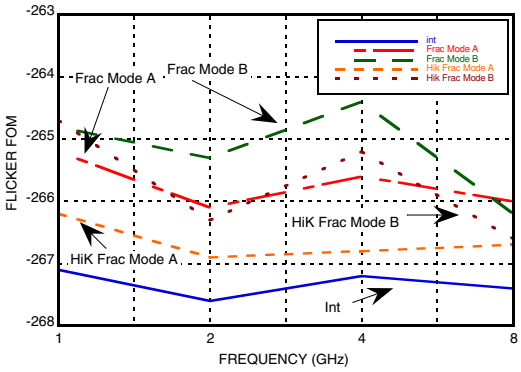

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Figure 5. Floor FOM vs. Reference Power and Mode

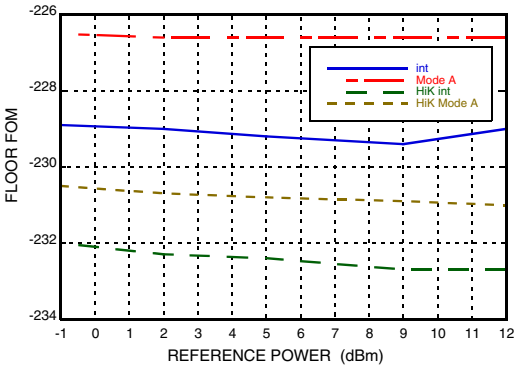

Figure 6. Flicker FOM vs. Reference Power and Mode

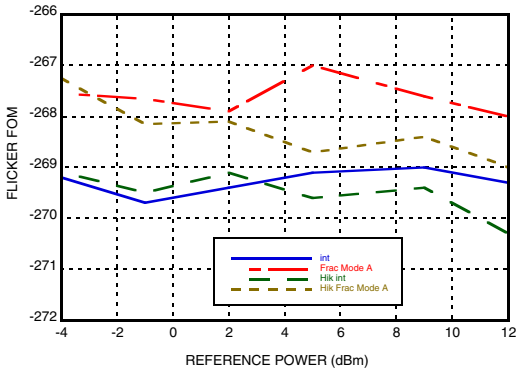

Figure 7. Flicker FOM vs. Charge Pump Current

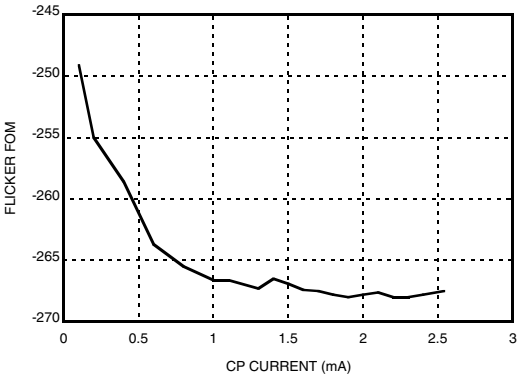

Figure 8. Flicker FOM vs. CP Voltage, CP Current = 2.5mA

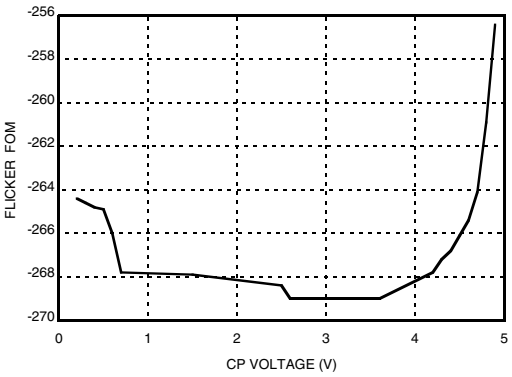

Figure 9. Flicker FOM vs. CP Voltage, Hikcp + CP Current = 6mA

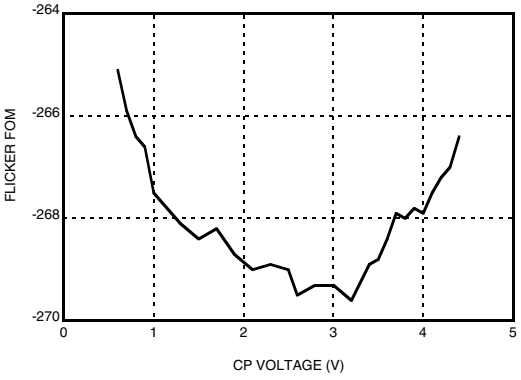

Figure 10. Floor FOM vs. CP Voltage, CP Current = 2.5mA

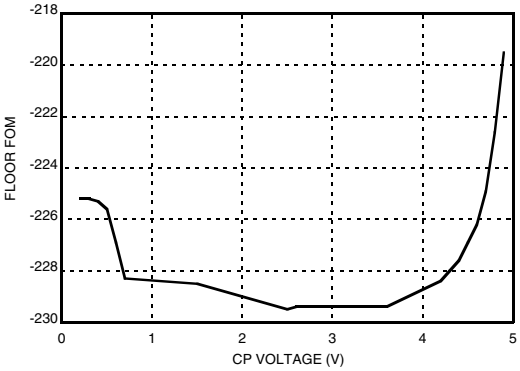

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Figure 11. Floor FOM vs. CP Voltage, Hikcp+CP Current = 6mA

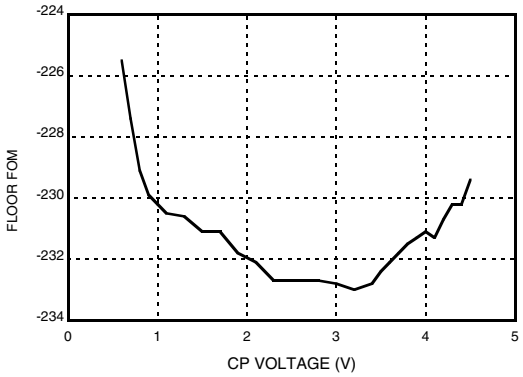


Figure 12. Floor FOM vs. CP Current

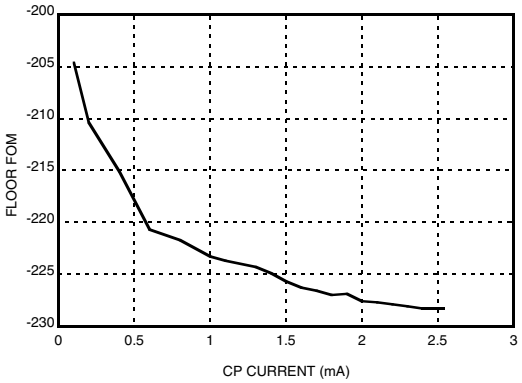


Figure 13. Spur Performance vs. Frequency Offset[1]

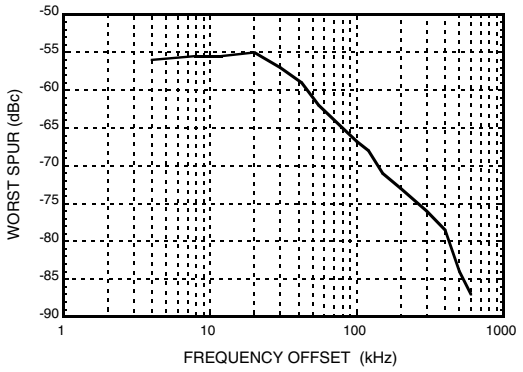


Figure 14. Spur Performance vs. Frequency Offset [2]

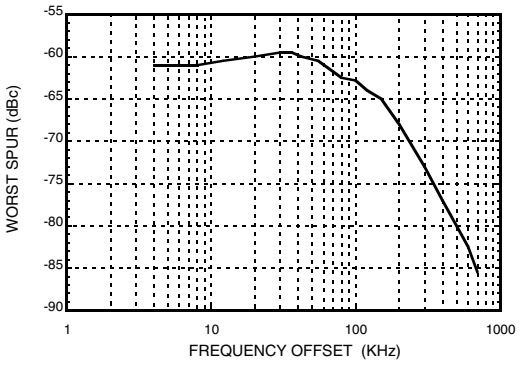


Figure 15. Worst Case Integer Boundary Spur Near 8 GHz

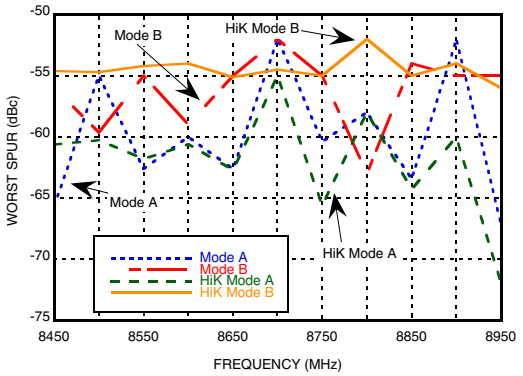
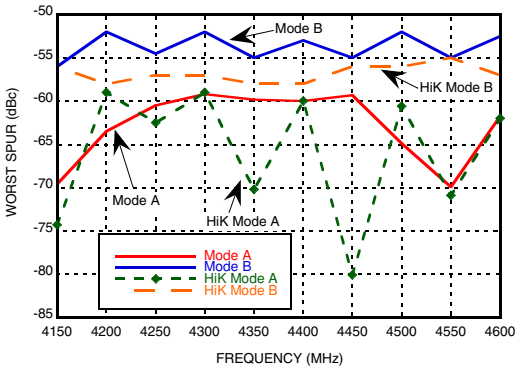


Figure 16. Worst Case Integer Boundary Spur Near 4 GHz



[1] CP Current = 2.5 mA, Loop Filter = 20 kHz, Phase Margin = 78°

[2] Hi K, CP Current = 6 mA, Loop Filter BW = 45 kHz, Phase Margin = 78°

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Figure 17. Integer Boundary Spur vs. CP Offset [3]

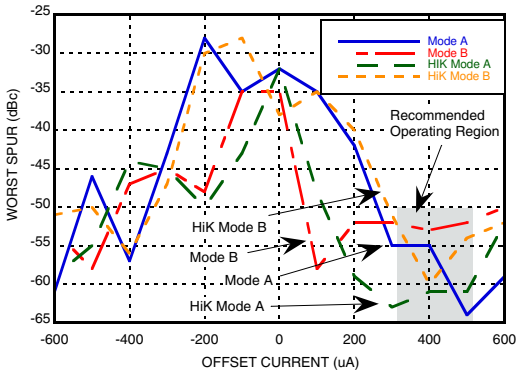


Figure 18. Modelled vs. Measured Phase Noise [4]

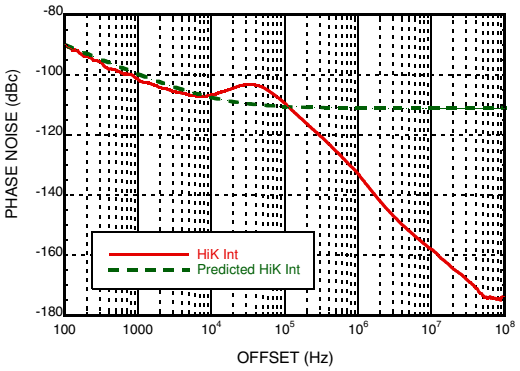


Figure 19. Modelled vs. Measured Phase Noise, Fractional Mode [3]

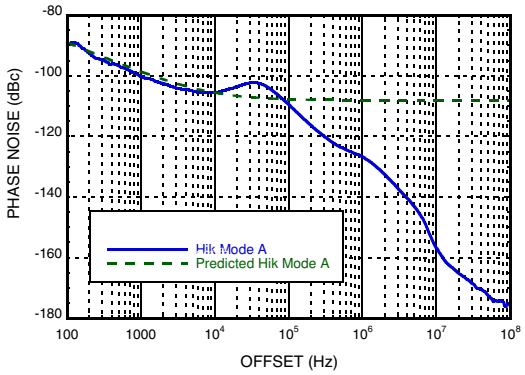


Figure 20. Floor FOM Near 8 GHz vs. RF Power and Mode

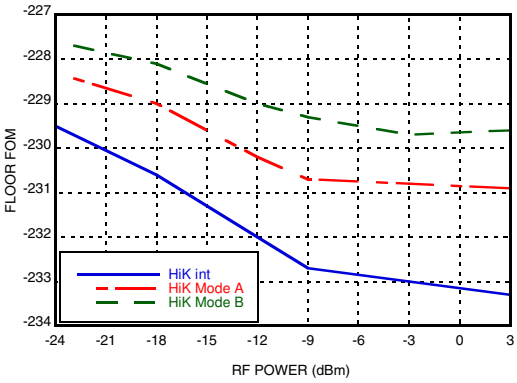


Figure 21. Flicker FOM Near 8 GHz vs. RF Power and Mode

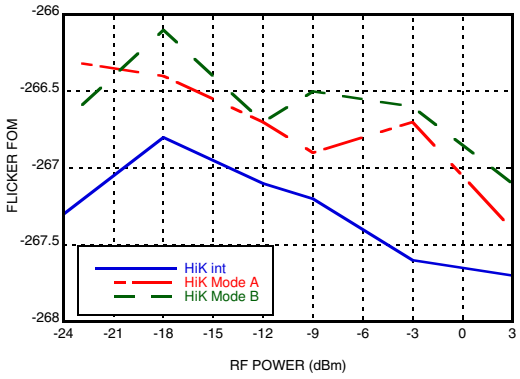
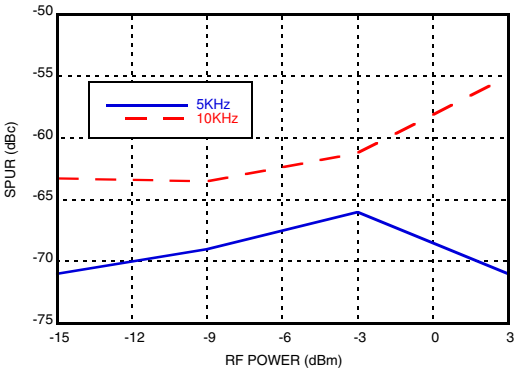


Figure 22. Integer Boundary Spurious at 8 GHz + 10 kHz vs. RF Power [3]



[3] VCO Near 8.6 GHz, Prescalar = VCO/2

[4] Active Fractional A Mode (Prescalar @ 4 GHz + 5 kHz)

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Table 2. Pin Descriptions

Pin Number	Function	Description
1	SDI	Main Serial port data input
2	SCK	Main Serial port clock input
3	ASEN	Auxiliary Serial Port Enable Output
4	LD_SDO	Lock Detect Output or Serial Data Output or GPO, Selectable
5	VCOIN	Complementary Input to the RF Prescaler. For Single Ended operation must be decoupled to the ground plane with a ceramic bypass capacitor, typically 100 pF. DC Bias of 2.0V is generated internally
6	VCOIP	Input to the RF Prescaler. Small signal input from external VCO. DC Bias of 2.0V is generated internally. External AC Coupling required
7	VCCHF	Power supply pin for the RF Section. Nominal +3.3 V. A decoupling capacitor to the ground plane should be placed as close as possible to this pin. See eval board layout.
8	N/C	No Connect
9	VCCPS	Power Supply Prescaler, Nominal +3.3V
10	N/C	No Connect
11	VCCPD	Power supply for the phase detector, Nominal +3.3V
12	BIAS	External bypass decoupling for precision bias circuits, 1.920V +/-20 mV NOTE: BIAS ref voltage cannot drive an external load. Must be measured with 10 GOhm meter such as Agilent 34410A, normal 10 Mohm DVM will read erroneously.
13	N/C	No Connect
14	AVDD	Power supply for analog bias generation, Nominal +3.3V
15	VPPCP	Power supply for charge pump, Nominal +5V
16	CP	Charge pump output.
17	VDDLS	Power Supply for charge pump digital section, Nominal +5V
18	RVDD	Ref path supply, Nominal +3.3V
19	XREFP	Reference input
20	ASCK	Auxiliary Serial Port Clock Output
21	ASD	Auxiliary Serial Port Data Output
22	DVDD	Digital supply, Nominal +3.3V
23	CEN	Hardware Chip Enable
24	SEN	Main Serial port latch enable input

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Table 3. Absolute Maximum Ratings

Parameter	Rating
AVDD or DVDD to GND	-0.3V to +3.6V
AVDD to DVDD	-0.5V to +0.5V
VDDLS, VPPCP	-0.3V to +5.2V
VCOIN, VCOIP Single Ended DC	VCCHF-0.2V
VCOIN, VCOIP Differential DC	5.2V
VCOIN, VCOIP Single Ended AC 50Ohm	+7 dBm
VCOIN, VCOIP Differential AC 50Ohm	+13 dBm
XREFP reference input	+18dBm, 5.6Vpeak
Digital Load	1kOhm min
Digital Input 1.4V to 1.7V min rise time	20nsec
Digital Input Voltage Range	-0.25 to DVDD+0,5V
Thermal Resistance (Jxn to Gnd Paddle)	25 °C/W
Operating Temperature Range	-40 °C to +85 °C
Storage Temperature Range	-65 °C to + 125 °C
Maximum Junction Temperature	+125 °C
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40sec
ESD Sensitivity HBM	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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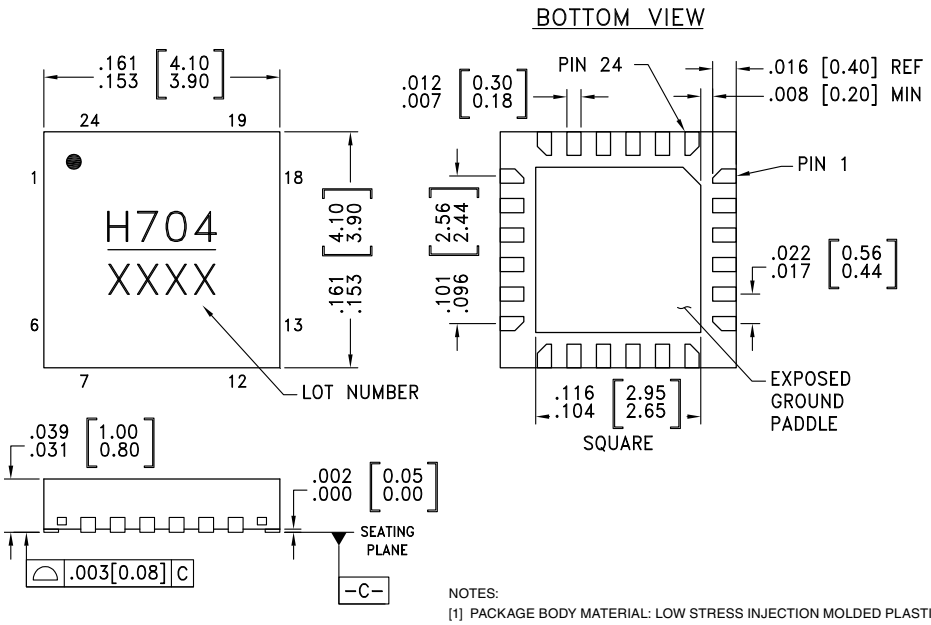
Outline Drawing



NOTES:

[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15 mm MAX. PAD BURR HEIGHT SHALL BE 0.05 mm MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05 mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 4. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC704LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1[2]	H704 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260°C

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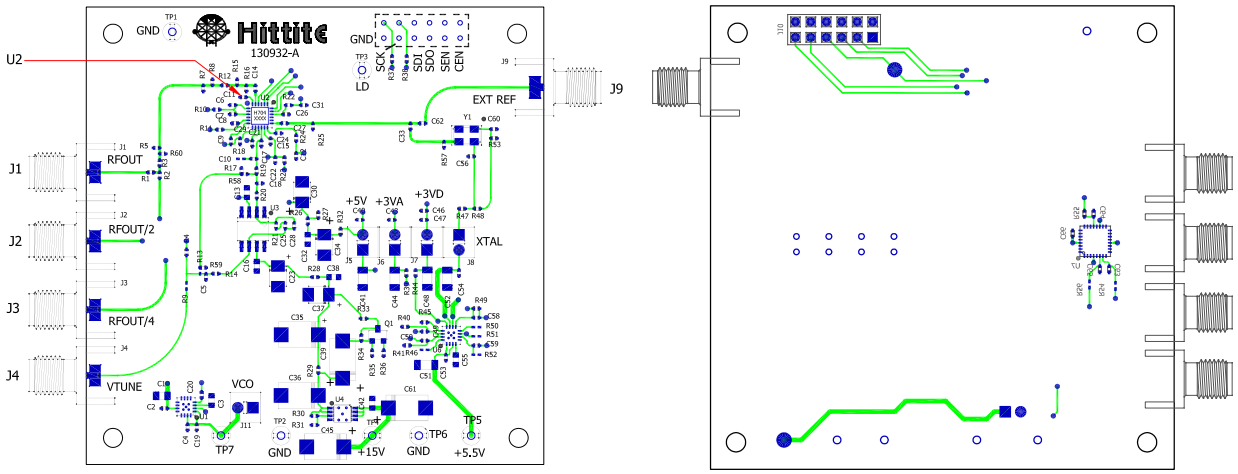
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 5. Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit	HMC704LP4E Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	129856-HMC704LP4E

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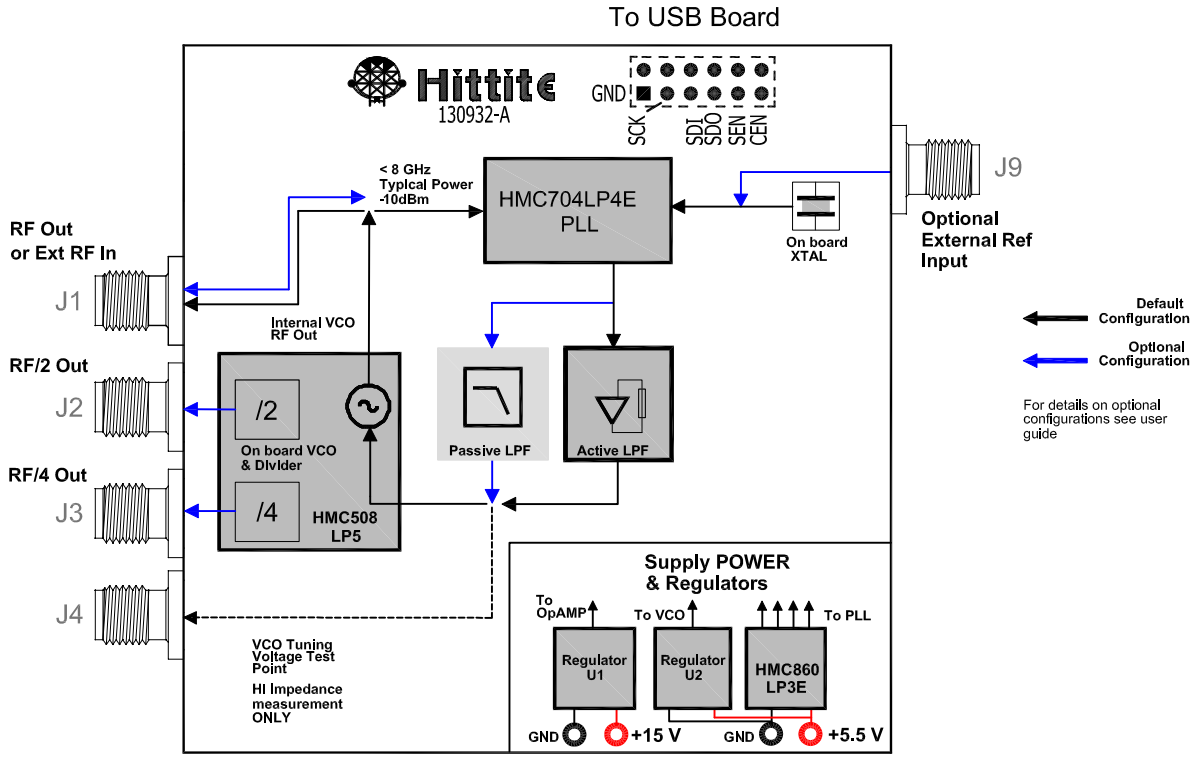
Evaluation PCB Block Diagram



Evaluation PCB Schematic

To view Evaluation PCB Schematic please visit www.hittite.com and choose HMC704LP4E from "Search by Part Number" pull down menu to view the product splash page.

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Theory of Operation

The PLL consists of the following functional blocks:

1. Reference Path Input Buffer and 'R' Divider
2. VCO Path Input Buffer, RF Divide-by-2 and Multi-Modulus 'N' Divider
3. $\Delta\Sigma$ Fractional Modulator
4. Phase Detector
5. Charge Pump
6. Main Serial Port
7. Lock Detect and Register Control
8. Auxiliary Output Serial Port
9. Power On Reset Circuit

External VCO

The PLL charge pump can operate with the charge pump supply as high as 5.2V. The charge pump output at the varactor tuning port, normally can maintain low noise performance to within 500 mV of ground or 800 mV of the upper supply voltage.

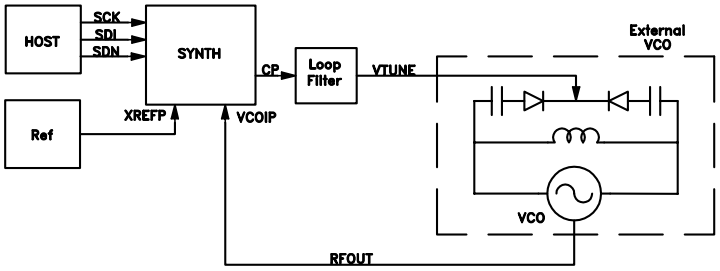

Figure 23. Synthesizer with External VCO

High Performance Low Spurious Operation

The HMC704LP4E has been designed for the best phase noise and low spurious content possible in an integrated PLL. Spurious signals in a PLL can occur in any mode of operation and can come from a number of sources.

Figure of Merit Noise Floor and Flicker Noise Models

The phase noise of an ideal phase locked oscillator is dependent upon a number of factors:

- **a.** Frequency of the VCO, and the Phase detector
- **b.** VCO Sensitivity, kvco, VCO and Reference Oscillator phase noise profiles
- **c.** Charge Pump current, Loop Filter and Loop Bandwidth
- **d.** Mode of Operation: Integer, Fractional modulator style

The contributions of the PLL to the output phase noise can be characterized in terms of a Figure of Merit (FOM) for both the PLL noise floor and the PLL flicker (1/f) noise regions, as follows:

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where:

Φ_p^2	Phase Noise Contribution of the PLL (rads^2/Hz)
f_o	Frequency of the VCO (Hz)
f_{pd}	Frequency of the Phase Detector (Hz)
f_m	Frequency offset from the carrier (Hz)
F_{po}	Figure of Merit (FOM) for the phase noise floor
F_{p1}	Figure of Merit (FOM) for the flicker noise region

PLL Phase Noise Contribution

$$\Phi_p^2\left(f_0, f_m, f_{pd}\right) = \frac{F_{p_1} f_0^2}{f_m} + \frac{F_{p_0} f_0^2}{f_{f_d}} \qquad \textit{(EQ 1)}$$

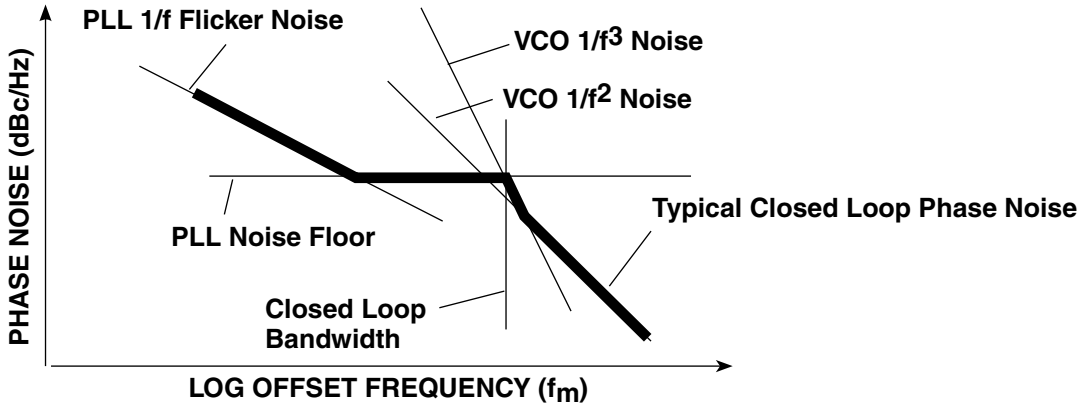

Figure 24. Figures of Merit Noise Models for the PLL

If the free running phase noise of the VCO is known, it may also be represented by a figure of merit for both $1/f^2$, F_{v2}, and the $1/f^3$, F_{v3}, regions.

VCO Phase Noise Contribution

$$\Phi_v^2\left(f_0, f_m\right) = \frac{F_v f_0^2}{f_m^2} + \frac{F_{v_3} f_0^2}{f_m^3} \qquad \textit{(EQ 2)}$$

The Figures of Merit are essentially normalized noise parameters for both the PLL and VCO that can allow quick estimates of the performance levels of the PLL at the required VCO, offset and phase detector frequency. Normally, the PLL IC noise dominates inside the closed loop bandwidth of the PLL, and the VCO dominates outside the loop bandwidth at offsets far from the carrier. Hence a quick estimate of the closed loop performance of the PLL can be made by setting the loop bandwidth equal to the frequency where the PLL and free running phase noise are equal.

The Figure of Merit is also useful in estimating the noise parameters to be entered into a closed loop design tool such as Hittite PLL Design, which can give a much more accurate estimate of the closed loop phase noise and PLL loop filter component values.

Given an optimum loop design, the approximate closed loop performance is simply given by the minimum of the PLL and VCO noise contributions.

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PLL-VCO Noise

$$\Phi^2 = \min\left(\Phi_p^2, \Phi_v^2\right) \quad \textbf{(EQ 3)}$$

An example of the use of the FOM values to make a quick estimate of PLL performance: Estimate the phase noise of an 8GHz closed loop PLL with a 100MHz reference operating in Fractional Mode B with the VCO operating at 8 GHz and the VCO divide by 2 port driving the PLL at 4GHz. Assume an HMC509 VCO has free running phase noise in the $1/f^2$ region at 1 MHz offset of -135 dBc/Hz and phase noise in the $1/f^3$ region at 1 kHz offset of -60 dBc/Hz.

F_{v1_dB} =	-135	Free Running VCO PN at 1MHz offset
	+20*log10(1e6)	PNoise normalized to 1Hz offset
	-20*log10(8e9)	Pnoise normalized to 1Hz carrier
	= -213.1 dBc/Hz at 1Hz	VCO FOM
F_{v3_dB} =	-60	Free Running VCO PN at 1kHz offset
	+30*log10(1e3)	PNoise normalized to 1 Hz offset
	-20*log10(8e9)	Pnoise normalized to 1 Hz carrier
	= -168 dBc/Hz at 1Hz	VCO Flicker FOM

We can see from Figure 3 and Figure 4 respectively that the PLL FOM floor and FOM flicker parameters in fractional Mode A:

Fpo_dB = -227 dBc/Hz at 1Hz
Fp1_dB = -266 dBc/Hz at 1Hz

Each of the Figure of Merit equations result in straight lines on a log-frequency plot. We can see in the example below the resulting

PLL floor at 8 GHz = F_{po_dB} +20log10(fvco) -10log10(fpd) = -227+198 -80 = -109 dBc/Hz
PLL Flicker at 1 kHz = F_{p1_dB}+20log10(fvco)-10log10(fm) = -266 +198-30 = -98 dBc/Hz
VCO at 1 MHz = F_{v1_dB}+20log10(fvco)-20log10(fm)= -213 +198-120 = -135dBc/Hz
VCO flicker at 1 kHz = F_{v3_dB}+20log10(fvco)-30log10(fm)= -168 +198-90 = -60dBc/Hz

These four values help to visualize the main contributors to phase noise in the closed loop PLL. Each falls on a linear line on the log-frequency phase noise plot shown in Figure 25.

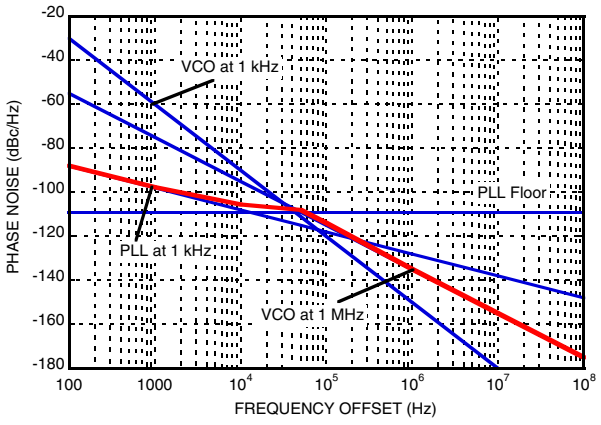

Figure 25. Example of Figure of Merit models at 8 GHz

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It should be noted that actual phase noise near the corner frequency of the loop bandwidth is affected by loop parameters and one should use a more complete design tool such as Hittite PLL Design for better estimates of the phase noise performance. Noise models for each of the components in Hittite PLL Design can be derived from the FOM equations or can be provided by Hittite applications engineering.

Spurious Performance

Integer Operation

The VCO always operates at an integer multiple of the PD frequency in an integer PLL. In general spurious signals originating from an integer PLL can only occur at multiples of the PD frequency. These unwanted outputs are often simply referred to as reference sidebands.

Spurs unrelated to the reference frequency must originate from outside sources. External spurious sources can modulate the VCO indirectly through power supplies, ground, or output ports, or bypass the loop filter due to poor isolation of the filter. It can also simply add to the output of the PLL.

The HMC704LP4E has been designed and tested for ultra-low spurious performance. Reference spurious levels are typically below -100 dBc with a well designed board layout. A regulator with low noise and high power supply rejection, such as the HMC860LP3E, is recommended to minimize external spurious sources.

Reference spurious levels of below -100 dBc require superb board isolation of power supplies, isolation of the VCO from the digital switching of the PLL and isolation of the VCO load from the PLL. Typical board layout, regulator design, demo boards and application information are available for very low spurious operation. Operation with lower levels of isolation in the application circuit board, from those recommended by Hittite, can result in higher spurious levels.

Of course, if the application environment contains other interfering frequencies unrelated to the PD frequency, and if the application isolation from the board layout and regulation are insufficient, then the unwanted interfering frequencies will mix with the desired PLL output and cause additional spurs. The level of these spurs is dependant upon isolation and supply regulation or rejection (PSRR).

Fractional Operation

Unlike an integer PLL, spurious signals in a fractional PLL can occur due to the fact that the VCO operates at frequencies unrelated to the PD frequency. Hence intermodulation of the VCO and the PD harmonics can cause spurious sidebands. Spurious emissions are largest when the VCO operates very close to an integer multiple of the PD. When the VCO operates exactly at a harmonic of the PD then, no in-close mixing products are present.

Interference is always present at multiples of the PD frequency, f_{pd}, and the VCO frequency, f_{vco}. If the fractional mode of operation is used, the difference, Δ, between the VCO frequency and the nearest harmonic of the reference, will create what are referred to as integer boundary spurs. Depending upon the mode of operation of the PLL, higher order, lower power spurs may also occur at multiples of integer fractions (sub-harmonics) of the PD frequency. That is, fractional VCO frequencies which are near $nf_{pd} + f_{pd}d/m$, where n, d and m are all integers and d<m (mathematicians refer to d/m as a rational number). We will refer to $f_{pd}d/m$ as an integer fraction. The denominator, m, is the order of the spurious product. Higher values of m produce smaller amplitude spurious at offsets of $m\Delta$ and usually when m>4 spurs are very small or unmeasurable.

The worst case, in fractional mode, is when d=0, and the VCO frequency is offset from nf_{pd} by less than the loop bandwidth. This is the “in-band fractional boundary” case.

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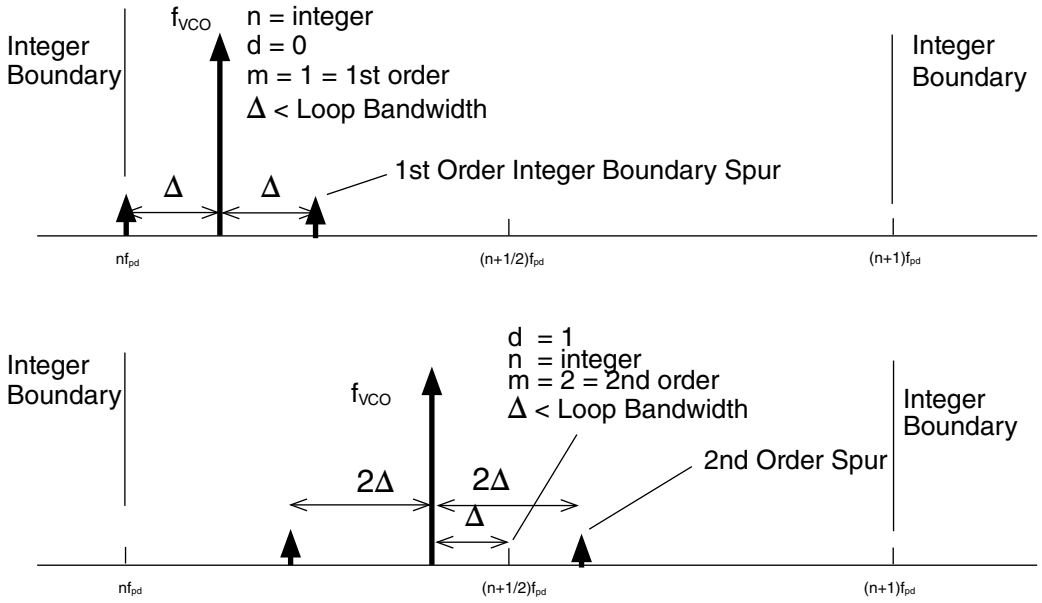

Figure 26. Fractional Spurious Example

Characterization of the levels and orders of these products is not unlike a mixer spur chart. Exact levels of the products are dependent upon isolation of the various PLL parts. Hittite can offer guidance about expected levels of spurious with our PLL and VCO application boards. Regulators with high power supply rejection ratios (PSRR) are recommended, especially in noisy applications.

When operating in fractional mode, charge pump and phase detector linearity is of paramount importance. Any non-linearity degrades phase noise and spurious performance. Phase detector linearity degrades when the phase error is very small and is operating back and forth between reference lead and VCO lead. To mitigate these non-linearities in fractional mode it is critical to operate the phase detector with some finite phase offset such that either the reference or VCO always leads. To provide a finite phase error, extra current sources can be enabled which provide a constant DC current path to VDD (VCO leads always) or ground (reference leads always). These current sources are called charge pump offset and they are controlled via "Reg 09h". The time offset at the phase detector should be ~2.5 ns + $4T_{ps}$, where T_{ps} is the RF period at the fractional prescaler input in nanoseconds (ie. after the optional fixed divide by 2). The specific level of charge pump offset current is determined by this time offset, the comparison frequency and the charge pump current and can be calculated from:

$$\text{Required CP Offset } (\mu A) = \left(2.5\times10^{-9} + 4T_{PS}\right)(\text{sec})\times\left(F_{comparison}\right)(Hz)\times I_{CP}(\mu A) \qquad \textbf{(EQ 4)}$$

CP Offset Current should never be more than 25% of the programmed CP current. Operation with charge pump offset influences the required configuration of the Lock Detect function. Refer to the description of "PD Window Based Lock Detect" later in this document. Note that this calculation can be performed for the center frequency of the VCO, and does not need refinement for small differences (<25%) in center frequencies.

Another factor in the spectral performance in Fractional Mode is the choice of the Delta-Sigma Modulator mode. Mode A can offer better in-band spectral performance (inside the loop bandwidth) while Mode B offers better out of band performance. See "Reg 06h"[3:2] for DSM mode selection. Finally, all fractional PLLs create fractional spurs at some level. Hittite offers the lowest level fractional spurious in the industry in an integrated solution.

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Reference Input Stage

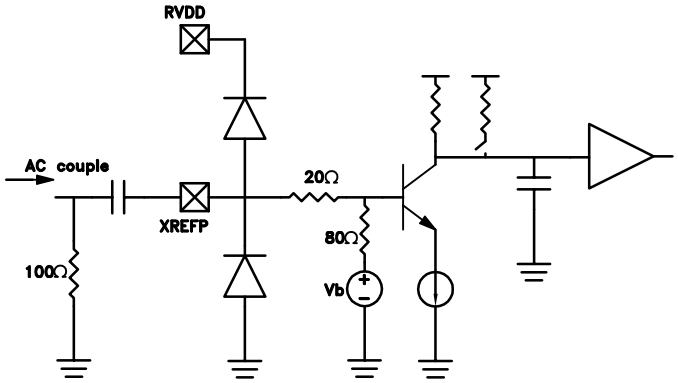

Figure 27. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation. High Gain (recommended below 200 MHz), and High frequency, for 200 to 350 MHz operation. The buffer is internally DC biased, with 100 Ohm internal termination. For 50 Ohm match, an external 100 Ohm resistance to ground should be added, followed by an AC coupling capacitance (impedance < 1 Ohm), then to the XREFP pin of the part.

At low frequencies, a relatively square reference is recommended to keep the input slew rate high. At higher frequencies, a square or sinusoid can be used. The following table shows the recommended operating regions for different reference frequencies. If operating outside these regions the part will normally still operate, but with degraded performance.

Minimum pulse width at the reference buffer input is 2.5 ns. For best spur performance when R = 1, the pulse width should be (2 .5ns + 8 Tps), where Tps is the period of the VCO at the prescaler input. When R > 1 minimum pulse width is 2.5 ns.

Table 6. Reference Sensitivity Table

	Square Input			Sinusoidal Input		
Frequency (MHz)	Slew > 0.5 V/ns	Recommended Swing (Vpp)			Recommended Power Range (dBm)	
	Recommended	Min	Max	Recommended	Min	Max
< 10	YES	0.6	2.5	x	x	x
10	YES	0.6	2.5	x	x	x
25	YES	0.6	2.5	ok	8	15
50	YES	0.6	2.5	YES	6	15
100	YES	0.6	2.5	YES	5	15
150	ok	0.9	2.5	YES	4	12
200	ok	1.2	2.5	YES	3	8
200 to 350	x	x	x	YES[1]	5	10
Note: For greater than 200 MHz operation, use buffer in High Frequency Mode. Reg[8] bit 21 = 1						

Input referred phase noise of the PLL when operating at 50 MHz is between -150 and -156 dBc/Hz at 10 kHz offset depending upon the mode of operation. The input reference signal should be 10 dB better than this floor to avoid degradation of the PLL noise contribution. It should be noted that such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

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Ref Path 'R' Divider

The reference path "R" divider is based on a 14 bit counter and can divide input signals of up to 350 MHz input by values from 1 to 16,383 and is controlled by "Reg 02h"[13:0]. The reference divider output may be viewed in test mode on the LD_SDO pin, by setting "Reg 0Fh"[4:0] = 9d.

RF Path

The RF path is shown in Figure 28. This path features a low noise 8 GHz RF input buffer followed by an 8GHz RF divide-by-2 with a selectable bypass. If the VCO input is below 4 GHz the RF divide-by-2 should be by-passed for reduced power consumption and improved performance in fractional mode. The RF divide-by-2 is followed by the N divider, a 19 bit divider that can operate in either integer or fractional mode with up to 4 GHz inputs. Finally the N divider is followed by the Phase Detector (PD), which has two inputs, the RF path from the VCO (V) and the reference path (R) from the crystal. The PD can operate at speeds up to 80 MHz in fractional Mode A, 100 MHz in fractional Mode B and 115 MHz in integer mode.

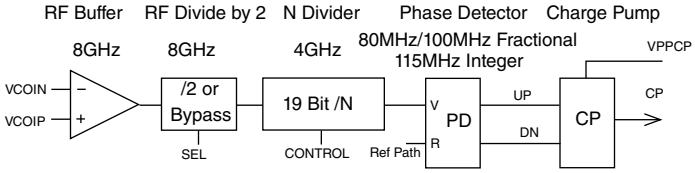

Figure 28. RF Path

RF Input Stage

The RF input stage provides the path from the external VCO to the phase detector via the RF or 'N' divider. The RF input path is rated to operate up to 8 GHz across all conditions. The RF input stage is a differential common emitter stage with internal DC bias, and is protected by ESD diodes as shown in Figure 29. This input is not matched to 50 Ohms. A 50 Ohm resistor placed across the inputs can be used if desired. In most applications the input is used single-ended into either the VCOIP or VCOIN pin with the other input connected to ground through a DC blocking capacitor. The preferred input level for best spectral performance is -10 dBm nominally.

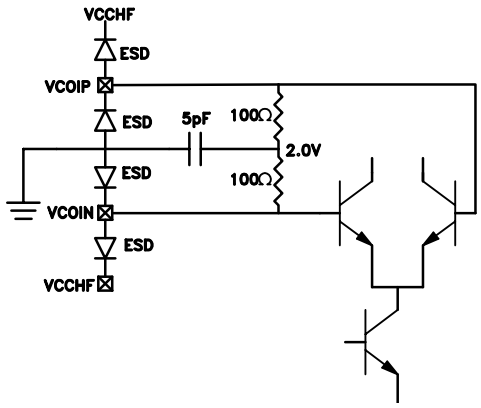

Figure 29. RF Input Stage

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RF Path 'N' Divider

The main RF path 'N' divider is capable of divide ratios anywhere between 2^{19}-1 (524,287) and 16 . This divider for example could divide a 4 GHz input to a PD frequency anywhere between its maximum output limit of 115 MHz to as low as 7.6 kHz. The 'N' divider output may be viewed in test mode on LD_SDO by setting "Reg 0Fh"[4:0] = 10 d. When operating in fractional mode the N divider can change by up to +/-4 from the average value. Hence the selected divide ratio in fractional mode is restricted to values between 2^{19}-5 (524,283) and 20.

If the VCO input is above 4 GHz then the 8 GHz fixed RF divide-by-2 should be used, "Reg 08h"[19] = 1. In this case the total division range is restricted to even numbers over the range $2*(2^{19}-5)$ (1,048,566) to 40.

Charge Pump and Phase Detector

The Phase Detector or PD has two inputs, one from the reference path divider and one from the RF path divider. When in lock these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. We refer to the frequency of operation of the PD as f_{pd}. Most formula related to step size, delta-sigma modulation, timers etc., are functions of the operating frequency of the PD, f_{pd} is sometimes referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies in a linear fashion over nearly ±2π radians (±360) of input phase difference.

Phase Detector and Charge Pump Functions

Phase detector register "Reg 08h" allows manual access to control special phase detector features.

"Reg 0Bh"[2:0] allows fine tuning of the PD reset path delay. This adjustment can be used to improve performance at very high PD rates. Most often this register is set to the recommended value only.

"Reg 06h"[5] and [6] enables the PD UP and DN outputs respectively. Disabling prevents the charge pump from pumping up or down respectively and effectively tri-states the charge pump while leaving all other functions operating internally.

CP Force UP "Reg 08h"[9] and CP Force DN "Reg 00h"[10] allows the charge pump to be forced up or down respectively. This will force the VCO to the ends of the tuning range which can be useful for testing of the VCO.

PD Force Mid "Reg 0Bh"[11] will disable the charge pump current sources and place a voltage source on the loop filter at approximately VPPCP/2. If a passive filter is used this will set the VCO to the mid-voltage tuning point which can be useful for testing of the VCO.

"Reg 0Bh"[21:7] control other aspects of the phase detector operation and should be set to recommended values.

PLL Jitter

The standard deviation of the arrival time of the VCO signal, or the jitter, may be estimated with a simple approximation if we assume that the locked VCO has a constant phase noise, $\Phi^2(f_0)$, at offsets less than the loop 3 dB bandwidth and a 20 dB per decade roll off at greater offsets. The simple locked VCO phase noise approximation is shown on the left of Figure 30.

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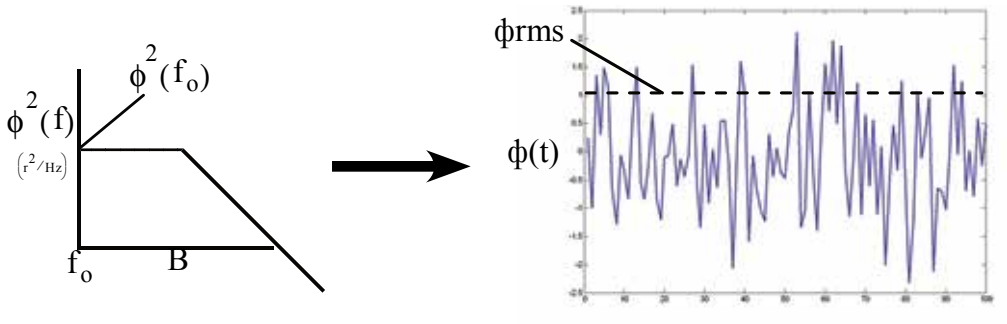

Figure 30. Synthesizer Phase Noise and Jitter

With this simplification the total integrated VCO phase noise, Φ_v^2, in rads² is given by

$$\Phi_v^2 = \Phi^2(f_0)B\pi \qquad \textbf{(EQ 5)}$$

where
$\Phi^2(f_0)$ is the single sideband phase noise in rads²/Hz inside the loop bandwidth, and
B is the 3dB corner frequency of the closed loop PLL

The integrated phase noise at the phase detector, Φ_{pd}^2, is just scaled by N² ie. $\Phi_{pd}^2 = \frac{\Phi_v^2}{N^2}$

The rms phase jitter of the VCO (Φ_v) in rads, is just the square root of the phase noise integral.

Since the simple integral of (EQ 5) is just a product of constants, we can easily do the integral in the log domain. For example if the phase noise inside the loop is -110 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio is 100, then the integrated phase noise at the phase detector, in dB, is given by;

$\Phi_{pd}^2 dB = 10\log\left(\Phi^2(f_0)\beta\pi/N^2\right)$ = -110 + 5 +50 - 40 = -95 dBrads, or equivalently $\Phi = 10^{-95/20}$ = 18urads = 1 milli-degrees rms.

While the phase noise reduces by a factor of 20logN after division to the reference, due to the increased period of the PD reference signal, the jitter is constant.

The rms jitter from the phase noise is then given by $T_{jpn} = T_{pd}\Phi_{pd}/2\pi$

In this example if the PD reference was 50 MHz, T_{pd} = 20 nsec, and hence T_{jpn} = 56 femto-sec.

PD Window Based Lock Detect

Lock Detect Enable "Reg 07h"[3] = 1 is a global enable for all lock detect functions.

The window based Lock Detect circuit effectively measures the difference between the arrival of the reference and the divided VCO signals at the PD. The arrival time difference must consistently be less than the Lock Detect window length, to declare lock. Either signal may arrive first, only the difference in arrival times is counted.

Analog Window Lock Detect

The lock detect window may be generated by either an analog circuit or a digital one-shot circuit. Clearing "Reg 07h"[6]=0 will result in a fixed, analog, nominal 10 nsec window, as shown in Figure 31. The analog window cannot be used if the PD rate is very high, for example near 100 MHz, or if the charge pump offset current results in an offset larger than 7 nsec.

For example a 25 MHz PD rate with a 1mA charge pump setting ("Reg 09h"[6:0]="Reg 09h"[13:7]= 50d) and a -400uA offset current "Reg 09h"[20:14]=80d), would have a phase offset of about 400/1000 = 40% of the PD period or about 16 nsec. In such an extreme case the divided VCO would arrive 16 ns after the PD reference, and would always arrive outside of the 10 nsec lock detect window. In such a case the lock detect circuit would always read unlocked, even though the VCO might be locked. The charge pump current, reference period, charge pump offset current, and lock detect window are related.

Digital Window Lock Detect

Setting "Reg 07h"[6]=1 will result in a variable length lock detect window based upon the internal digital timer. The one shot timer period is controlled by "Reg 07h"[11:10]. The resulting lock detect window period is then generated by the number of timer periods defined in "Reg 07h"[9:7].

Declaration of Lock

"Reg 07h"[2:0] defines the number of consecutive counts of the divided VCO that must land inside the lock detect window to declare lock. If for example we set "Reg 07h"[2:0] =5 then the VCO arrival would have to occur inside the widow 2048 times in a row to be declared locked, which would result in a Lock Detect Flag high. A single occurrence outside of the window will result in an out of lock, i.e. Lock Detect Flag low. Once low, the Lock Detect Flag will stay low until the lkd_wincnt_max = 2048 condition is met again.

The Lock Detect Flag status is always readable in "Reg 12h"[1]. Lock Detect status is also output to the LD_SDO pin if "Reg 0Fh"[4:0]=1, "Reg 0Fh"[6]=1 and "Reg 0Fh"[7]=1. Clearing"Reg 0Fh"[6]=0 will display the Lock Detect Flag on LD_SDO except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin and returns to the Lock Detect Flag after the read is completed. Timing of the Lock Detect function is shown in Figure 31 and Figure 32.

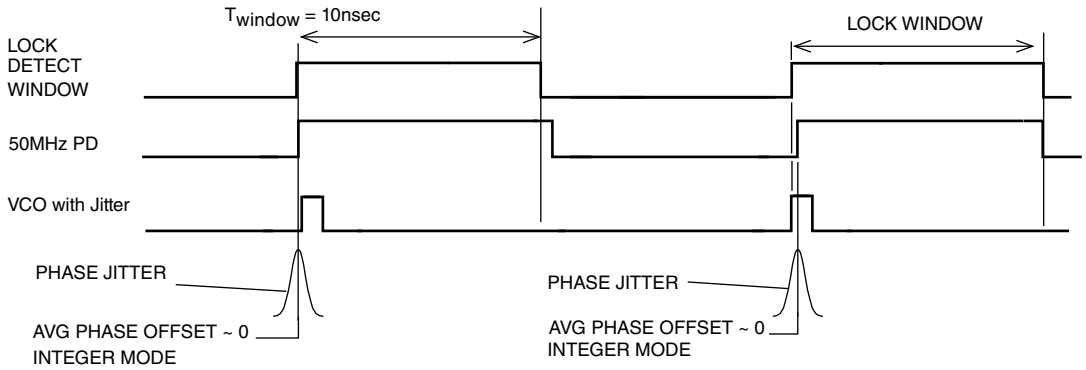

Figure 31. Normal Lock Detect Window - Integer Mode, Zero Offset

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Lock Detect Operation with Phase Offset

When operating in fractional mode the linearity of the charge pump and phase detector are much more critical than in integer mode. The phase detector linearity degrades when operated with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the reference and VCO at the phase detector. In such a case, for example with an offset delay, as shown in Figure 32, the VCO arrival may always occur after the reference. The lock detect circuit window may need to be adjusted to allow for the delay being used, if the delay is large.

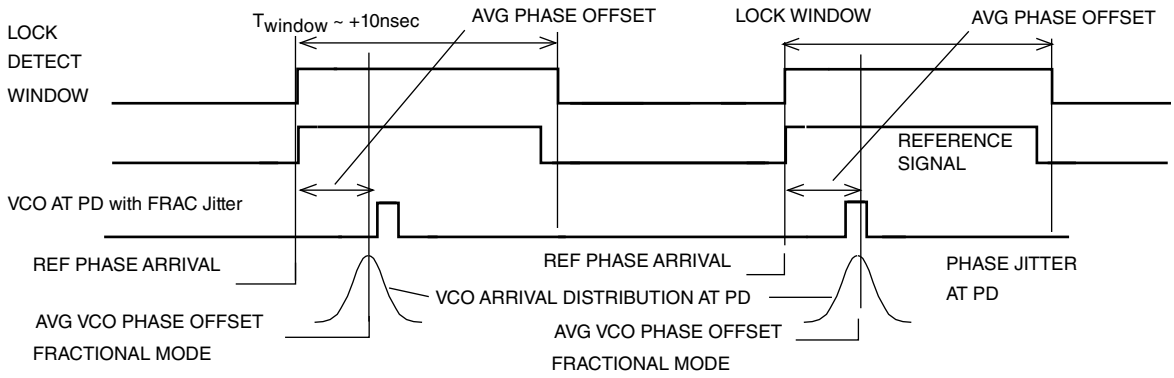

Figure 32. Lock Detect Window - Fractional Mode with Offset

In integer mode, 0 offset is recommended. In fractional mode, the time offset should be set to ~ 2.5 ns + 4 Tps, where Tps is the RF period at the fractional prescaler input (i.e. after the optional fixed divide by 2). Refer to the Fractional Operation section for further details about calculating charge pump offset currents

Digital Lock Detect with Digital Window Example

Typical Digital Lock detect window widths are shown in Table 7. Lock Detect windows typically vary +/-10% vs voltage and +/-15% over -40 C to +85 C.

Table 7. Typical Digital Lock Detect Window

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Nominal Value +/-25% (nsec)							
Fastest 00	6.5	8.0	11.0	17	29	53	100	195
01	7.0	8.9	12.8	21	36	68	130	255
10	7.1	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divider Setting Reg07[9:7]	0	1	2	3	4	5	6	7
LD Timer Divider Value	0.5	1	2	4	8	16	32	64

As an example, if we operate in fractional mode at 2.7 GHz with a 50 MHz PD, charge pump gain of 2 mA and a down leakage of 400 uA. Then our average offset at the PD will be 0.4 mA/2 mA = 0.2 of the PD period or about 4 ns (0.2 x 1/50 MHz). However, the fractional modulation of the VCO divider will result in time excursions of the VCO divider output of +/-4Tvco (assuming the internal 8 GHz Divide-by-2 is not enabled. See Reg 8 Bit [19]) from this average value (+/-1.5ns in this example). Hence when in lock, the divided VCO will arrive at the PD about 4 +/-1.5 ns after the divided reference. The Lock Detect window always starts on the arrival of the first signal at the PD, in this case the reference.

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The Lock Detect window must be longer than 4 ns + 1.5 ns (5.5 ns) and shorter than the period of the PD, in this example, 20 ns. A perfect Lock Detect window would be midway between these two values, or 12.75 ns.

Tolerance on the window is +25% at +85 C, -25% at -40 C. Here 12.8 ns nominal window may extend by +25% at +85C to 16 ns, which is fine for a PD period of 20 ns. Also the minimum window may shrink by 25% to 9.6ns at -40C, which again works well for the DC offset of 5.5 ns.

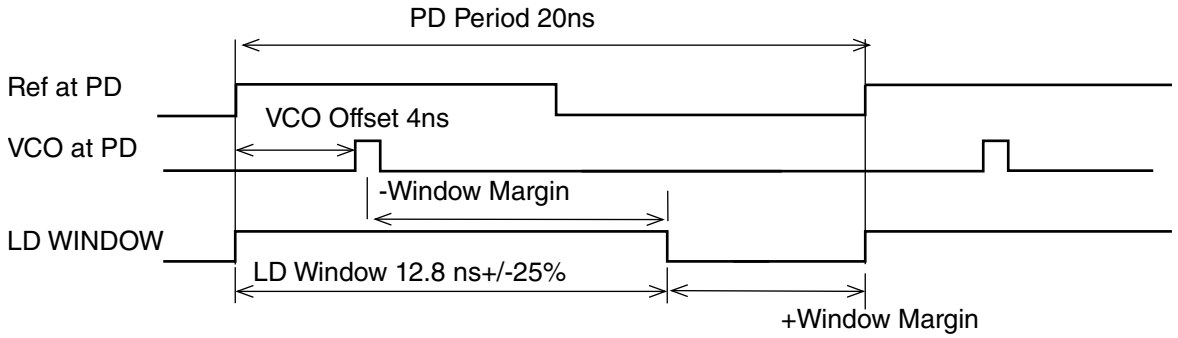

Figure 33. Lock Detect Window Example with 50MHz PD and 4ns VCO Offset

There is always a good solution for the lock detect window for a given operating point. The user should understand however that one solution does not fit all operating points. If charge pump offset or PD frequency are changed significantly then the lock detect window may need to be adjusted.

Cycle Slip Prevention (CSP)

When changing frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than +/-2π radians. Since the gain of the PD varies linearly with phase up to +/-2π, the gain of a conventional PD will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than 0 radians. The output current from the charge pump will cycle from maximum to minimum even though the VCO has not yet reached its final frequency.

The charge on the loop filter small cap may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency actually reverse temporarily during locking. This phenomenon is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle Slipping increases the time to lock to a value much greater than that predicted by normal small signal Laplace analysis.

The PLL PD features an ability to reduce cycle slipping during acquisition. The Cycle Slip Prevention (CSP) feature increases the PD gain during large phase errors. The specific phase error that triggers the momentary increase in PD gain is set via "Reg 0Bh"[8:7].

PD Polarity

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