Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Fractional-N PLL with Integrated VCO 25 MHz to 3000 MHz

Data Sheet **HMC832**

FEATURES

- RF bandwidth:
- 25 MHz to 3000 MHz
- 3.3 V supply
- Maximum phase detector rate: 100 MHz
- Ultralow phase noise
- −110 dBc/Hz in band, typical
- Fractional figure of merit (FOM): −226 dBc/Hz
- 24-bit step size, resolution 3 Hz typical
- Exact frequency mode with 0 Hz frequency error
- Fast frequency hopping
- 40-lead 6 mm × 6 mm SMT package: 36 mm²

APPLICATIONS

- Cellular infrastructure
- Microwave radio
- WiMax, WiFi
- Communications test equipment
- CATV equipment
- DDS replacement
- Military
- Tunable reference source for spurious-free performance

FUNCTIONAL BLOCK DIAGRAM

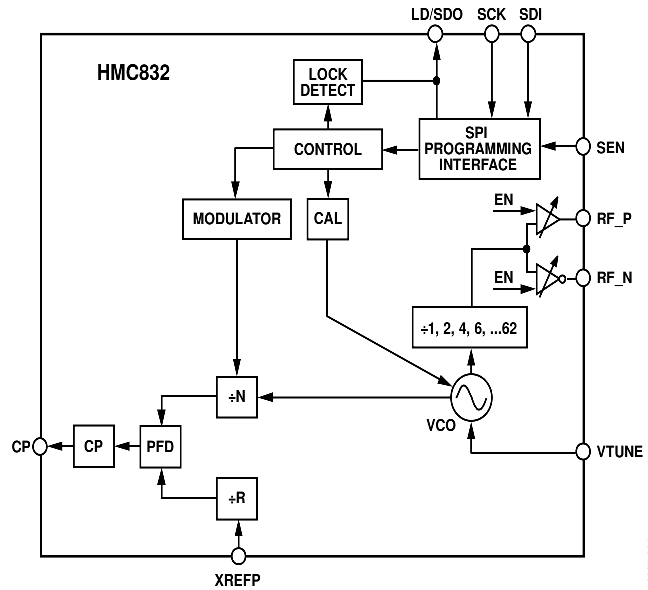

Figure 1.

GENERAL DESCRIPTION

The HMC832 is a 3.3 V, high performance, wideband, fractional-N, phase-locked loop (PLL) that features an integrated voltage controlled oscillator (VCO) with a fundamental frequency of 1500 MHz to 3000 MHz, and an integrated VCO output divider (divide by 1/2/4/6/…60/62), that enables the HMC832 to generate continuous frequencies from 25 MHz to 3000 MHz. The integrated phase detector (PD) and delta-sigma (Δ-Σ) modulator, capable of operating at up to 100 MHz, permit wider loop bandwidths and faster frequency tuning with excellent spectral performance.

Industry leading phase noise and spurious performance, across all frequencies, enable the HMC832 to minimize blocker effects, and to improve receiver sensitivity and transmitter spectral purity. A low noise floor (−160 dBc/Hz) eliminates any contribution to modulator/mixer noise floor in transmitter applications.

The HMC832 is footprint-compatible to the market leading HMC830 PLL with integrated VCO. It features 3.3 V supply and an innovative programmable performance technology that enables the HMC832 to tailor current consumption and corresponding noise floor performance to individual applications by selecting either a low current consumption mode or a high performance mode for an improved noise floor performance.

Additional features of the HMC832 include 12 dB of RF output gain control in 1 dB steps; output mute function to automatically mute the output during frequency changes when the device is not locked; selectable output return loss; programmable differential or single-ended outputs, with the ability to select either output in single-ended mode; and a Δ-Σ modulator exact frequency mode that enables users to generate output frequencies with 0 Hz frequency error.

Rev. A **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

HMC832* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC832LP6GE Evaluation Board

DOCUMENTATION

Application Notes

- Frequency Hopping with Hittite PLLVCOs Application Note
- PLL & PLLVCO Serial Programming Interface Mode Selection Application Note
- Power-Up & Brown-Out Design Considerations for RF PLL +VCO Products Application Note
- Wideband RF PLL+VCO and Clock Generation Products FAQs

Data Sheet

- HMC832 Data Sheet

TOOLS AND SIMULATIONS

- ADIsimFrequency Planner Tool
- ADIsimPLL™

REFERENCE MATERIALS

Quality Documentation

- HMC Legacy PCN: LP6CE and LP6GE QFN - Alternate assembly source
- Package/Assembly Qualification Test Report: LP6, LP6C, LP6G (QTR: 2014-00368)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

Technical Articles

- Hittite Introduces New 3.3V Wideband PLL with Integrated VCO
- Low Cost PLL with Integrated VCO Enables Compact LO Solutions

DESIGN RESOURCES

- HMC832 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC832 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

11/14—Rev. 0 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Updated Format ... Universal
Moved Endnotes from Typical Performance Characteristics Section to the Applications Information Section ... 34
Changes to Ordering Guide ... 48

SPECIFICATIONS

VPPCP, VDDLS, VCC1, VCC2 = 3.3 V; RVDD, AVDD, DVDD, VCCPD, VCCHF, VCCPS = 3.3 V minimum and maximum specified across the temperature range of −40°C to +85°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT CHARACTERISTICS					
Output Frequency		25		3000	MHz
VCO Frequency at PLL Input		1500		3000	MHz
RF Output Frequency at f_{VCO}		1500		3000	MHz
OUTPUT POWER					
RF Output Power at Fundmental Frequency	2000 MHz across all frequencies (see Figure 25)				
	Maximum gain setting: VCO_REG 0x07[3:0] = 11d single-ended		7		dBm
	Gain Setting 6: VCO_REG 0x07[3:0] = 6d differential		2		dBm
Output Power Control Range	1 dB steps		12		dB
HARMONICS FOR FUNDAMENTAL MODE					
fo Mode at 2 GHz	2nd/3rd/4th		−20/−29/−45		dBc
fo/2 Mode at 2 GHz/2 = 1 GHz	2nd/3rd/4th		−26/−10/−34		dBc
fo/30 Mode at 3 GHz/30 = 100 MHz	2nd/3rd/4th		−33/−10/−40		dBc
fo/62 Mode at 1550 MHz/62 = 25 MHz	2nd/3rd/4th		−40/−6/−43		dBc
VCO OUTPUT DIVIDER					
VCO RF Divider Range	1, 2, 4, 6, 8, … 62	1		62	
PLL RF DIVIDER CHARACTERISTICS					
19-Bit N-Divider Range (Integer)	Maximum = $2^{19} - 1$	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (±4) dynamically maximum	20		524,283	
REFERENCE (XREFP PIN) INPUT CHARACTERISTICS					
Maximum XREFP Input Frequency				350	MHz
XREFP Input Level	AC-coupled[1]	−6		+12	dBm
XREFP Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
PHASE DETECTOR (PD)[2]					
PD Frequency Fractional Mode[3]		DC		100	MHz
PD Frequency Integer Mode		DC		100	MHz
CHARGE PUMP					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		μA
PD/Charge Pump SSB Phase Noise	50 MHz reference, input referred				
1 kHz			−143		dBc/Hz
10 kHz	Add 2 dB for fractional mode		−150		dBc/Hz
100 kHz	Add 3 dB for fractional mode		−152		dBc/Hz
LOGIC INPUTS					
V_{SW}		40	50	60	% DVDD
LOGIC OUTPUTS					
Output High Voltage (VOH)			DVDD		V
Output Low Voltage (VOL)			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA
POWER SUPPLY VOLTAGES					
3.3 V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD, VPPCP, VDDLS, VCC1, VCC2	3.1	3.3	3.5	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY CURRENTS					
High Performance Mode	VCO_REG 0x03[1:0] = 3d[4]				
2500 MHz, Gain 11	Gain 11 (VCO_REG 0x07[3:0] = 11d) single-ended output (VCO_REG 0x03[3:2] = 2d)		219		mA
800 MHz, Gain 11	Single-ended output		230		mA
2500 MHz, Gain 6	Gain 6 (VCO_REG 0x07[3:0] = 6d) differential output (VCO_REG 0x03[3:2] = 3d)		226		mA
800 MHz, Gain 6	Differential output		237		mA
2500 MHz, Gain 1	Gain 1 (VCO_REG 0x07[3:0] = 1d) differential output (VCO_REG 0x03[3:2] = 3d)		210		mA
800 MHz, Gain 1	Differential output		221		mA
Low Current Mode	VCO_REG 0x03[1:0] = 1d[4]				
2500 MHz, Gain 6	Gain 6 (VCO_REG 0x07[3:0] = 6d), differential output (VCO_REG 0x03[3:2] = 3d)		195		mA
800 MHz, Gain 6	Differential output		205		mA
2500 MHz, Gain 1	Gain 1 (VCO_REG 0x07[3:0] = 1d), differential output (VCO_REG 0x03[3:2] = 3d)		180		mA
800 MHz, Gain 1	Differential output		192		mA
Power-Down					
Crystal Off	Register 0x01 = 0, crystal not clocked		10		µA
Crystal On, 100 MHz	Register 0x01 = 0, crystal clocked 100 MHz		5		mA
POWER-ON RESET					
Typical Reset Voltage on DVDD			700		mV
Minimum DVDD Voltage for No Reset		1.5			V
Power-On Reset Delay			250		µs
VCO OPEN-LOOP PHASE NOISE					
fo @ 2 GHz[5]					
10 kHz Offset			−88		dBc/Hz
100 kHz Offset			−116		dBc/Hz
1 MHz Offset			−139		dBc/Hz
10 MHz Offset			−157		dBc/Hz
100 MHz Offset			−162		dBc/Hz
fo @ 2 GHz/2 = 1 GHz[5]					
10 kHz Offset			−93		dBc/Hz
100 kHz Offset			−122		dBc/Hz
1 MHz Offset			−145		dBc/Hz
10 MHz Offset			−159		dBc/Hz
100 MHz Offset			−162		dBc/Hz
fo @ 3 GHz/30 = 100 MHz[5]					
10 kHz Offset			−110		dBc/Hz
100 kHz Offset			−139		dBc/Hz
1 MHz Offset			−160		dBc/Hz
10 MHz Offset			−163		dBc/Hz
100 MHz Offset			−163		dBc/Hz
FIGURE OF MERIT (FOM)					
Floor Integer Mode (Figure 24)	Normalized to 1 Hz		−229		dBc/Hz
Floor Fractional Mode (Figure 24)	Normalized to 1 Hz		−226		dBc/Hz
Flicker (Both Modes) (Figure 24)	Normalized to 1 Hz		−268		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCO CHARACTERISTICS					
VCO Tuning Sensitivity					
2800 MHz	Measured with 1.5 V on VTUNE; see Figure 29		24.6		MHz/V
2400 MHz	Measured with 1.5 V on VTUNE; see Figure 29		25.8		MHz/V
2000 MHz	Measured with 1.5 V on VTUNE; see Figure 29		25.2		MHz/V
1600 MHz	Measured with 1.5 V on VTUNE; see Figure 29		24.3		MHz/V
VCO Supply Pushing	Measured with 1.5 V on VTUNE		2.8		MHz/V

[1] Measured with 100 Ω external termination. See Reference Input Stage section for more details.
[2] Slew rate of ≥0.5 ns/V is recommended, see Reference Input Stage section for more details. Frequency is guaranteed across process voltage and temperature from −40°C to +85°C.
[3] This maximum PD frequency can only be achieved if the minimum N value is respected. For example, in the case of fractional mode, the maximum PD frequency = f_{VCO}/20 or 100 MHz, whichever is less.
[4] For detailed current consumption information, refer to Figure 33 and Figure 36.
[5] Gain setting = 6 (VCO_REG 0x07[3:0] = 6d) in high performance mode (VCO_REG 0x03[1:0] = 3d).

TIMING SPECIFICATIONS

SPI Write Timing Characteristics

AVDD = DVDD = 3 V, AGND = DGND = 0 V.

Table 2. SPI Write Timing Characteristics, See Figure 47

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	SDI setup time to SCLK rising edge	3			ns
t_2	SCLK rising edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK 32nd rising edge to SEN rising edge	10			ns
t_6	Recovery time	20			ns
	Maximum serial port clock speed		50		MHz

Table 3. SPI Read Timing Characteristics, See Figure 48

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	SDI setup time to SCK rising edge	3			ns
t_2	SCK rising edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCK rising edge to SDO time		8.2 ns + 0.2 ns/pF		ns
t_6	Recovery time	10			ns
t_7	SCK 32nd rising edge to SEN rising edge	10			ns

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
AVDD, RVDD, DVDD, VCCPD, VCCHF, VCCPS	−0.3 V to +3.6 V
VPPCP, VDDLS, VCC1	−0.3 V to +3.6 V
VCC2	−0.3 V to +3.6 V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature	150°C
Thermal Resistance (θ_{JC}) (Junction to Case (Ground Paddle))	9°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Temperature				
Junction Temperature[1]			125	°C
Ambient Temperature	−40		+85	°C
Supply Voltage				
AVDD, RVDD, DVDD, VCCPD, VCCHF, VCCPS, VPPCP, VDDLS, VCC1, VCC2	3.1	3.3	3.5	V

[1] Layout design guidelines set out in Qualification Test Report are strongly recommended.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

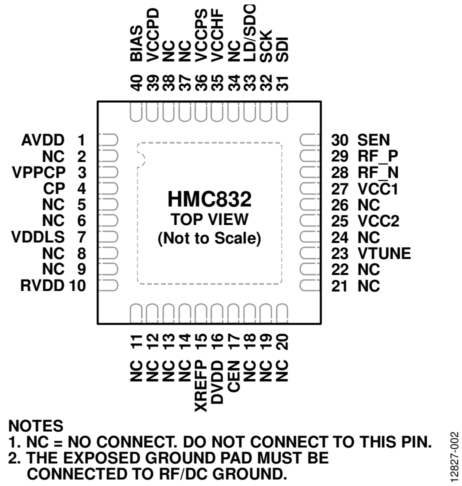

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AVDD	DC Power Supply for Analog Circuitry.
2, 5, 6, 8, 9, 11 to 14, 18 to 22, 24, 26, 34, 37, 38	NC	No Connect. These pins are not connected internally; however, it is recommended to connect these pins to RF/dc ground externally.
3	VPPCP	Power Supply for Charge Pump Analog Section.
4	CP	Charge Pump Output.
7	VDDLS	Power Supply for the Charge Pump Digital Section.
10	RVDD	Reference Supply.
15	XREFP	Reference Oscillator Input.
16	DVDD	DC Power Supply for Digital (CMOS) Circuitry.
17	CEN	PLL Subsystem Enable. Note that there is no effect on the VCO subsystem. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning port input.
25	VCC2	VCO Analog Supply 2.
27	VCC1	VCO Analog Supply 1.
28	RF_N	RF Negative Output.
29	RF_P	RF Positive Output.
30	SEN	PLL Serial Port Enable (CMOS) Logic Input.
31	SDI	PLL Serial Port Data (CMOS) Logic Input.
32	SCK	PLL Serial Port Clock (CMOS) Logic Input.
33	LD/SDO	Lock Detect, or Serial Data, or General-Purpose (CMOS) Logic Output (GPO).
35	VCCHF	DC Power Supply for Analog Circuitry.
36	VCCPS	DC Power Supply for Analog Prescaler.
39	VCCPD	DC Power Supply for Phase Detector.
40	BIAS	External Bypass Decoupling for Precision Bias Circuits. Note: 1.920 V ± 20 mV reference voltage (BIAS) is generated internally and cannot drive an external load. It must be measured with a 10 GΩ meter, such as the Agilent 34410A; a normal 10 MΩ DVM reads erroneously.
	EP	Exposed Pad. The exposed pad must be connected to RF/dc ground.

TYPICAL PERFORMANCE CHARACTERISTICS

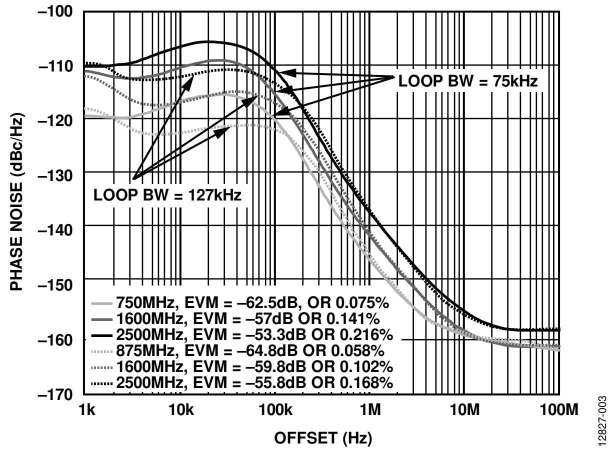

Figure 3. Typical Closed-Loop Integer Phase Noise, 50 MHz PD Frequency, Output Gain = 6 (VCO_REG 0x07[3:0] = 6d), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Phase Noise Integrated from 1 kHz to 100 MHz, See Table 12

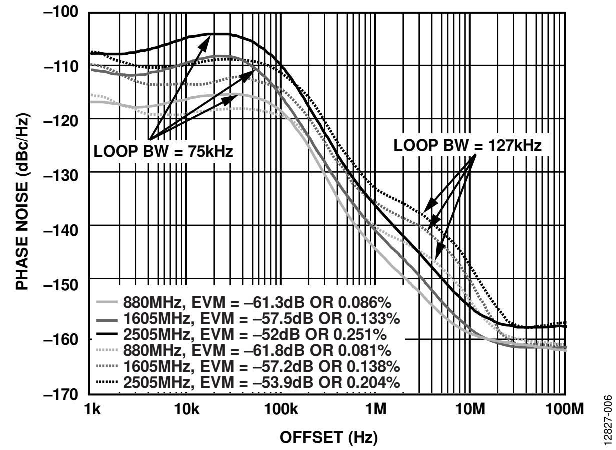

Figure 6. Typical Closed-Loop Fractional Phase Noise, 50 MHz PD Frequency, Output Gain = 6 (VCO_REG 0x07[3:0] = 6d), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Phase Noise Integrated from 1 kHz to 100 MHz, See Table 12

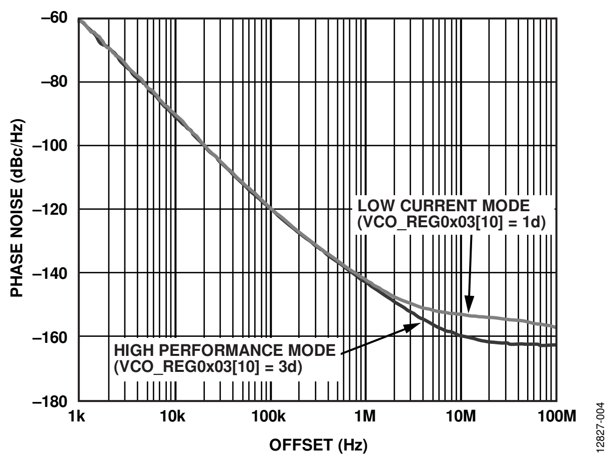

Figure 4. Open-Loop VCO Phase Noise at 1800 MHz

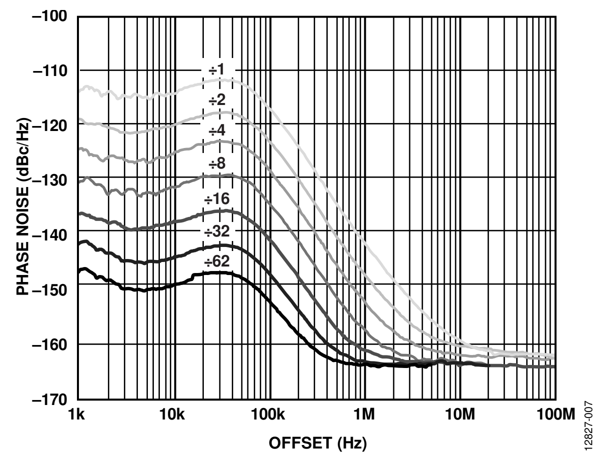

Figure 7. Closed-Loop Phase Noise at 1800 MHz, Divided by 1 to 62, PD Frequency, Loop Filter Bandwidth = 75 kHz (Type 2 from Table 12), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Subset of Available Output Divide Ratios is Shown; Full Range of Output Divide Values Includes 1, 2, 4, 6, 8, … 58, 60, 62

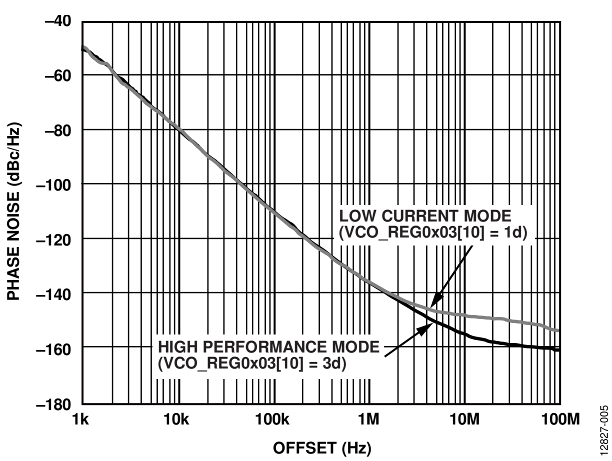

Figure 5. Free Running VCO Phase Noise at 3000 MHz

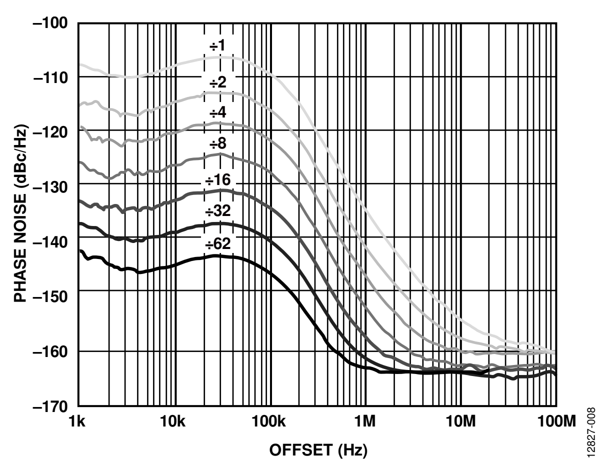

Figure 8. Closed-Loop Phase Noise at 3000 MHz, Divided by 1 to 62, PD Frequency, Loop Filter Bandwidth = 75 kHz (Type 2 from Table 12), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Subset of Available Output Divide Ratios is Shown; Full Range of Output Divide Values Includes 1, 2, 4, 6, 8, … 58, 60, 62

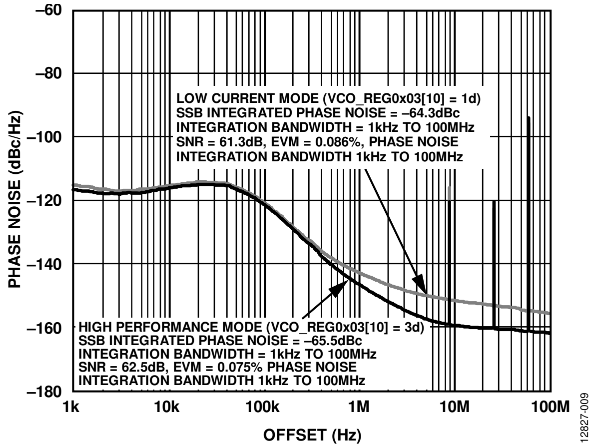

Figure 9. Fractional Spurious Performance at 904 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 200 kHz, Loop Filter Type 2 (See Table 12)

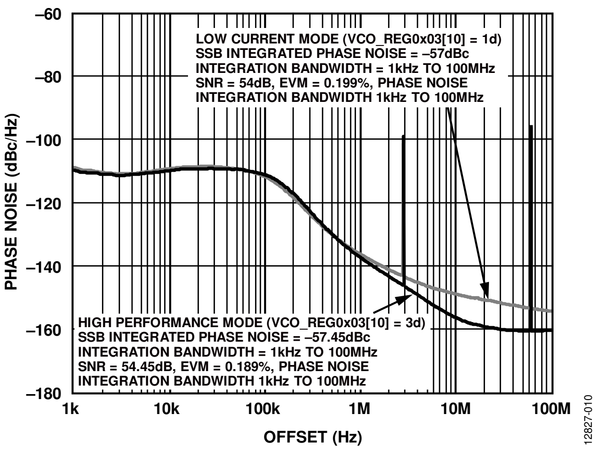

Figure 10. Fractional Spurious Performance at 2118.24 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 240 kHz, Loop Filter Type 2 (See Table 12)

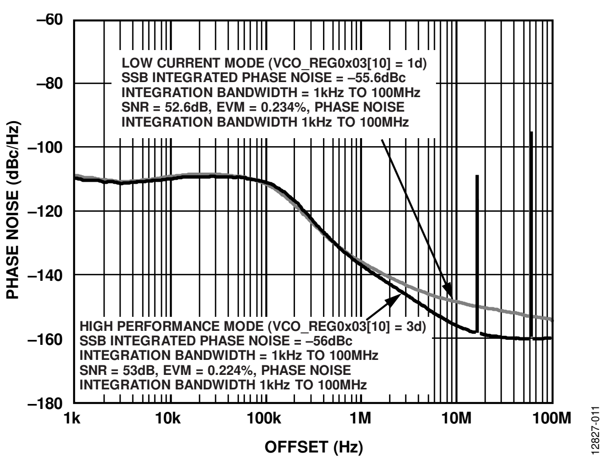

Figure 11. Fractional Spurious Performance at 2646.96 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 240 kHz, Loop Filter Type 2 (See Table 12)

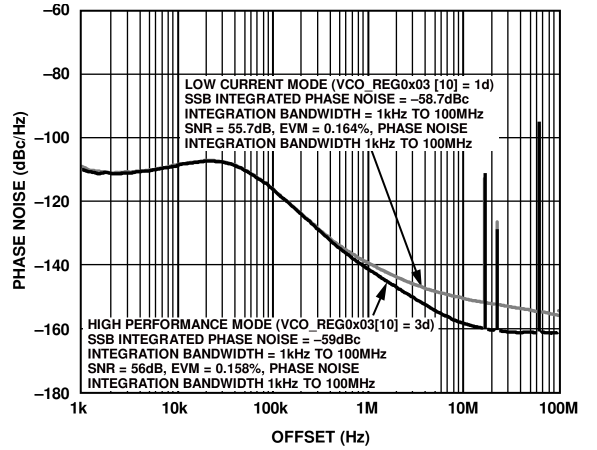

Figure 12. Fractional Spurious Performance at 1804 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 200 kHz, Loop Filter Type 2 (See Table 12)

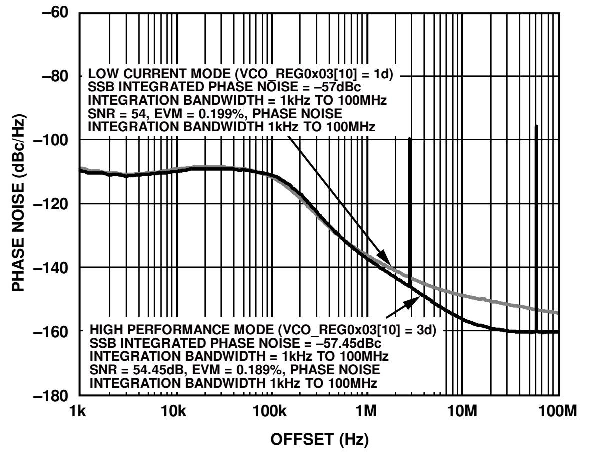

Figure 13. Fractional Spurious Performance at 2118.24 MHz, Identical Configuration to Figure 10 with Exact Frequency Mode Off

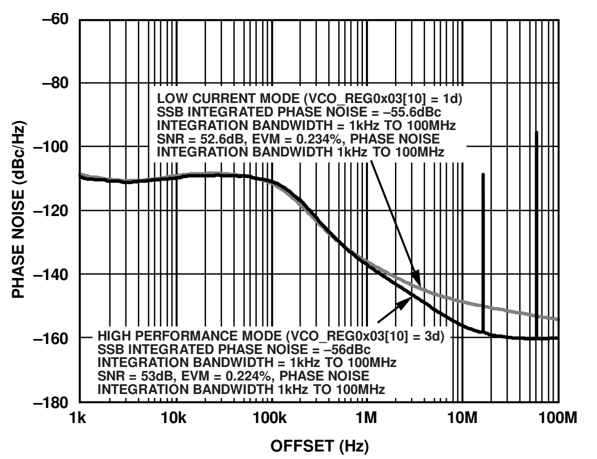

Figure 14. Fractional Spurious Performance at 2646.96 MHz, Identical Configuration to Figure 11 with Exact Frequency Mode Off

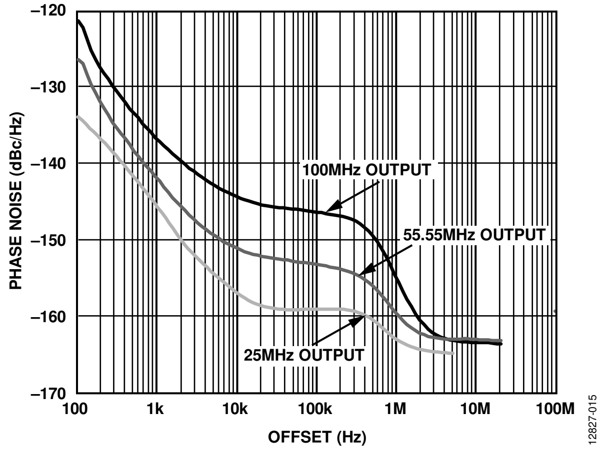

Figure 15. Low Frequency Performance, 100 MHz XTAL, PD Frequency = 50 MHz, Loop Filter Type 3 (See Table 12), Integer Mode, 50 MHz Low-Pass Filter at the Output of HMC832 for the 25 MHz Curve Only, Charge Pump Set to Maximum Value

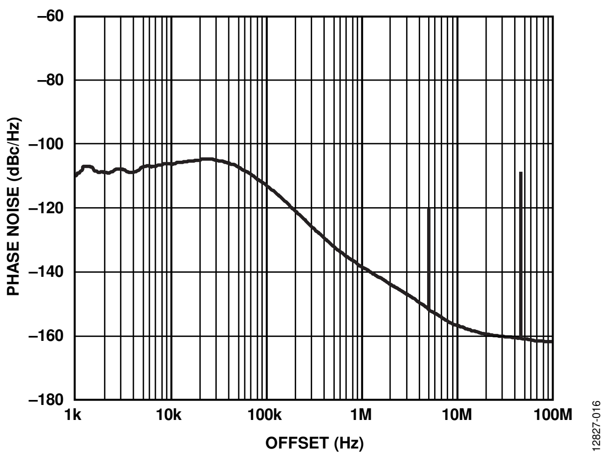

Figure 16. Typical Spurious Emissions at 2000.1 MHz, Tunable Reference, Loop Filter Type 2 (see Table 12 and the Loop Filter and Frequency Changes Section)

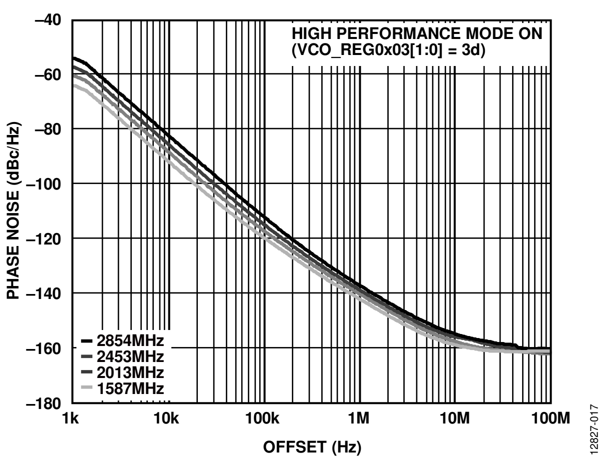

Figure 17. Open-Loop Phase Noise

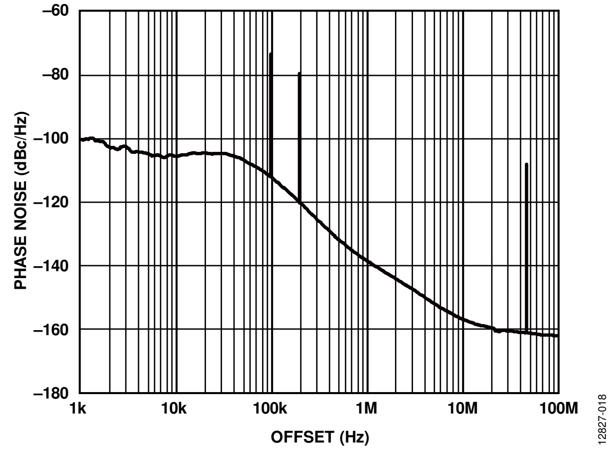

Figure 18. Typical Spurious Emissions at 2000.1 MHz, 50 MHz Fixed Reference, 50 MHz PD Frequency, Integer Boundary Spur Inside the Loop Filter Bandwidth (See the Loop Filter and Frequency Changes Section)

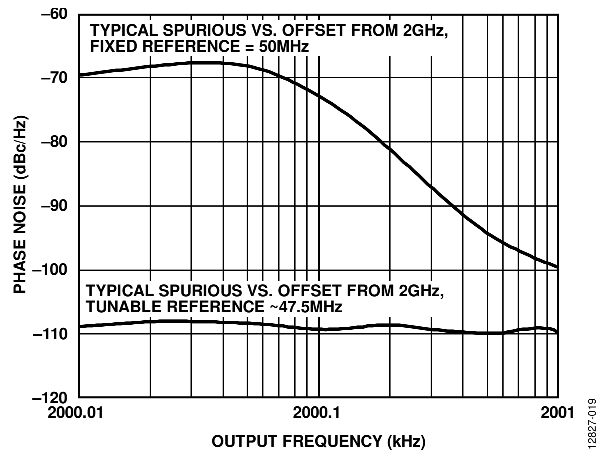

Figure 19. Typical Spurious vs. Offset from 2 GHz, Fixed 50 MHz Reference vs. Tunable 47.5 MHz Reference (See the Loop Filter and Frequency Changes Section)

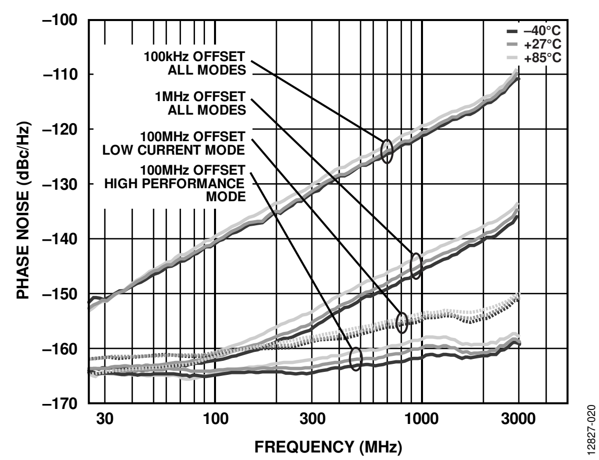

Figure 20. Open-Loop Phase Noise vs. Frequency at Various Temperatures

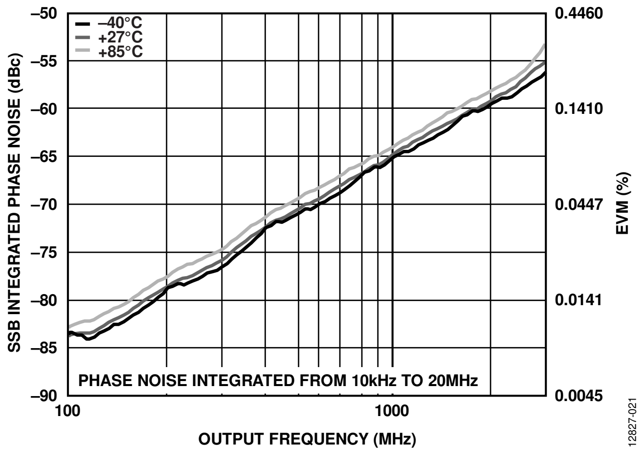

Figure 21. Single Sideband Integrated Phase Noise, High Performance Mode, Loop Filter Type 2 (See Table 12)

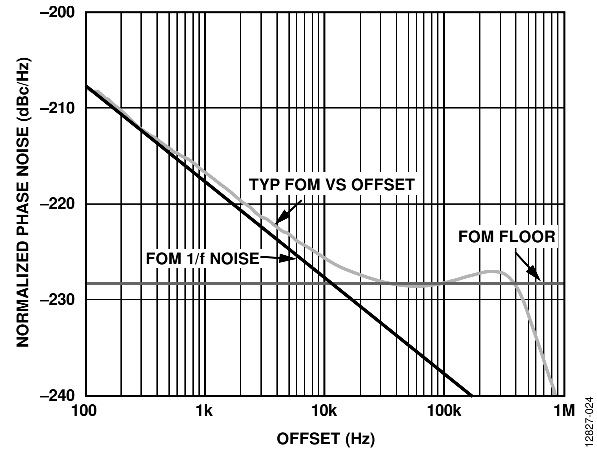

Figure 24. Figure of Merit

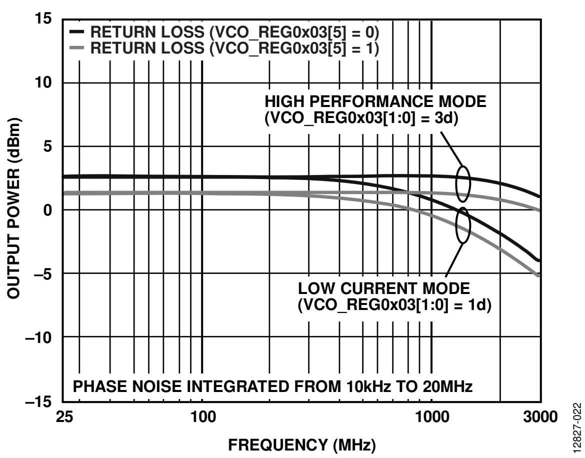

Figure 22. Typical Single-Ended Output Power vs. Frequency (Mid Gain Setting 6)

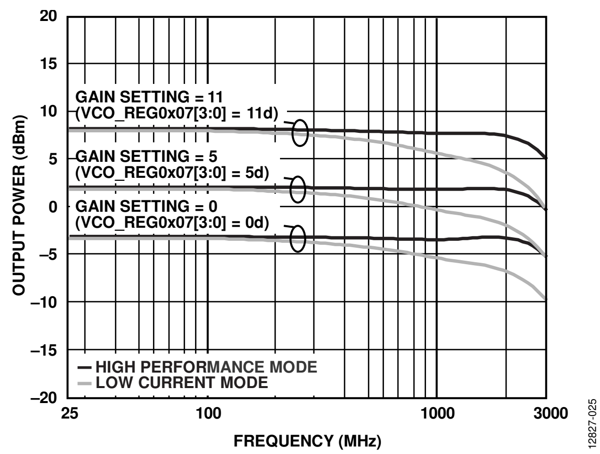

Figure 25. Typical Output Power vs. Frequency and Gain (Single-Ended)

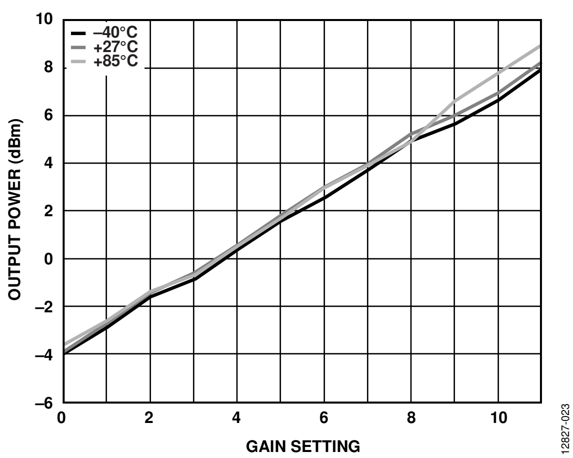

Figure 23. Typical RF Output Power at 2 GHz (Single-Ended) vs. Temperature

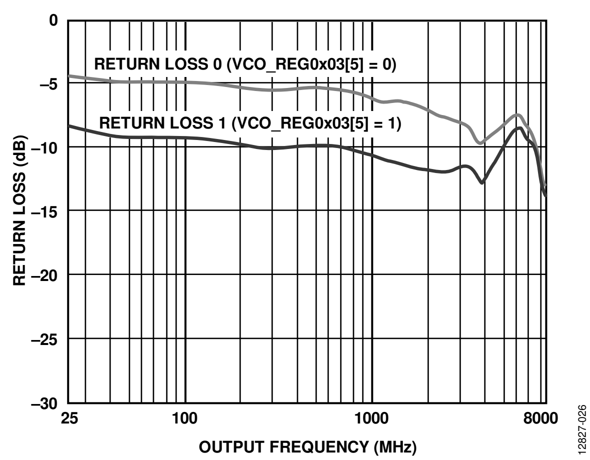

Figure 26. RF Output Return Loss

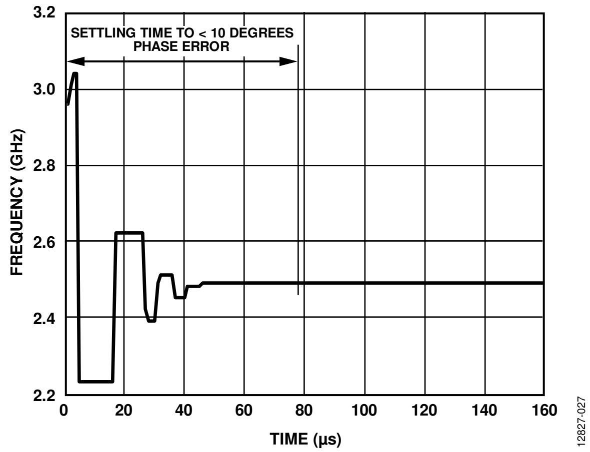

Figure 27. Frequency Settling After Frequency Change, Autocalibration Enabled, Loop Filter BW = 127 kHz (Type 1, See Table 12)

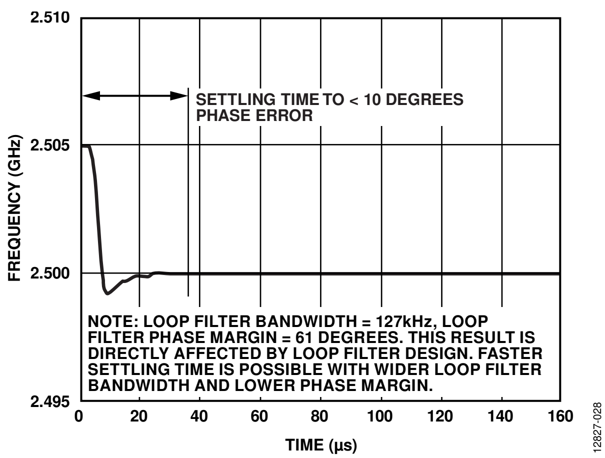

Figure 28. Frequency Settling After Frequency Change, Manual Calibration, Loop Filter BW = 127 kHz (Type 1 in Table 12)

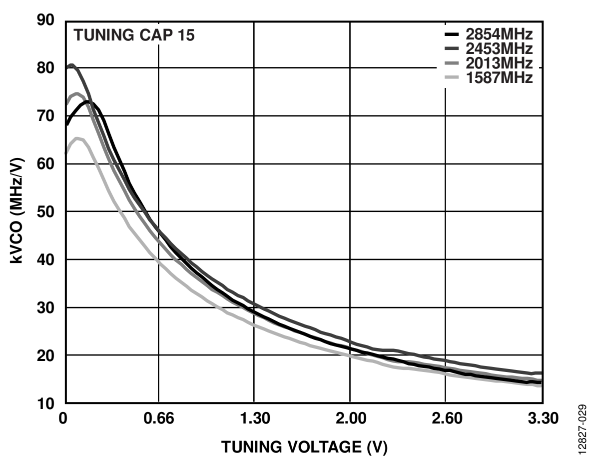

Figure 29. Typical VCO Sensitivity

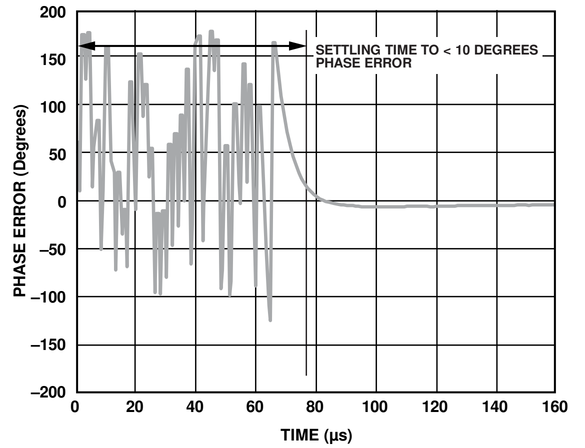

Figure 30. Phase Settling After Frequency Change, Autocalibration Enabled Loop Filter BW = 127 kHz (Type 1, See Table 12)

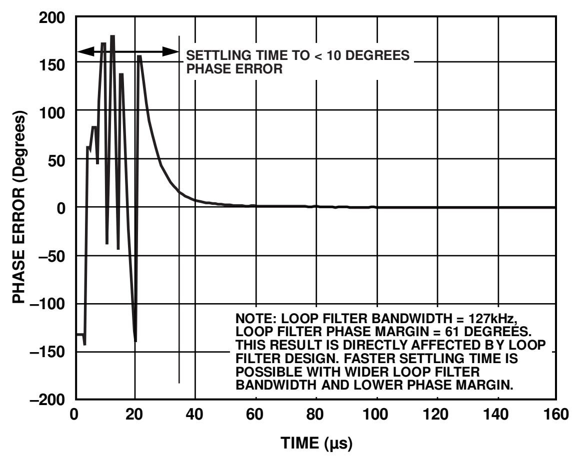

Figure 31. Phase Settling After Frequency Change, Manual Calibration

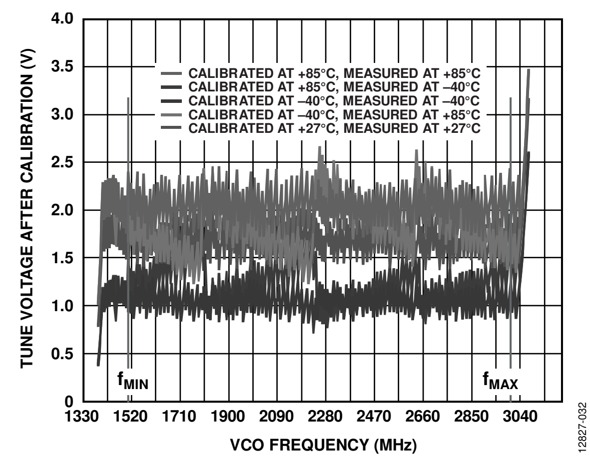

Figure 32. Typical Tuning Voltage After Calibration (See the Loop Filter and Frequency Changes Section)

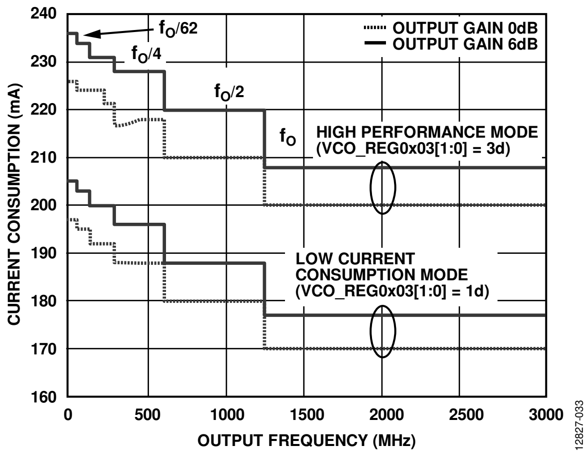

Figure 33. Current Consumption in Single-Ended Output Configuration, Output Gain Configured in VCO_REG 0x07[3:0], Differential or Single-Ended Mode Programmed in VCO_REG 0x03[3:2]

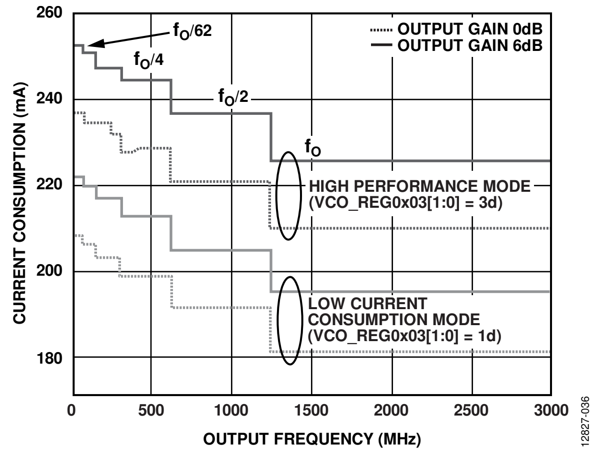

Figure 36. Current Consumption in Differential Output Configuration, Output Gain Configured in VCO_REG 0x07[3:0], Differential or Single-Ended Mode Programmed in VCO_REG 0x03[3:2]

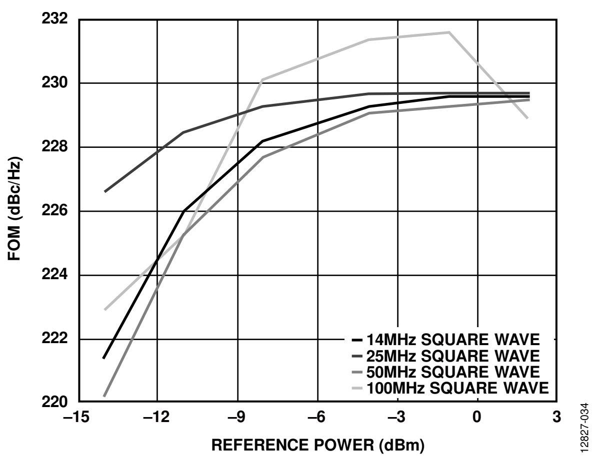

Figure 34. Reference Input Sensitivity, Square Wave, Measured from a 50 Ω Source with a 100 Ω External Resistor Termination

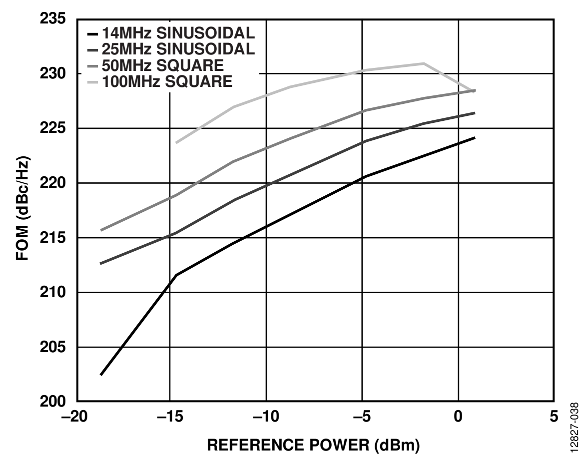

Figure 37. Reference Input Sensitivity, Sinusoidal Wave, Measured from a 50 Ω Source with a 100 Ω External Resistor Termination

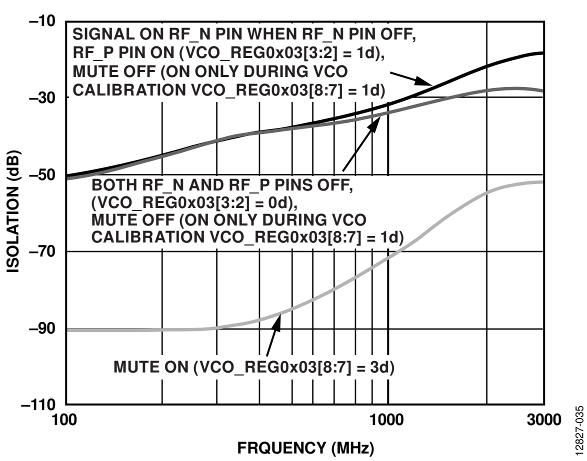

Figure 35. Mute Mode Isolation, Measured at Output

THEORY OF OPERATION

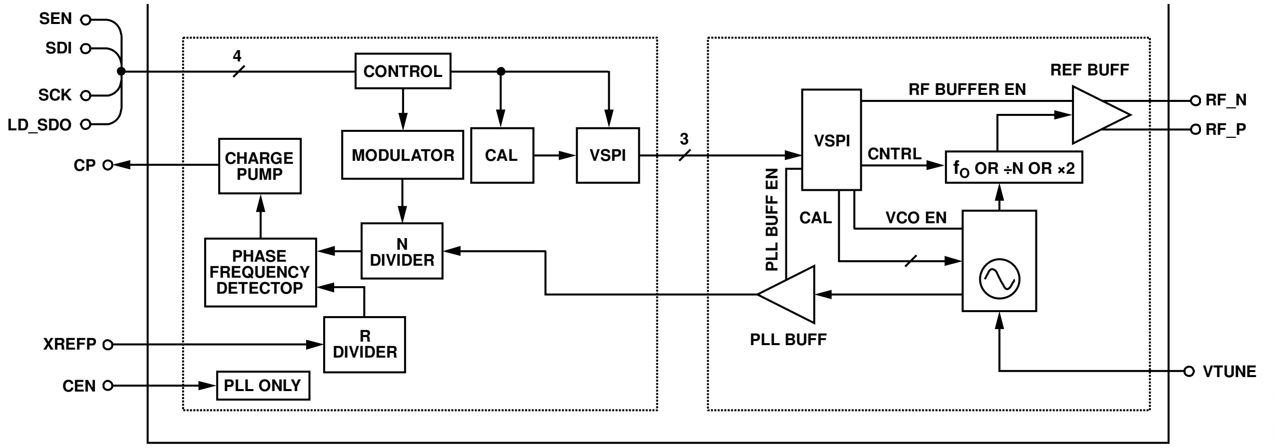

Figure 38. PLL and VCO Subsystems

The HMC832 PLL with integrated VCO is comprised of two subsystems; PLL subsystem and VCO subsystem, as shown in Figure 38.

PLL SUBSYSTEM OVERVIEW

The PLL subsystem divides down the VCO output to the desired comparison frequency via the N-divider (integer value set in Register 0x03, fractional value set in Register 0x04), compares the divided VCO signal to the divided reference signal (reference divider set in Register 0x02) in the phase detector (PD), and drives the VCO tuning voltage via the charge pump (CP) (configured in Register 0x09) to the VCO subsystem. Some of the additional PLL subsystem functions include

- Delta-sigma configuration (Register 0x06).
- Exact frequency mode (configured in Register 0x0C, Register 0x03, and Register 0x04).
- Lock detect (LD) configuration (use Register 0x07 to configure LD and Register 0x0F to configure the LD_SDO output pin).
- External CEN pin used for the hardware PLL enable pin. CEN pin does not affect the VCO subsystem.

Typically, only writes to the divider registers (integer part uses Register 0x03, fractional part uses Register 0x04) of the PLL subsystem are required for HMC832 output frequency changes.

Divider registers of the PLL subsystem (Register 0x03 and Register 0x04), set the fundamental frequency (1500 MHz to 3000 MHz) of the VCO subsystem. Output frequencies ranging from 25 MHz to 1500 MHz are generated by tuning to the appropriate fundamental VCO frequency (1500 MHz to 3000 MHz) by programming the N divider (Register 0x03 and Register 0x04) and programming the output divider (divide by 1/2/4/6 … /60/62, in VCO_REG 0x02) in the VCO subsystem.

For detailed frequency tuning information and example, see the Frequency Tuning section.

VCO SUBSYSTEM OVERVIEW

The VCO subsystem consists of a capacitor switched step tuned VCO and an output stage. In typical operation, the VCO subsystem is programmed with the appropriate capacitor switch setting that is executed automatically by the PLL subsystem autocalibration state machine when autocalibration is enabled (Register 0x0A[11] = 0, see the VCO Calibration section for more information). The VCO tunes to the fundamental frequency (1500 MHz to 3000 MHz), and is locked by the CP output from the PLL subsystem. The VCO subsystem controls the output stage of the HMC832 enabling configuration of

- User defined performance settings (see the Programmable Performance Technology section) that are configured via VCO_REG 0x03[1:0].
- VCO output divider settings that are configured in the VCO_REG 0x02 (divide by 2/4/6 … 60/62 to generate frequencies from 25 MHz to 1500 MHz, or divide by 1 to generate fundamental frequencies between 1500 MHz and 3000 MHz).
- Output gain settings (VCO_REG 0x07[3:0]).
- Output return loss setting (VCO_REG 0x03[5]). See Figure 26 for more information.
- Single-ended or differential output operation (VCO_REG 0x03[3:2]).
- Mute (VCO_REG 0x03[8:7]).

SPI (SERIAL PORT INTERFACE) CONFIGURATION OF PLL AND VCO SUBSYSTEMS

The two subsystems (PLL subsystem and VCO subsystem) have their own register maps as shown in the PLL Register Map and VCO Subsystem Register Map sections. Typically, writes to both register maps are required for initialization and frequency tuning operations.

As shown in Figure 38, the PLL subsystem is connected directly to the SPI of the HMC832, whereas the VCO subsystem is connected indirectly through the PLL subsystem to the

HMC832 SPI. As a result, writes to the PLL Register Map are written directly and immediately, whereas the writes to the VCO Subsystem Register Map are written to the PLL subsystem Register 0x05 and forwarded via the internal VCO SPI (VSPI) to the VCO subsystem. This is a form of indirect addressing.

Note that VCO subsystem registers are write only and cannot be read. More information is available in the VCO Serial Port Interface (VSPI) section.

VCO Serial Port Interface (VSPI)

The HMC832 communicates with the internal VCO subsystem via an internal 16-bit VCO SPI. The internal serial port controls the step tuned VCO and other VCO subsystem functions.

Note that the internal VCO subsystem SPI (VSPI) runs at the rate of the autocalibration FSM clock, t_{FSM}, (see the VCO Autocalibration section) where the FSM clock frequency cannot be greater than 50 MHz. The VSPI clock rate is set by Register 0x0A[14:13].

Writes to the control registers of the VCO are handled indirectly via writes to Register 0x05 of the HMC832. A write to HMC832 Register 0x05 causes the internal PLL subsystem to forward the packet, MSB first, across its internal serial link to the VCO subsystem, where it is interpreted.

VSPI Use of Register 0x05

The packet data written into Register 0x05 is subparsed by logic at the VCO subsystem into the following three fields:

Field 1—Bits[2:0]: 3-bit VCO_ID, target subsystem address = 000b.

Field 2—Bits[6:3]: 4-bit VCO_REGADDR, the internal register address inside the VCO subsystem.

Field 3—Bits[15:7]: 9-bit VCO_DATA, data field to write to the VCO register.

For example, to write 0_1111_1110 into Register 2 of the VCO subsystem (VCO_ID = 000b), and set the VCO output divider to divide by 62, the following needs to be written to Register 0x05 = 0_1111_1110b, 0010b, 000b or equivalently, Register 0x05 = 7F10.

During autocalibration, the autocalibration controller writes into the VCO register address specified by the VCO_ID and VCO_REGADDR, as stored in Register 0x05[2:0] and Register 0x05[6:3], respectively. Autocalibration requires that these values be zero (Register 0x05[6:0] = 0); otherwise, when they are not zero (Register 0x05[6:0] ≠ 0), autocalibration does not function.

To ensure that the autocalibration functions, it is critical to write Register 0x05[6:0] = 0 after the last VCO subsystem write prior to an output frequency change triggered by a write to either Register 0x03 or Register 0x04.

However, it is impossible to write only Register 0x05[6:0] = 0 (VCO_REGADDR) without writing Register 0x05[15:7] (VCO_DATA). Therefore, to ensure that the VCO_DATA (Register 0x05[15:7]) in VCO_REGADDR 0x00 is not changed, it is required to read the switch settings provided in Register 0x10[7:0], and then rewrite them to Register 0x05[15:7], as shown in the following example:

1. Read Register 0x10
2. Write to Register 0x05 the following:
    a. Register 0x05[15:14] = Register 0x10[7:6]
    b. Register 0x05[13] = 1, reserved bit
    c. Register 0x05[12:8] = Register 0x10[4:0]
    d. Register 0x05[7:0] = 0

Changing the VCO subsystem configuration (VCO Subsystem Register Map section) without following this procedure results in a failure to lock to the desired frequency.

For applications not using the read functionality of the HMC832 SPI, in which Register 0x10 cannot be read, it is possible to write Register 0x05 = 0x0 to set Register 0x05[6:0] = 0, which also sets the VCO subband setting equal to zero (Register 0x05[15:7] = 0), effectively programming incorrect VCO subband settings and causing the HMC832 to lose lock. This procedure is then immediately followed by a write to:

- Register 0x03, if in integer mode.
- Register 0x04, if in fractional mode.

This write effectively retriggers the autocalibration state machine, forcing the HMC832 to relock whether in integer or fractional mode.

This procedure causes the HMC832 to lose lock and relock after every VCO subsystem change. Typical output frequency and lock time is shown in Figure 27 and Figure 30, and is typically in the order of 100 µs for a phase settling of 10°, and is also dependent on loop filter design (loop filter bandwidth and loop filter phase margin).

VCO SUBSYSTEM

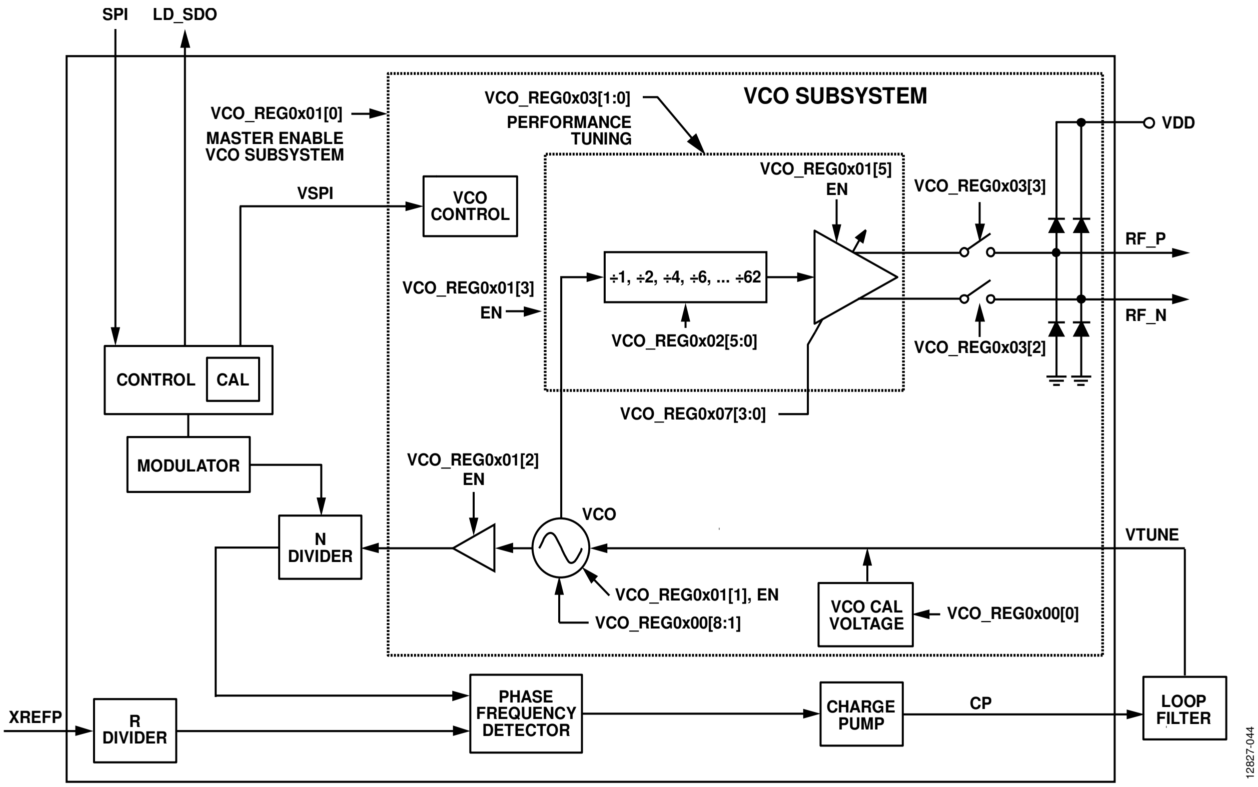

Figure 39. PLL and VCO Subsystems

The HMC832 contains a VCO subsystem that can be configured to operate in:

- Fundamental frequency (fo) mode (1500 MHz to 3000 MHz).
- Divide by N mode, where N = 2, 4, 6, 8 … 58, 60, 62 (25 MHz to 1500 MHz).

All modes are VCO register programmable, as shown in Figure 39. One loop filter design can be used for the entire frequency of operation of the HMC832.

VCO Calibration

VCO Autocalibration

The HMC832 uses a step tuned type VCO. A simplified step tuned VCO is shown in Figure 41. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or stepped by switching in and out of the VCO tank capacitors. Note that more than one capacitor can be switched in at a time.

A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid voltage tuning point of the HMC832 charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (k_{VCO}).

The VCO switches are normally controlled automatically by the HMC832 using the autocalibration feature. The autocalibration feature is implemented in the internal state machine. It manages the selection of the VCO subband (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via Register 0x05 for testing or for other special purpose operations. Other control bits specific to the VCO are also sent via Register 0x05.

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC832 knows which switch position on the VCO is optimum for the desired output frequency. The HMC832 supports autocalibration of the step tuned VCO. The autocalibration fixes the VCO tuning voltage at the optimum midpoint of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the desired phase-locked frequency. This procedure results in a phase-locked oscillator that locks over a narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 40. Note that the tuning voltage stays in a narrow range over a wide range of output frequencies.

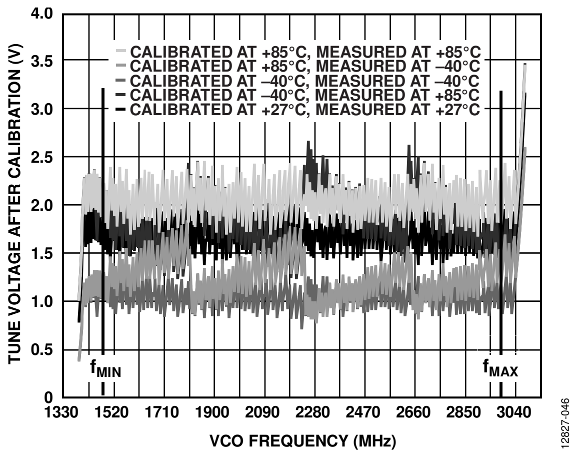

Figure 40. Typical VCO Tuning Voltage After Calibration

The calibration is normally run automatically, once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally need to be concerned about which switch setting is used for a given frequency because this is handled by the autocalibration routine.

The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency and ensures that the VCO stays locked and performs well over its full temperature range without additional calibration, regardless of the temperature at which the VCO was calibrated.

Autocalibration can also be disabled, thereby allowing manual VCO tuning. Refer to the Manual VCO Calibration for Fast Frequency Hopping section for a description of manual tuning.

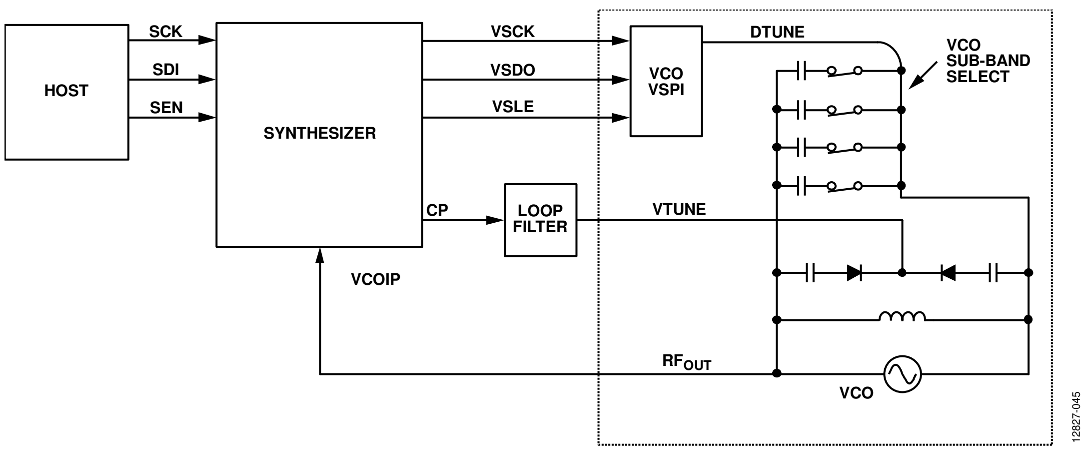

Figure 41. Simplified Step Tuned VCO

Autocalibration Using Register 0x05

Autocalibration transfers switch control data to the VCO subsystem via Register 0x05. The address of the VCO subsystem in Register 0x05 is not altered by the autocalibration routine. The address and ID of the VCO subsystem in Register 0x05 must be set to the correct value before autocalibration is executed. For more information see the VCO Serial Port Interface (VSPI) section.

Automatic Relock on Lock Detect Failure

It is possible by setting Register 0x07[13] to have the VCO subsystem automatically rerun the calibration routine and relock itself if lock detect indicates an unlocked condition for any reason. With this option the system attempts to relock only once.

VCO Autocalibration on Frequency Change

Assuming Register 0x0A[11] = 0, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the autocalibration routine for any reason at the same frequency, rewrite the frequency change with the same value and the autocalibration routine executes again without changing the final frequency.

VCO Autocalibration Time and Accuracy

The VCO frequency is counted for t_{MMT}, the period of a single autocalibration measurement cycle.

$$t_{MMT} = t_{XTAL} \times R \times 2^n \quad (1)$$

where:
n is set by Register 0x0A[2:0] and results in measurement periods which are multiples of the PD period, $t_{XTAL}R$.
R is the reference path division ratio currently in use, Register 0x02.
t_{XTAL} is the period of the external reference (crystal) oscillator.

The VCO autocalibration counter, on average, expects to register N counts, rounded down (floor) to the nearest integer, for every PD cycle.

N is the ratio of the target VCO frequency, f_{VCO}, to the frequency of the PD, f_{PD}, where N can be any rational number supported by the N divider.

N is set by the integer (N_{INT} = Register 0x03) and fractional (N_{FRAC} = Register 0x04) register contents by Equation 2.

$$N = N_{INT} + N_{FRAC}/2^{24} \quad (2)$$

The autocalibration state machine and the data transfers to the internal VCO subsystem SPI (VSPI) run at the rate of the FSM clock, t_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$t_{FSM} = t_{XTAL} \times 2^m \quad (3)$$

where m is 0, 2, 4, or 5 as determined by Register 0x0A[14:13].

The expected number of VCO counts, V, is given by

$$V = floor\,(N \times 2^n) \quad (4)$$

The nominal VCO frequency measured, f_{VCOM}, is given by

$$f_{VCOM} = V \times f_{XTAL}/(2^n \times R) \quad (5)$$

where the worst case measurement error, f_{ERR} , is

$$f_{ERR} \approx \pm f_{PD}/2^{n+1} \quad (6)$$

A 5-bit step tuned VCO, for example, nominally requires five measurements for calibration or in the worst case, six measurements, and hence, seven VSPI data transfers of 20 clock cycles each. The measurement has a programmable number of wait states, k, of 128 FSM cycles defined by Register 0x0A[7:6] = k. Total calibration time, worst case, is given by

$$t_{CAL} = k128\, t_{FSM} + 6t_{PD}\, 2^n + 7 \times 20\, t_{FSM} \quad (7)$$

or equivalently

$$t_{CAL} = t_{XTAL}\,(6R \times 2^n + (140+(k \times 128)) \times 2^m) \quad (8)$$

For guaranteed hold of lock, across temperature extremes, the resolution should be better than 1/8th the frequency step caused by a VCO subband switch change. Better resolution settings show no improvement.

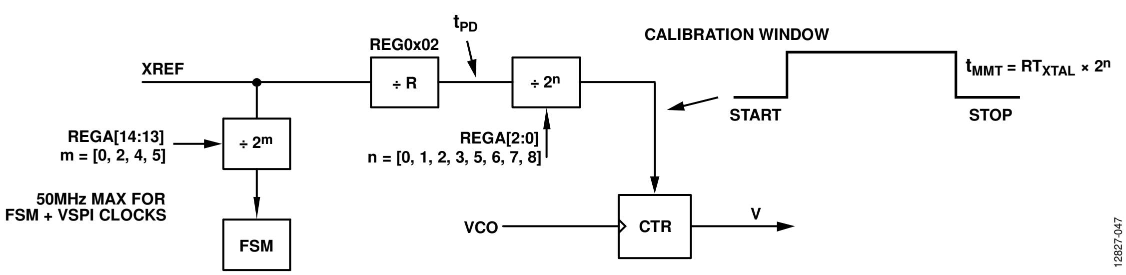

Figure 42. VCO Calibration

Table 7. Autocalibration Example with f_{XTAL} = 50 MHz, R = 1, m = 0

Control Value Register 0x0A[2:0]	n	2^n	t_{MMT} (µs)	t_{CAL} (µs)	f_{ERR} Maximum
0	0	1	0.02	4.92	±25 MHz
1	1	2	0.04	5.04	±12.5 MHz
2	2	4	0.08	5.28	±6.25 MHz
3	3	8	0.16	5.76	±3.125 MHz
4	5	32	0.64	8.64	±781 kHz

Control Value Register 0x0A[2:0]	n	2^n	t_{MMT} (µs)	t_{CAL} (µs)	f_{ERR} Maximum
5	6	64	1.28	12.48	±390 kHz
6	7	128	2.56	20.16	± 95 kHz
7	8	256	5.12	35.52	±98 kHz

VCO Autocalibration Example

The VCO subsystem must satisfy the maximum f_{PD} limited by the two following conditions:

$N \geq 16$ (f_{INT}), $N \geq 20.0$ (f_{FRAC})

where $N = f_{VCO}/ f_{PD}$.

$f_{PD} \leq 100$ MHz

For example, if the VCO subsystem output frequency is to operate at 2.01 GHz and the crystal frequency is f_{XTAL} = 50 MHz, R = 1, and m = 0 (see Figure 42), then t_{FSM} = 20 ns (50 MHz).

Note that when using autocalibration, the maximum autocalibration finite state machine (FSM) clock cannot exceed 50 MHz (see Register 0x0A[14:13]). The FSM clock does not affect the accuracy of the measurement, it only affects the time to produce the result. This same clock is used to clock the 16-bit VCO serial port.

If time to change frequencies is not a concern, then the calibration time for maximum accuracy can be set, and therefore, the measurement resolution is of no concern.

Using an input crystal of 50 MHz (R = 1 and f_{PD} = 50 MHz) the times and accuracies for calibration using Equation 6 and Equation 8 are listed in Table 7, where minimal tuning time is 1/8th of the VCO band spacing.

Across all VCOs, a measurement resolution better than 800 kHz produces correct results. Setting m = 0 and n = 5, provides 781 kHz of resolution and adds 8.6 µs of autocalibration time to a normal frequency hop. After the autocalibration sets the final switch value, 8.64 µs after the frequency change command, the fractional register is loaded, and the loop locks with a normal transient predicted by the loop dynamics. Therefore, as shown in this example, autocalibration typically adds about 8.6 µs to the normal time to achieve frequency lock. Use autocalibration for all but the most extreme frequency hopping requirements.

Manual VCO Calibration for Fast Frequency Hopping

When switching frequencies quickly is needed, it is possible to eliminate the autocalibration time by calibrating the VCO in advance and storing the switch number vs. frequency information in the host. This is accomplished by initially locking the HMC832 on each desired frequency using autocalibration, then reading and storing the selected VCO switch settings. The VCO switch settings are available in Register 0x10[7:0] after every autocalibration operation. The host must then program the VCO switch settings directly when changing frequencies.

Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when autocalibration is disabled. Therefore, frequency changes with manual control and autocalibration disabled requires a minimum of two serial port transfers to the PLL, once to set the VCO switches and once to set the PLL frequency.

When autocalibration is disabled, Register 0x0A[11] = 1, the VCO updates its registers immediately with the value written via Register 0x05. The VCO internal transfer requires 16 VSCK clock cycles after the completion of a write to Register 0x05. VSCK and the autocalibration controller clock are equal to the input reference divided by 0, 4, 16, or 32 as controlled by Register 0x0A[14:13].

Registers Required for Frequency Changes in Fractional Mode

In fractional mode (Register 0x06[11] = 1), a large change of frequency may require main serial port writes to one of the three following registers

- The integer register, INTG, Register 0x03. This is required only if the integer part changes.
- The VCO SPI register, Register 0x05. This is required only for manual control of VCO if Register 0x0A[11] = 1, autocalibration is disabled, or to change the VCO output divider value (VCO_REG 0x02), see Figure 39 for more information.
- The fractional register, Register 0x04. The fractional register write triggers autocalibration when Register 0x0A[11] = 0, and it is loaded into the modulator automatically after the autocalibration runs. If autocalibration is disabled, Register 0x0A[11] = 1, the fractional frequency change is loaded immediately into the modulator when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with autocalibration enabled (Register 0x0A[11] = 0), usually require only a single write to the fractional register. In a worst-case scenario, three main serial port transfers to the HMC832 could be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, then the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register, Register 0x04, for frequency changes.

Registers Required for Frequency Changes in Integer Mode

In integer mode (Register 0x06[11] = 0), a change of frequency requires main serial port writes to the following registers:

- VCO SPI register, Register 0x05. This is required for manual control only of the VCO when Register 0x0A[11] = 1 (autocalibration disabled) or when the VCO output divider value must change (VCO_REG 0x02).
- Integer register, Register 0x03. In integer mode, an integer register write triggers autocalibration when Register 0x0A[11] = 0 and it is loaded into the prescaler automatically after autocalibration runs. If autocalibration is disabled, Register 0x0A[11] = 1, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally, changes to the integer register cause large steps in the VCO frequency; therefore, the VCO switch settings must be adjusted. Autocalibration enabled is the recommended method for integer mode frequency changes. If autocalibration is disabled (Register 0x0A[11] = 1), a priori knowledge of the correct VCO switch setting and the corresponding adjustment to the VCO is required before executing the integer frequency change.

VCO Output Mute Function

The HMC832 features an intelligent output mute function with the capability to disable the VCO output while maintaining fully functional PLL and VCO subsystems. The mute function is automatically controlled by the HMC832 and provides a number of mute control options including

- Automatic mute. This option automatically mutes the outputs during VCO calibration during output frequency changes. This mode can be useful in eliminating any out of band emissions during frequency changes, and ensuring that the system emits only the desired frequencies. It is enabled by writing VCO_REG 0x03[8:7] = 1d.
- Always mute (VCO_REG 0x03[8:7] = 3d). This mode is used for manual mute control.

Typical isolation when the HMC832 is muted is always better than 50 dB, and is ~40 dB better than disabling the individual outputs of the HMC832 via VCO_REG 0x03[3:2], as shown in Figure 35.

Also note that the VCO subsystem registers are not directly accessible. They are written to the VCO subsystem via PLL Register 0x05. See Figure 39 and the VCO Serial Port Interface (VSPI) section for more information about the VCO subsystem SPI.

VCO Built-In Test (BIST) with Autocalibration

The frequency limits of the VCO can be measured using the BIST features of the autocalibration machine by setting Register 0x0A[10] = 1, which freezes the VCO switches in one position. VCO switches may then be written manually with the varactor biased at the nominal midrail voltage used for autocalibration. For example, to measure the VCO maximum frequency use Switch 0, written to the VCO subsystem via Register 0x05 = 000000001 0000 VCO_ID, where VCO_ID = 000b.

When autocalibration is enabled (Register 0x0A[11] = 0), and a new frequency is written, autocalibration runs. The VCO frequency error relative to the command frequency is measured and the results are written to Register 0x11[19:0], where Register 0x11[19] is the sign bit. The result is written in terms of VCO count error (see Equation 4).

For example, if the expected VCO is 2 GHz, the reference is 50 MHz, and n is 6, expect to measure $2000/(50/2^6) = 2560$ counts. If a difference of −5 counts is measured in Register 0x11, then it means 2555 counts were actually measured. Hence, the actual frequency of the VCO is 5/2560 low, or 1.99609375 GHz, ±1 count ~ ±781 kHz.

PLL SUBSYSTEM

Charge Pump (CP) and Phase Detector (PD)

The phase detector (PD) has two inputs, one from the reference path divider and one from the RF path divider. When in lock, these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. The frequency of operation of the PD is f_{PD}. Most formulae related to step size, Δ-Σ modulation, timers, and so forth are functions of the operating frequency of the PD, f_{PD}. f_{PD} is also referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

Charge Pump

A simplified diagram of the charge pump is shown in Figure 43. The CP consists of four programmable current sources, two controlling the CP gain (Up Gain Register 0x09[13:7], and Down Gain Register 0x09[6:0]) and two controlling the CP offset, where the magnitude of the offset is set by Register 0x09[20:14], and the direction is selected by Register 0x09[21] = 1 for up and Register 0x09[22] = 1 for down offset.

CP gain is used at all times, whereas CP offset is recommended for fractional mode of operation only. Typically, the CP up and down gain settings are set to the same value (Register 0x09[13:7] = Register 0x09[6:0]).

Charge Pump Gain

Charge pump up and down gains are set by Register 0x09[6:0] and Register 0x09[13:7], respectively. The current gain of the pump in amps/radian is equal to the gain setting of this register (Register 0x09) divided by 2π.

Typical CP gain setting is set to 2 mA to 2.5 mA; however, lower values can also be used. Note that values less than 1 mA may result in degraded phase noise performance.

For example, if both Register 0x09[13:7] and Register 0x09[6:0] are set to 50 decimal, the output current of each pump is 1 mA, and the phase frequency detector gain is k_P = 1 mA/2π radians, or 159 µA/rad. See the Charge Pump (CP) and Phase Detector (PD) section for more information.

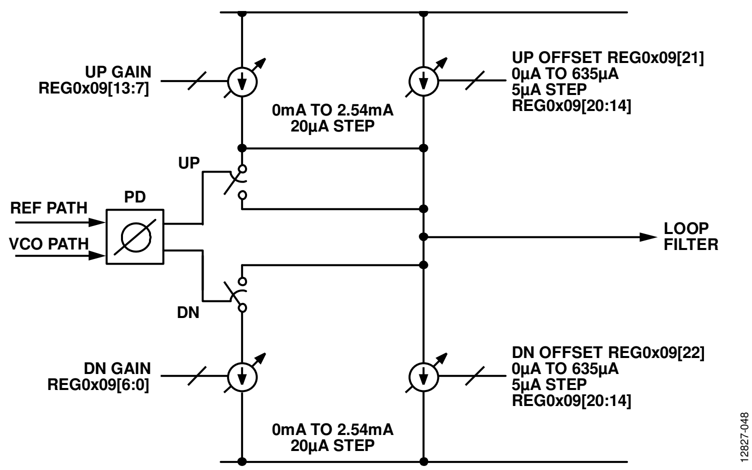

Figure 43. Charge Pump Gain and Offset Control

Charge Pump Phase Offset

In integer mode, the phase detector operates with zero offset. The divided reference signal and the divided VCO signal arrive at the phase detector inputs at the same time. Integer mode does not require any CP offset current. When operating in integer mode, disable CP offset in both directions (up and down) by writing Register 0x09[22:21] = 00b, and set the CP offset magnitude to zero by writing Register 0x09[20:14] = 0.

In fractional mode, CP linearity is of paramount importance. Any nonlinearity degrades phase noise and spurious performance. These nonlinearities are eliminated by operating the PD with an average phase offset, either positive or negative (either the reference or the VCO edge always arrives first at the PD, that is, leads).

A programmable CP offset current source is used to add dc current to the loop filter and to create the desired phase offset. Positive current causes the VCO to lead, negative current causes the reference to lead.

The CP offset is controlled via Register 0x09. The phase offset is scaled from 0° to 360°, where they arrive a full cycle late.

The specific level of charge pump offset current (Register 0x09, Bits[20:14]) is provided in Equation 9 and plotted in Figure 44.

$$\textit{Required CP Offset} = \min\left[(4.3 \times 10^{-9} \times f_{PD} \times I_{CP}), 0.25 \times I_{CP}\right] \quad (9)$$

where:
f_{PD} is the comparison frequency of the phase detector (Hz).
I_{CP} is the full-scale current setting (A) of the switching charge pump (set in Register 0x09[6:0] and Register 0x09[13:7]).

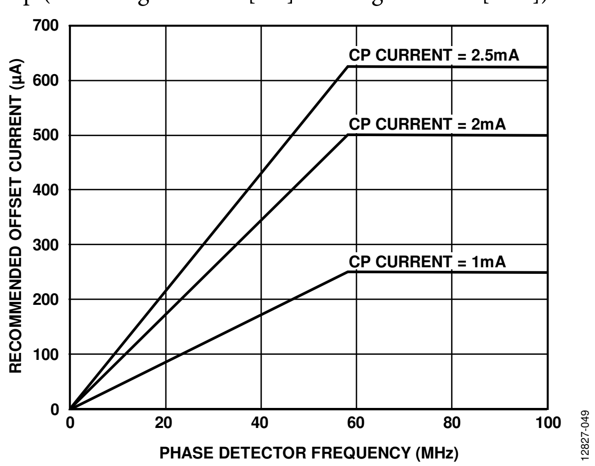

Figure 44. Recommended CP Offset Current vs. PD Frequency for Typical CP Gain Currents, Calculated Using Equation 9

Do not allow the required CP offset current to exceed 25% of the programmed CP current. It is recommended to enable the up offset and disable the down offset by writing Register 0x09, Bits[22:21] = 01b.

Operation with CP offset influences the required configuration of the lock detect function. See the description of the lock detect function in the Lock Detect section.

Phase Detector Functions

Register 0x0B, the phase detector register, allows manual access to control special phase detector features.

Setting Register 0x0B[5] = 0 masks the PD up output, which prevents the charge pump from pumping up.

Setting Register 0x0B[6] = 0, masks the PD down output, which prevents the charge pump from pumping down.

Clearing both Register 0x0B[5] and Register 0x0B[6] tristates the charge pump while leaving all other functions operating internally.

PD force up (Register 0x0B[9] = 1) and PD force down (Register 0x0B[10] = 1) allows the charge pump to be forced up or down, respectively. This forces the VCO to the ends of the tuning range, which is useful in testing the VCO.

Reference Input Stage

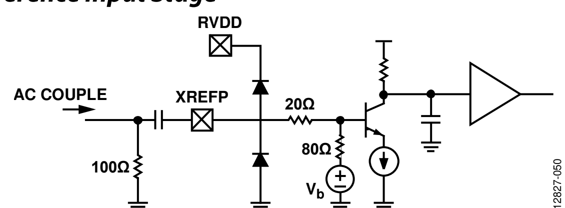

Figure 45. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal-based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation controlled by Register 0x08[21]. High gain (Register 0x08[21] = 0) is recommended below 200 MHz, and high frequency (Register 0x08[21] = 1) for 200 MHz to 350 MHz operation. The buffer is internally dc biased with 100 Ω internal termination. For a 50 Ω match, add an external 100 Ω resistor to ground followed by an ac coupling capacitor (impedance less than 1 Ω).

At low frequencies, a relatively square reference is recommended to maintain a high input slew rate. At higher frequencies, use a square or sinusoid.

Table 8 shows the recommended operating regions for different reference frequencies. If operating outside these regions, the device usually still operates, but with degraded reference path phase noise performance.

When operating at 50 MHz, the input referred phase noise of the PLL is between −148 dBc/Hz and −150 dBc/Hz at a 10 kHz offset, depending upon the mode of operation. To avoid degradation of the PLL noise contribution, the input reference signal should be 10 dB better than this floor. Note that such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

Table 8. Reference Sensitivity

Reference Input Frequency (MHz)	Square Input			Sinusoidal Input		
	Slew > 0.5 V/ns	Recommended Swing (V p-p)			Recommended Power Range (dBm)	
	Recommended	Minimum	Maximum	Recommended	Minimum	Maximum
<10	Yes	0.6	2.5	No	No	No
10	Yes	0.6	2.5	No	No	No
25	Yes	0.6	2.5	Okay	8	15
50	Yes	0.6	2.5	Yes	6	15
100	Yes	0.6	2.5	Yes	5	15
150	Okay	0.9	2.5	Yes	4	12
200	Okay	1.2	2.5	Yes	3	8

Reference Path, R Divider

The reference path, R divider is based on a 14-bit counter and can divide input signals by values from 1 to 16,383 and is controlled via Register 0x02.

RF Path, N Divider

The main RF path divider is capable of average divide ratios between $2^{19} – 5$ (524,283) and 20 in fractional mode, and $2^{19} – 1$ (524,287) to 16 in integer mode. The VCO frequency range divided by the minimum N divider value places practical restrictions on the maximum usable PD frequency. For example, a VCO operating at 1.5 GHz in fractional mode with a minimum N divider value of 20 has a maximum PD frequency of 75 MHz.

Lock Detect

The lock detect (LD) function verifies that the HMC832 is generating the desired frequency. It is enabled by writing Register 0x07[3] = 1. The HMC832 provides an LD indicator in one of two ways

- As an output available on the LD_SDO pin of the HMC832, (configuration is required to use the LD_SDO pin for LD purposes, for more information, see the Serial Port and Configuring the LD_SDO Pin for LD Output sections).
- Or reading from Register 0x12[1], where Bit 1 = 1 indicates a locked condition and Bit 1 = 0 indicates an unlocked condition.

The LD circuit expects the divided VCO edge and the divided reference edge to appear at the PD within a user specified time period (window), repeatedly. Either signal may arrive first, only the difference in arrival times is significant. The arrival of the two edges within the designated window increments an internal counter. When the count reaches and exceeds a user specified value (Register 0x07[2:0]) the HMC832 declares lock.

Failure in registering the two edges in any one window resets the counter and immediately declares an unlocked condition. Lock is deemed to be reestablished when the counter reaches the user specified value (Register 0x07[2:0]) again.

The HMC832 supports two lock detect modes:

- Analog LD, that only supports a fixed window size of 10 ns. Analog LD mode is selected by writing Register 0x07[6] = 0.
- Digital LD, that supports a user configurable window size, programmed in Register 0x07[11:7]. Digital LD is selected by writing Register 0x07[6] = 1.

Lock Detect Configuration

Optimal spectral performance in fractional mode requires CP current and CP offset current configuration discussed in detail in the Charge Pump (CP) and Phase Detector (PD) section.

These settings in Register 0x09 impact the required LD window size in fractional mode of operation. To function, the required lock detect window size is provided by Equation 10 in fractional mode and Equation 11 in integer mode.

$$LD\ Window\ (\text{sec}) = \frac{\left(\dfrac{I_{CP\,Offset}(\text{A})}{f_{PD}(\text{Hz}) \times I_{CP}\ (\text{A})} + 2.66 \times 10^{-9}(\text{sec}) + \dfrac{1}{f_{PD}(\text{Hz})}\right)}{2} \quad (10)$$

$$LD\ Window\ (sec) = \frac{1}{2 \times f_{PD}} \quad (11)$$

where:
f_{PD} is the comparison frequency of the phase detector.
$I_{CP\,Offset}$ is the charge pump offset current (Register 0x09[20:14]).
I_{CP} is the full-scale current setting of the switching charge pump (Register 0x09[6:0] or Register 0x09[13:7]).

If the result provided by Equation 10 is equal to 10 ns, analog LD can be used (Register 0x07[6] = 0); otherwise, digital LD is necessary (Register 0x07[6] = 1).

Table 9 lists the required Register 0x07 settings to appropriately program the digital LD window size. From Table 9, select the closest value in the digital LD window size columns to the ones calculated in Equation 10 and Equation 11, and program Register 0x07[11:10] and Register 0x07[9:7] accordingly.

Table 9. Typical Digital Lock Detect Window

LD Timer Speed Register 0x07 Bits[11:10]	Digital Lock Detect Window Size Nominal Value (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	7.1	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Register 0x07, Bits[9:7]	000	001	010	011	100	101	110	111

Digital Window Configuration Example

Assuming, fractional mode, with a 50 MHz PD and a

- Charge pump gain of 2 mA (Register 0x09[13:7] = 0x64, Register 0x09[6:0] = 0x64),
- Up offset (Register 0x09[22:21] = 01b)
- Offset current magnitude of +400 µA (Register 0x09[20:14] = 0x50)

Applying Equation 10, the required LD window size is:

$$LD\ Window\ (\text{sec}) = \frac{\left(\dfrac{0.4\times10^{-3}(\text{A})}{50\times10^{6}(\text{Hz})\times2\times10^{-3}(\text{A})} + 2.66\times10^{-9}(\text{sec}) + \dfrac{1}{50\times10^{6}(\text{Hz})}\right)}{2}$$

$$= 13.33\ \text{ns}$$

Locating the Table 9 value that is closest to this result is, in this case, 13.3 ≈ 13.33. To set the digital LD window size, program Register 0x07[11:10] = 10b and Register 0x07[9:7] = 010b, according to Table 9.

There is always a good solution for the lock detect window for a given operating point. The user should understand, however, that one solution does not fit all operating points. As observed from Equation 10 and Equation 11, if the charge pump offset or PD frequency is changed significantly, then the lock detect window may need to be adjusted.

Configuring the LD_SDO Pin for LD Output

Setting Register 0x0F[7] = 1 and Register 0x0F[4:0] = 1 displays the lock detect flag on the LD_SDO pin of the HMC832. When locked, LD_SDO is high. As the name suggests, LD_SDO pin is multiplexed between the LD and the serial data output (SDO) signals. Therefore, LD is available on the LD_SDO pin at all times except when a serial port read is requested, in which case the pin reverts temporarily to the serial data output pin, and returns to the lock detect flag after the read is completed.

LD can be made available on LD_SDO pin at all times by writing Register 0x0F[6] = 1. In that case, the HMC832 does not provide any readback functionality because the SDO signal is not available.

Cycle Slip Prevention (CSP)

When changing VCO frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than ±2π radians. Because the gain of the PD varies linearly with phase up to ±2π, the gain of a conventional PD cycles from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The output current from the charge pump cycles from maximum to minimum, even though the VCO has not yet reached its final frequency.

The charge on the loop filter small capacitor may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency reverse temporarily during locking. This phenomenon is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle slipping increases the time to lock to a value greater than that predicted by normal small signal Laplace transform analysis.

The HMC832 PD features an ability to reduce cycle slipping during acquisition. The cycle slip prevention (CSP) feature increases the PD gain during large phase errors. The specific phase error that triggers the momentary increase in PD gain is set via Register 0x0B[8:7].

Frequency Tuning

The HMC832 VCO subsystem always operates in fundamental frequency of operation (1500 MHz to 3000 MHz). The HMC832 generates frequencies below its fundamental frequency (25 MHz to 1500 MHz) by tuning to the appropriate fundamental frequency and selecting the appropriate output divider setting (divide by 2/4/6/ … 60/62) in VCO_REG 0x02[5:0].

The HMC832 automatically controls frequency tuning in the fundamental band of operation, for more information see the VCO Autocalibration section.

To tune to frequencies below the fundamental frequency range (<1500 MHz) it is required to tune the HMC832 to the appropriate fundamental frequency, then select the appropriate output divider setting (divide by 2/4/6/ … 60/62) in VCO_REG 0x02[5:0].

Integer Mode

The HMC832 is capable of operating in integer mode. For integer mode, set the following registers:

- Disable the fractional modulator, Register 0x06[11] = 0
- Bypass the modulator circuit, Register 0x06[7] = 1

In integer mode, the VCO step size is fixed to that of the PD frequency. Integer mode typically has a 3 dB lower phase noise than fractional mode for a given PD operating frequency. Integer mode, however, often requires a lower PD frequency to meet step size requirements. The fractional mode advantage is that higher PD frequencies can be used; therefore, lower phase noise can often be realized in fractional mode. Disable charge pump offset when in integer mode.