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HMC834LP6GE

v01.0112

FRACTIONAL-N PLL WITH INTEGRATED VCO
45 - 1050, 1400 - 2100, 2800 - 4200, 5600 - 8400 MHz

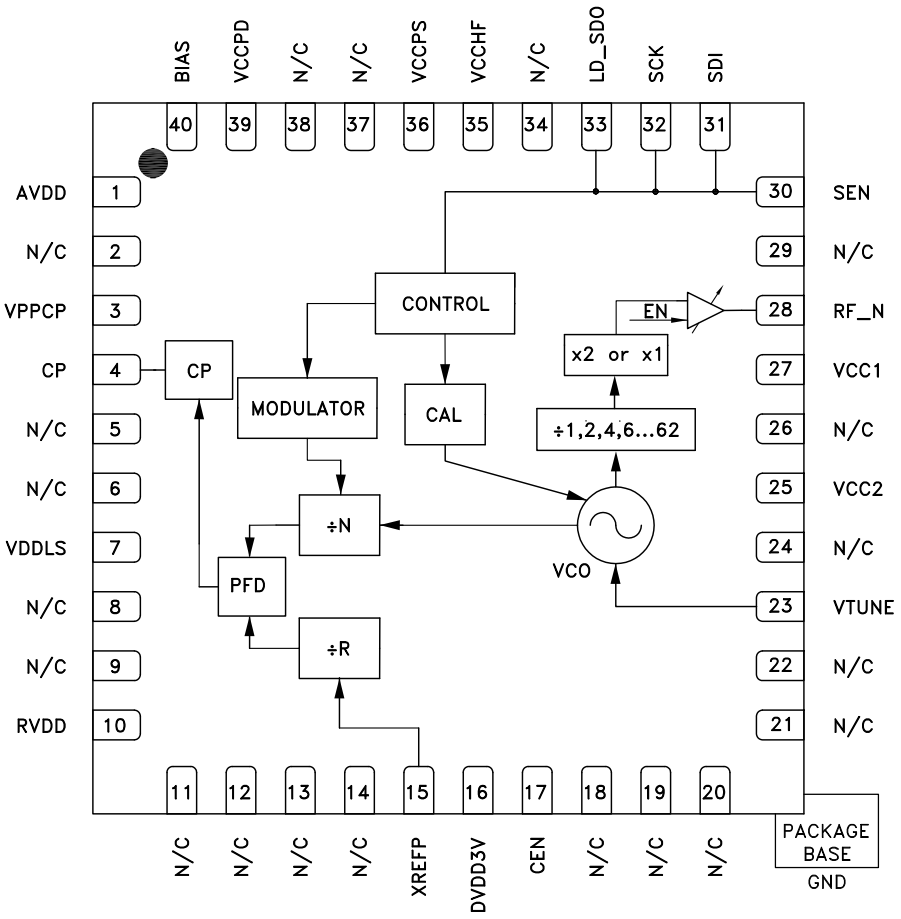
Features

- RF Bandwidth: 45 - 1050, 1400 - 2100, 2800 - 4200, 5600 - 8400 MHz
- Maximum Phase Detector Rate 100 MHz
- Ultra Low Phase Noise -110 dBc/Hz in Band Typ.
- Figure of Merit (FOM) -227 dBc/Hz
- <180 fs RMS Jitter
- 24-bit Step Size, Resolution 3 Hz typ
- Exact Frequency Mode
- Built in Digital Self Test
- 40 Lead 6x6 mm SMT Package: 36 mm^2

Typical Applications

- Cellular/4G, WiMax Infrastructure
- Repeaters and Femtocells
- Communications Test Equipment
- CATV Equipment
- Phased Array Applications
- DDS Replacement
- Very High Data Rate Radios
- Tunable Reference Source for Spurious-Free Performance

Functional Diagram



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EVALUATION KITS

- HMC834LP6GE Evaluation Board

DOCUMENTATION

Application Notes

- Frequency Hopping with Hittite PLLVCOs Application Note
- PLL & PLLVCO Serial Programming Interface Mode Selection Application Note
- Power-Up & Brown-Out Design Considerations for RF PLL +VCO Products Application Note
- Wideband RF PLL+VCO and Clock Generation Products FAQs

Data Sheet

- HMC834 Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™

REFERENCE MATERIALS

Quality Documentation

- HMC Legacy PCN: LP6CE and LP6GE QFN - Alternate assembly source

Technical Articles

- Low Cost PLL with Integrated VCO Enables Compact LO Solutions

DESIGN RESOURCES

- HMC834 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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FRACTIONAL-N PLL WITH INTEGRATED VCO
45 - 1050, 1400 - 2100, 2800 - 4200, 5600 - 8400 MHz

General Description

The HMC834LP6GE is a low noise, wide band, Fractional-N Phase-Locked-Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO) with a fundamental frequency of 2800 MHz - 4200 MHz, and an integrated VCO Output Divider (divide by 1/2/4/6.../60/62) and doubler, that together allow the HMC834LP6GE to generate frequencies from 45 MHz to 1050 MHz, from 1400 MHz to 2100 MHz, from 2800 MHz to 4200 MHz, and from 5600 MHz to 8400 MHz. The integrated Phase Detector (PD) and delta-sigma modulator, capable of operating at up to 100 MHz, permit wider loop-bandwidths with excellent spectral performance.

The HMC834LP6GE features industry leading phase noise and spurious performance, across all frequencies, that enable it to minimize blocker effects, and improve receiver sensitivity and transmitter spectral purity. The superior noise floor (< -170 dBc/Hz) makes the HMC834LP6GE an ideal source for a variety of applications - such as; LO for RF mixers, a clock source for high-frequency data-converters, or a tunable reference source for ultra-low spurious applications.

Additional features of the HMC834LP6GE include RF output power control from 0 to 6 dB (~2 dB steps), output Mute function, and a delta-sigma modulator Exact Frequency Mode which enables users to generate output frequencies with 0 Hz frequency error.

Electrical Specifications

VPPCP, VDDLS, VCC1, VCC2 = 5 V; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3 V Min and Max Specified across Temp -40 °C to +85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
RF Output Characteristics					
Output Frequency	Band 1	45		1050	MHz
	Band 2	1400		2100	MHz
	Band 3	*2800*		*4200*	*MHz*
	Band 4	5600		8400	MHz
VCO Frequency at PLL Input		2800		4200	MHz
RF Output Frequency at f_{VCO}		2800		4200	MHz
Output Power					
RF Output Power at f_{VCO} = 4000 MHz Across All Frequencies see Figure 9	Single-ended Power Broadband Matched Internally [1]	-2	0.5	2	dBm
Output Power Control	~2 dB Steps	6		7.5	dB
RF Output Power at f_{VCO} = 6000 MHz Across All Frequencies see Figure 9	Single-ended Power Broadband Matched Internally [1]	-11	-9	-7	dBm
RF Output Power at f_{VCO} = 8000 MHz Across All Frequencies see Figure 9	Single-ended Power Broadband Matched Internally [1]	-13.5	-11	-8.5	dBm
Harmonics for Fundamental Mode					
fo Mode at 4000 MHz	2nd / 3rd / 4th		-25/-29/-38		dBc
fo/2 Mode at 4000 MHz/2 = 2 GHz	2nd / 3rd / 4th		-25/-24/-35		dBc
fo/30 Mode at 2800 MHz/28 = 100 MHz	2nd / 3rd / 4th		-20/-10/-26		dBc
fo/62 Mode at 2800 MHz/62 = 45 MHz	2nd / 3rd / 4th		-14/-8/-21		dBc

[1] Measured single-ended. Additional 3 dB possible with differential outputs.
[2] Measured with 100 Ω external termination. See Hittite PLL w/ Integraged VCOs Operating Guide Reference Input Stage section for more details.

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Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
Harmonics in Doubler Mode					
2fo Mode at 5600 MHz	1/2 / 3rd / 4th/5th		-10/-22/-25/-35		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled [2]	1	2	3.3	Vp-p
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
Phase Detector (PD) [3]					
PD Frequency Fractional Mode B	[4]	DC		100	MHz
PD Frequency Fractional Mode A (and Register 6 [17:16] = 11)		DC		80	MHz
PD Frequency Integer Mode		DC		125	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 1 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-153		dBc/Hz
Logic Inputs					
Vsw		40	50	60	% DVDD
Logic Outputs					
VOH Output High Voltage			DVDD		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA
Power Supply Voltages					
3.3 V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD,DVDD	3.0	3.3	3.5	V
5 V Supplies	VPPCP, VDDLS, VCC1, VCC2	4.8	5	5.2	V
Power Supply Currents					
+5 V Analog Charge Pump	VPPCP, VDDLS		8		mA

[3] Slew rate of greater or equal to 0.5 ns/V is recommended, see PLL with Integrated RF VCOs Operating Guide for more details. Frequency is guaranteed across process voltage and temperature from -40 °C to +85 °C.
[4] This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional feedback mode, the maximum PFD rate = fvco/20 or 100 MHz, whichever is less.

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Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
+5 V VCO Core and VCO Buffer	fo/1 Mode VCC2		105		mA
	fo/N Mode VCC2		80		mA
+5 V VCO Divider and RF/PLL Buffer	Single-Ended Output Mode fo/1 Mode VCC1		25		mA
	Differential Output Mode fo/1 Mode VCC1		40		mA
	Single-Ended Output Mode fo/N Mode VCC1	80		100	mA
	Differential Output Mode fo/N Mode VCC1	95		115	mA
+3.3 V	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD3V		52		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg01h =0, Crystal Clocked 100 MHz		5		mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at fo @ 4 GHz/2 = 2 GHz					
10 kHz Offset			-83		dBc/Hz
100 kHz Offset			-113		dBc/Hz
1 MHz Offset			-139.5		dBc/Hz
10 MHz Offset			-165.5		dBc/Hz
100 MHz Offset			-167		dBc/Hz
VCO Open Loop Phase Noise at fo @ 2.8 GHz/28 = 100 MHz					
10 kHz Offset			-111		dBc/Hz
100 kHz Offset			-141		dBc/Hz
1 MHz Offset			-163.5		dBc/Hz
10 MHz Offset			-170		dBc/Hz
100 MHz Offset			-173		dBc/Hz
VCO Open Loop Phase Noise at 2fo @ 5.6 GHz					
10 kHz Offset			-77		dBc/Hz
100 kHz Offset			-107		dBc/Hz
1 MHz Offset			-132		dBc/Hz
10 MHz Offset			-154		dBc/Hz
100 MHz Offset			-162		dBc/Hz

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45 - 1050, 1400 - 2100, 2800 - 4200, 5600 - 8400 MHz

Parameter	Condition	Min.	Typ.	Max.	Units
VCO Open Loop Phase Noise at 2fo @ 8 GHz					
10 kHz Offset			-70		dBc/Hz
100 kHz Offset			-100		dBc/Hz
1 MHz Offset			-127		dBc/Hz
10 MHz Offset			-149		dBc/Hz
100 MHz Offset			-162		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 4053 MHz	Measured at 2.5 V		15		MHz/V
VCO Tuning Sensitivity at 3777 MHz	Measured at 2.5 V		13		MHz/V
VCO Tuning Sensitivity at 3411 MHz	Measured at 2.5 V		12		MHz/V
VCO Tuning Sensitivity at 2943 MHz	Measured at 2.5 V		11.5		MHz/V
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

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Figure 1. Typical Closed Loop Integer Phase Noise ["Loop Filter Configuration Table"]

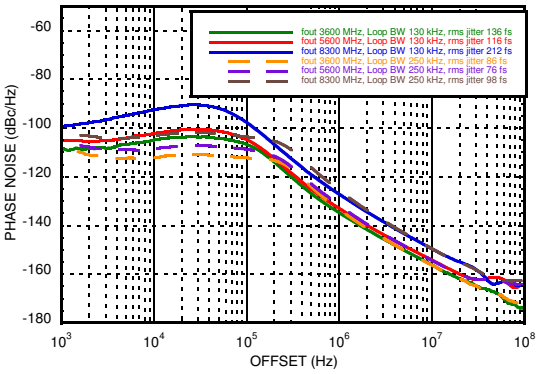

Figure 2. Typical Closed Loop Fractional Phase Noise ["Loop Filter Configuration Table"]

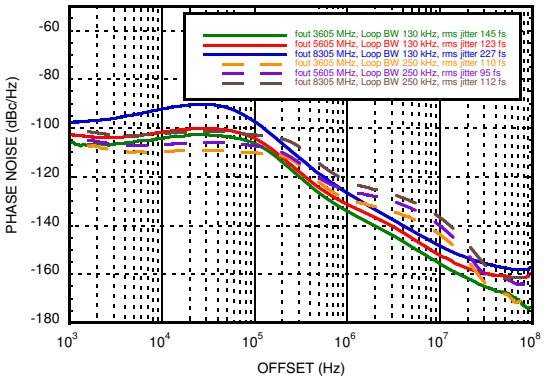

Figure 3. Free Running Phase Noise at f0

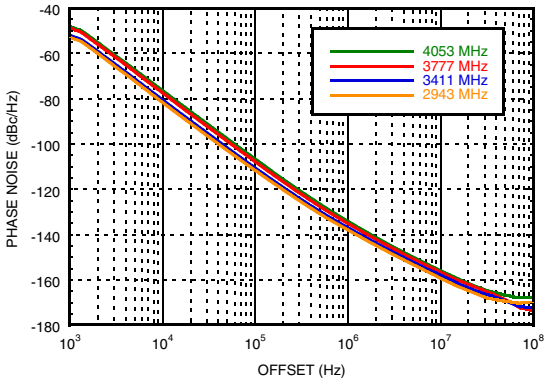

Figure 4. Free Running VCO Phase Noise vs. Temperature

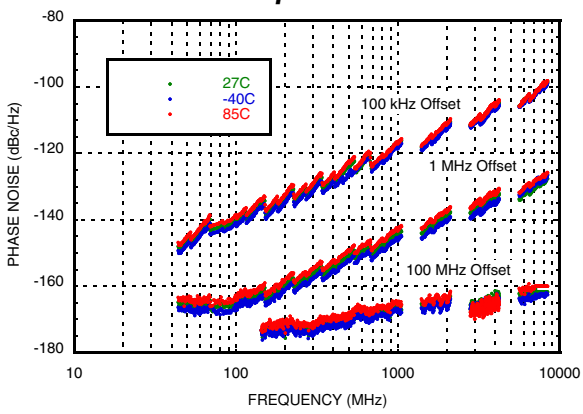

Figure 5. Typical VCO Sensitivity

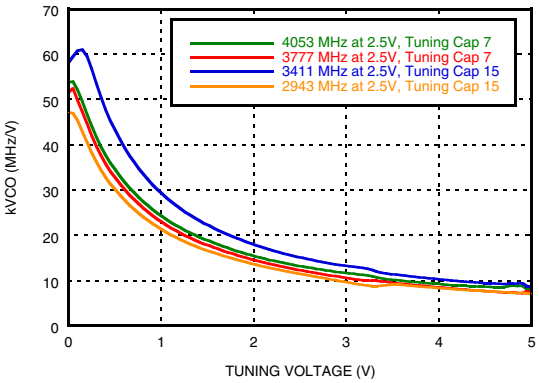

Figure 6. Typical Tuning Voltage After Calibration at f0

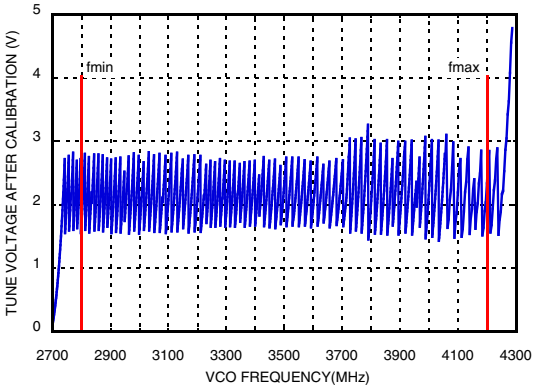

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Figure 7. Integrated RMS Jitter[1]

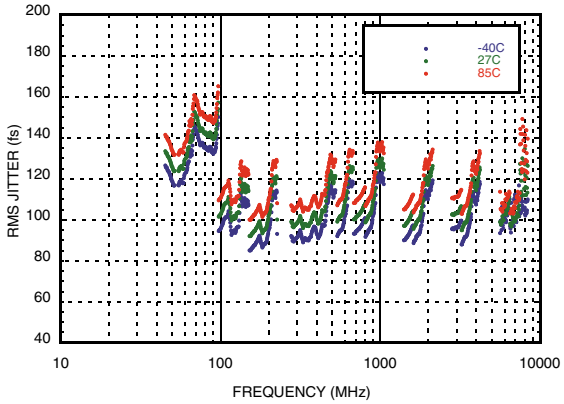


Figure 8. Figure of Merit

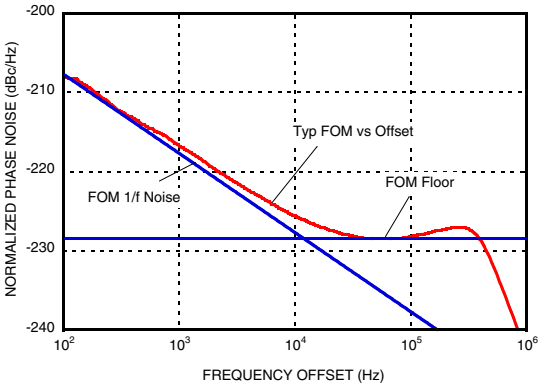


Figure 9. Typical Output Power vs. Temperature, Maximum Gain

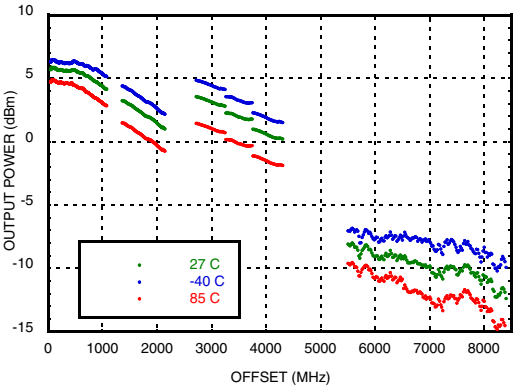


Figure 10. RF Output Return Loss

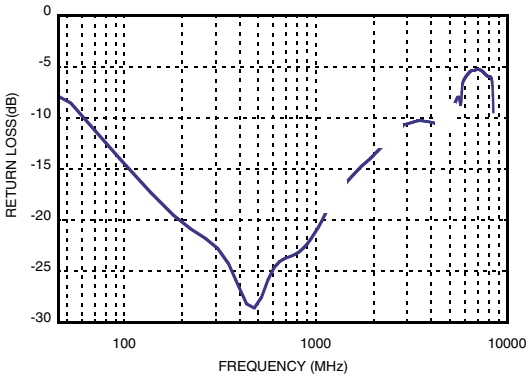


Figure 11. Reference Input Sensitivity Sinusoid Wave, 50 Ω[3]

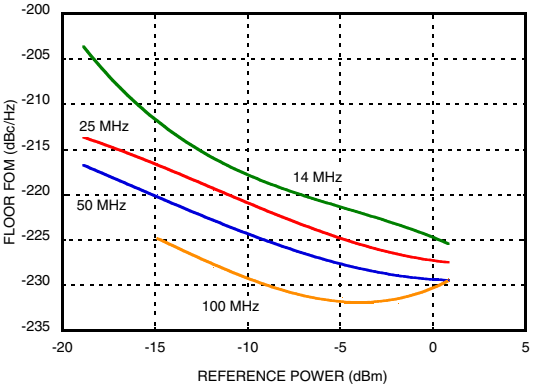
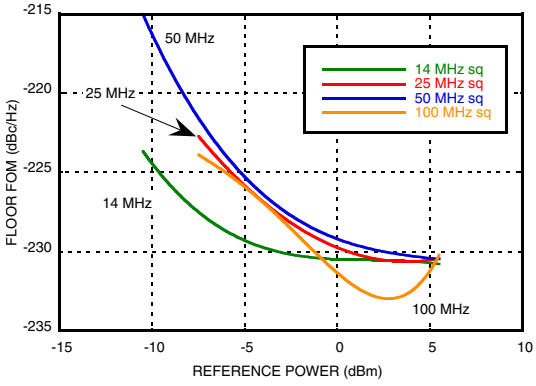


Figure 12. Reference Input Sensitivity, Square Wave, 50 Ω [2]



[1] RMS Jitter data is measured in fractional mode with 250 kHz Loop bandwidth using 100 MHz reference, PD 50 MHz. Integration bandwidth from 1 kHz to 100 MHz.

[2] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

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Figure 13. Integer Boundary Spur at 3600.2 MHz[4]

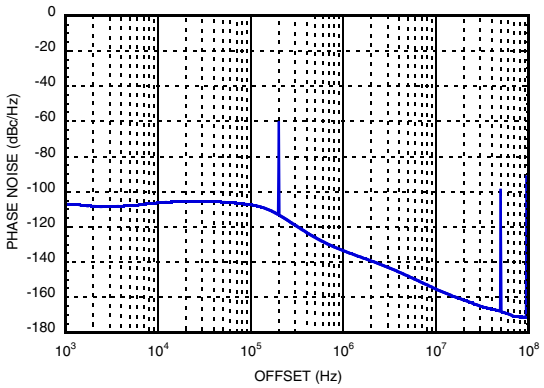


Figure 14. Integer Boundary Spur at 8300.8 MHz[4]

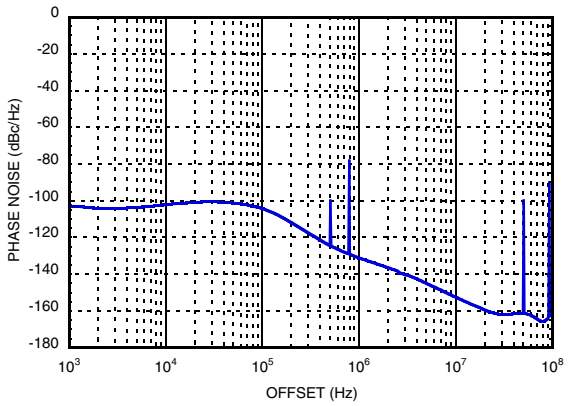


Figure 15. Integer-N, Exact Frequency Mode ON, Performance at 900 MHz[5]

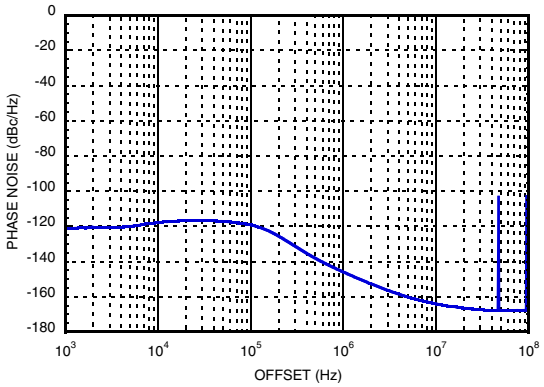


Figure 16. Fractional-N, Exact Frequency Mode ON, Performance at 1813.5 MHz[6]

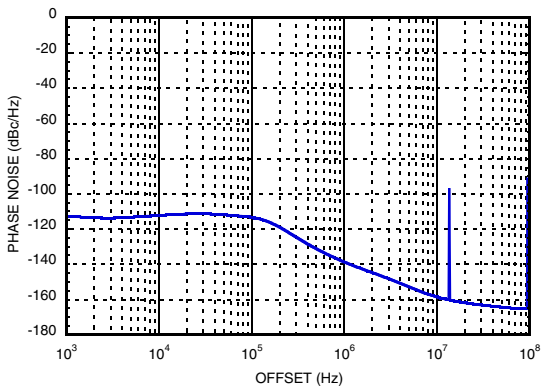


Figure 17. Fractional-N, Exact Frequency Mode ON, Performance at 3591 MHz[7]

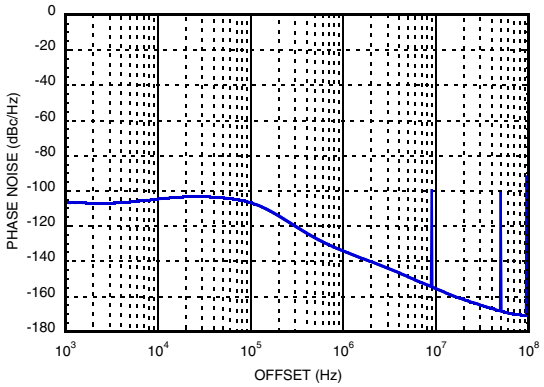
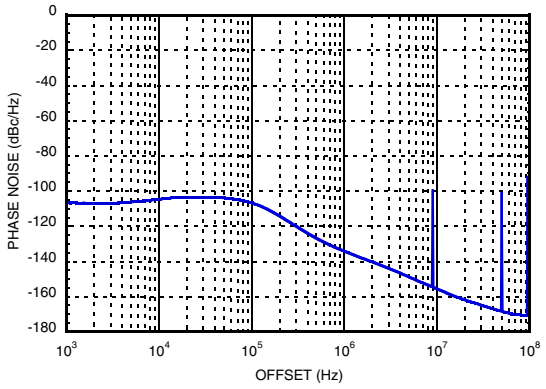


Figure 18. Fractional-N, Exact Frequency Mode OFF, Performance at 3591 MHz[8]



[4] Fractional Mode Mode B, Integer Boundary Spur, Loop Filter bandwidth 130 kHz, REF in 100 MHz, 50 MHz PD

[5] REF in 100 MHz, 50 MHz PD, Output Divider 4 Selected, Loop Filter bandwidth 130 kHz, Channel Spacing 100 kHz

[6] Exact Frequency Mode, REF in 100 MHz, 50 MHz PD, Output Divider 2 Selected, Loop Filter bandwidth = 130 kHz, Channel Spacing = 100 kHz

[7] Exact Frequency Mode, Channel Spacing 100 kHz, RF out = 3951 MHz, REF in 100 MHz, 50 MHz PD, Output Divider 1 selected, Loop Filter bandwidth 130 kHz,

[8] Fractional Mode B, RF out 3591 MHz, REF in 100 MHz, 50 MHz PD, Output Divider 1 selected, Loop Filter bandwidth 130 kHz.

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Figure 19. Worst Spur, Fixed 50 MHz Reference, Output Freq. = 3900.1 MHz[9]

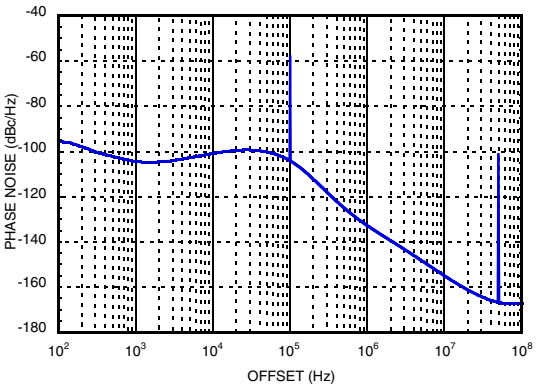


Figure 20. Worst Spur, Tunable Reference 47.5 MHz, Output Frequency = 3900.1 MHz [9]

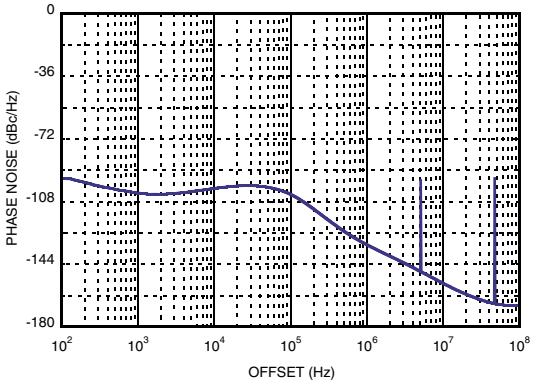


Figure 21. Worst Spur, Fixed vs. Tunable Reference [10]

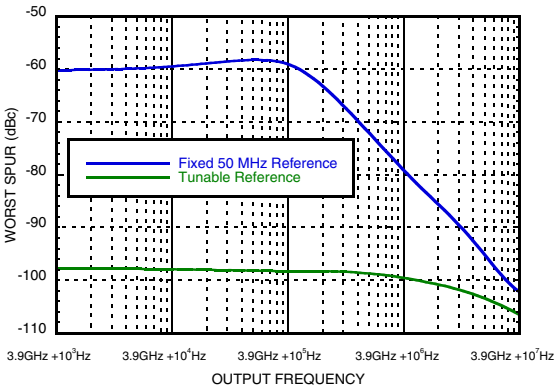
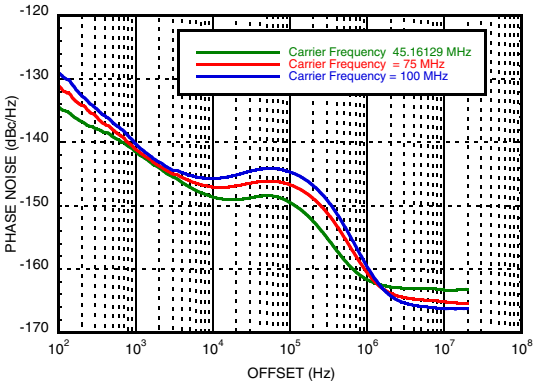
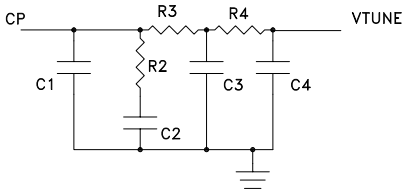


Figure 22. Low Frequency Performance [11]



Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
130	100	8.2	120	120	1	1.2	1.2	
250	150	3.3	18	18	2.2	1	1	

[9] Capability of HMC834LP6GE to generate low frequencies (as low as 45 MHz), enables the HMC834LP6GE to be used as a tunable reference source into another Hittite PLL. This maximizes spur performance of Hittite PLLs. Please see "HMC834LP6GE Application Information" for more information.

[10] The graph is generated by observing, and plotting, the magnitude of only the worst spur (largest magnitude), at any offset, at each output frequency, while using a fixed 50 MHz reference and a tunable reference tuned to 47.5 MHz. See "HMC834LP6GE Application Information" for more details.

[11] Phase noise performance of the HMC834LP6GE when used as a tunable reference source. HMC834LP6GE is operating at 4.2 GHz/42, 4.2 GHz/56, and 2.8 GHz/62 for the 100 MHz, 75 MHz, and 45.16129 MHz curves respectively, using a second order loop filter with 230 kHz bandwidth.

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Pin Descriptions

Pin Number	Function	Description
1	AVDD	DC Power Supply for analog circuitry.
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 29, 34, 37, 38	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	Power Supply for charge pump analog section
4	CP	Charge Pump Output
7	VDDLS	Power Supply for the charge pump digital section
10	RVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	VCO Analog Supply 2
27	VCC1	VCO Analog Supply 1
28	RF_N	RF Negative Output (On in differential and single-ended configuration)
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	DC Power Supply for Analog Circuitry
36	VCCPS	DC Power Supply for Analog Prescaler
39	VCCPD	DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V ±20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10GΩ meter such as Agilent 34410A, normal 10MΩ DVM will read erroneously.

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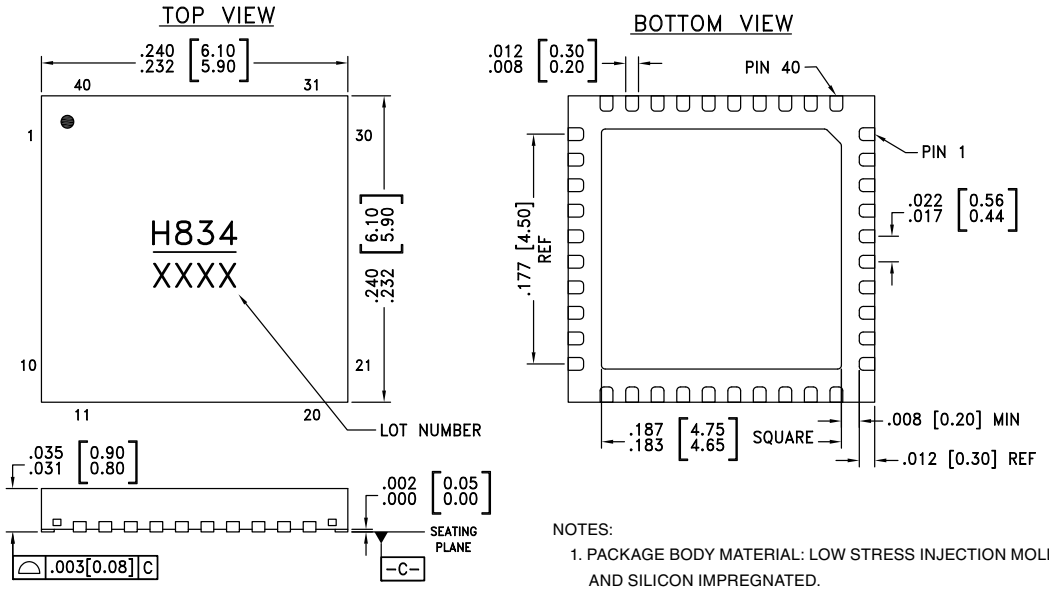
FRACTIONAL-N PLL WITH INTEGRATED VCO
45 - 1050, 1400 - 2100, 2800 - 4200, 5600 - 8400 MHz

Absolute Maximum Ratings

AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS	-0.3V to +3.6V
VPPCP, VDDLS, VCC1, VCC2	-0.3V to +5.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Maximum Junction Temperature	125 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	20 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC834LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H834 XXXX

[1] 4-Digit lot number XXXX

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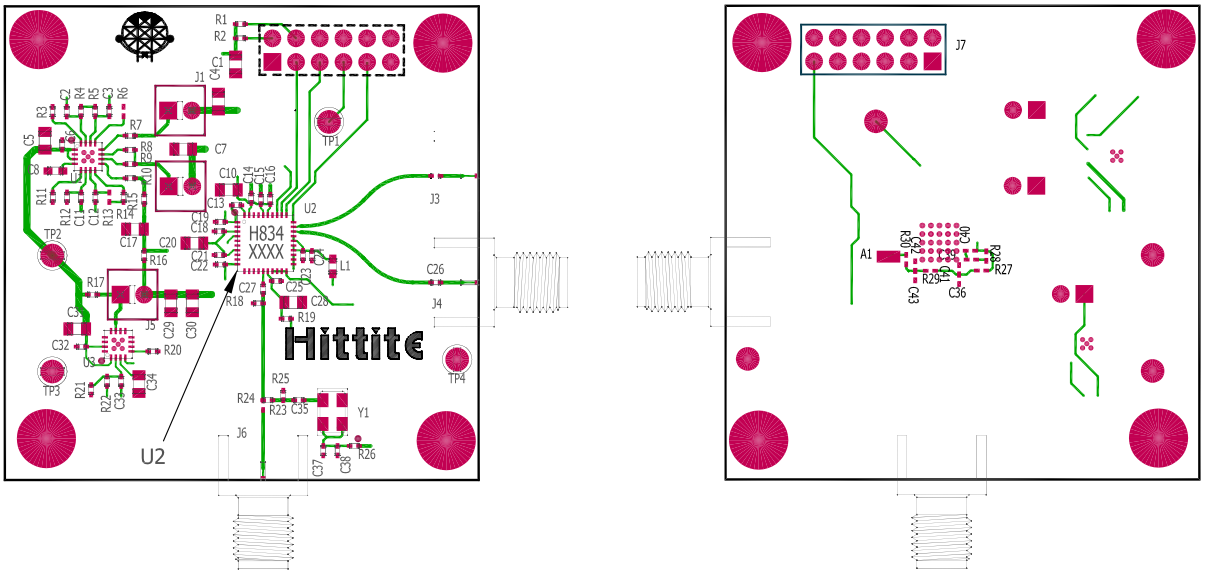
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC834LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC834LP6GE Evaluation PCB	EVAL01-HMC834LP6GE
Evaluation Kit	HMC834LP6GE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC834LP6GE

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HMC834LP6GE Application Information

Large bandwidth, industry leading phase noise and spurious performance, excellent noise floor (<-170 dBc/Hz), coupled with a high level of integration make the HMC834LP6GE ideal for a variety of applications; as an RF or IF stage LO, a clock source for high-frequency data-converters, or a tunable reference source for extremely low spurious applications (~ -100 dBc/Hz spurs).

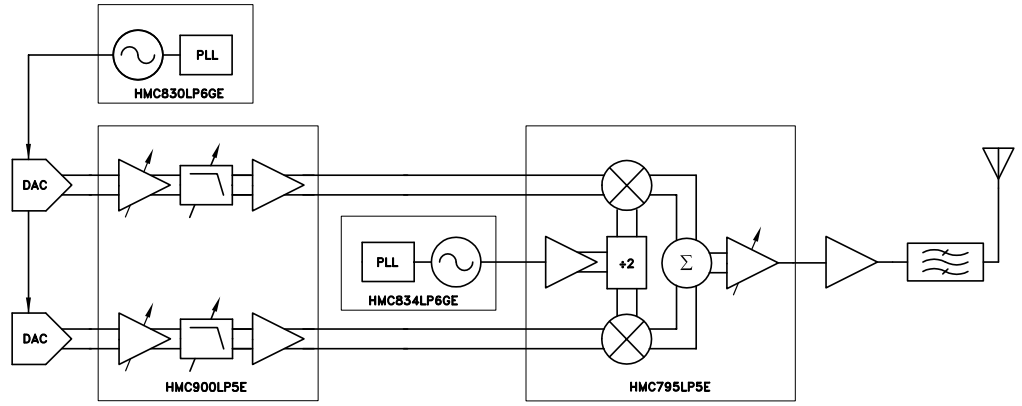

Figure 23. HMC834LP6GE in a typical transmit chain

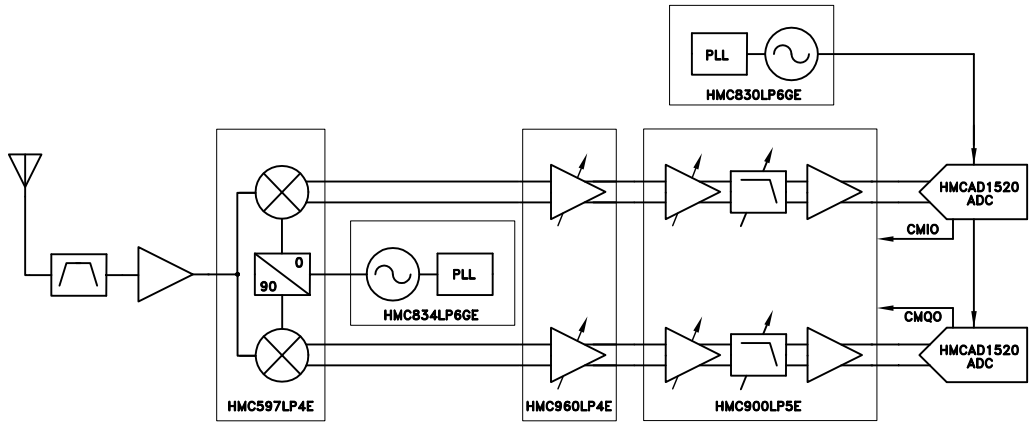

Figure 24. HMC834LP6GE in a typical receive chain

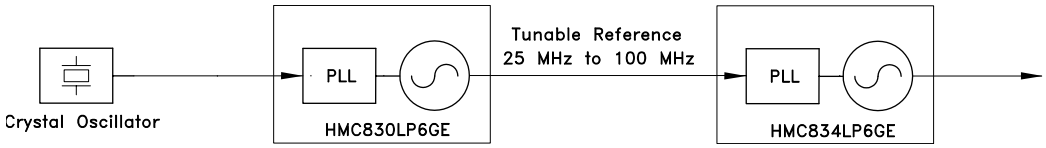

Figure 25. HMC834LP6GE used as a tunable reference for second HMC834LP6GE

Using the HMC834LP6GE with a tunable reference as shown in Figure 25, it is possible to drastically improve spurious emissions performance across all frequencies. Example shown in Figure 21 graph shows that it is possible to have spurious emissions ~ -100 dBc/Hz across all frequencies. For more information about spurious emissions, how they are related to the reference frequency, and how to tune the reference frequency for optimal spurious performance please see the "Spurious Performance" section of Hittite PLL w/ Integraged VCOs Operating Guide. Note that at very low output frequencies < 100 MHz, harmonics increase due to small internal AC coupling. Applications which are sensitive to harmonics may require external low pass filtering.

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Output gain setting for Optimal Power Flatness

The output of the HMC834LP6GE is matched to 50 Ω across all output frequencies from 45 MHz to 8400 MHz with gap. As a result of the wideband 50 Ω match, the output power of the HMC834LP6GE decreases with increasing output frequency, as shown in Figure 9. If required, it is possible to adjust the output stage gain setting of the HMC834LP6GE ("VCO_Reg 02h Biases") at various operating frequencies in order to achieve a more constant output power level across the frequency operating range of the HMC834LP6GE. An example is shown in Figure 26.

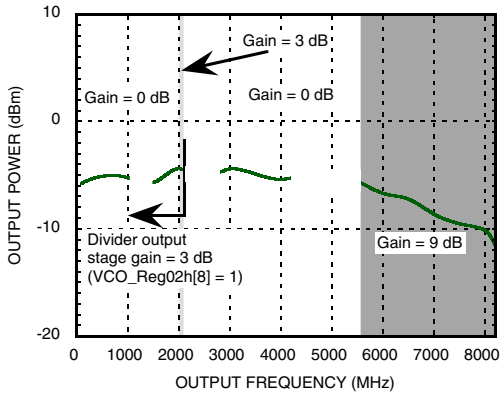

Figure 26.Reducing the output power variation of HMC834LP6GE across frequency by adjusting output stage gain control.

If a higher output power than that shown in Figure 26 is required, it is possible to follow the HMC834LP6GE output stage with a simple amplifier such as HMC311SC70E in order to achieve a constant and high output power level across the entire operating range of the HMC834LP6GE.

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1.0 Theory of Operation

HMC834LP6GE is targeted for ultra low phase noise applications and has been designed with very low noise reference path, phase detector and charge pump.

The HMC834LP6GE consists of the following functional blocks:

1. Reference Path Input Buffers and 'R' Divider
2. VCO Path Input Buffer and Multi-Modulus 'N' Divider
3. ΔΣ Fractional Modulator
4. Phase Detector
5. Charge Pump
6. Serial Port with Read Write Capability
7. General Purpose Output (GPO) Port
8. Power On Reset Circuit
9. VCO Subsystem
10. Built-In Self Test Features

1.1 VCO Subsystem

The HMC834LP6GE contains a VCO subsystem that can be configured to operate in:

- Fundamental frequency (fo) mode (2800 MHz to 4200 MHz).
- Divide by N (fo/N), where N = 1,2,4,6,8...58,60,62 mode (45 MHz to 1400 MHz and 1400 MHz to 2100 MHz with gap).
- Doubler (2fo) mode (5600 MHz to 8400 MHz).

All modes are VCO register programmable as shown in Figure 27. One loop filter design can be used for the entire frequency of operation of the HMC834LP6GE.

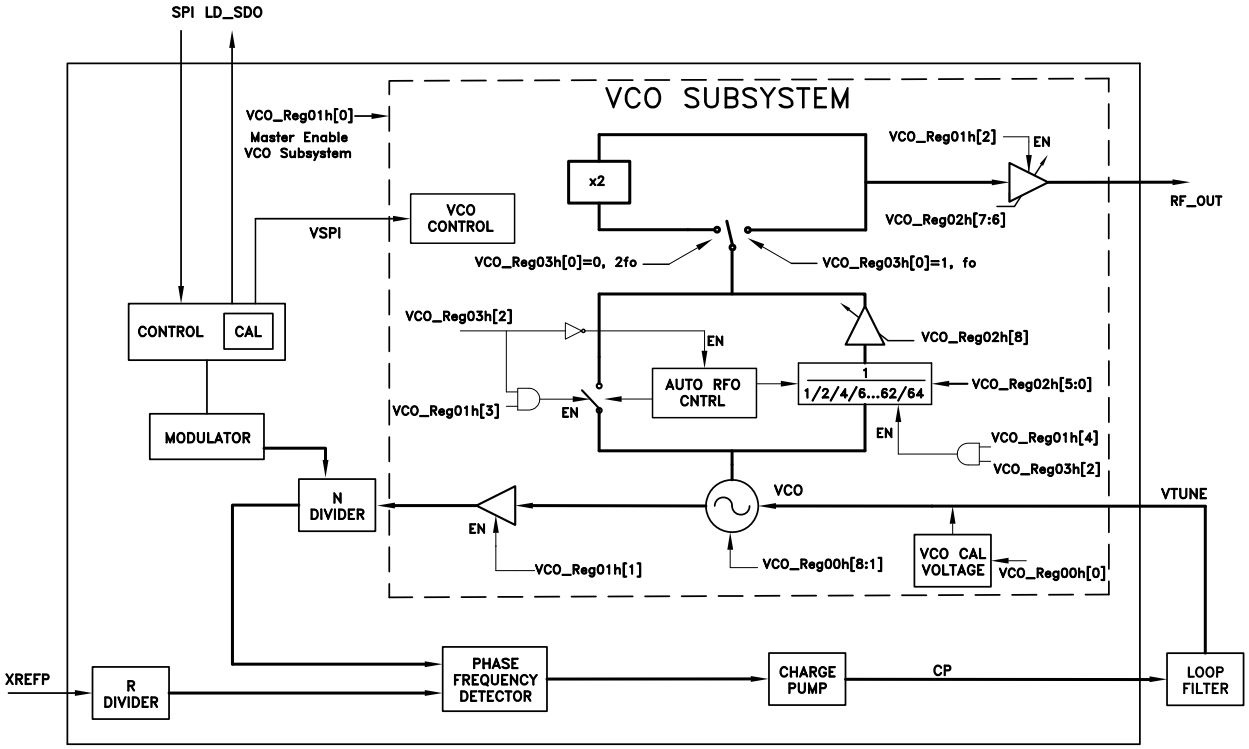

Figure 27. PLL and VCO Subsystems

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1.2 VCO Calibration

1.2.1 VCO Auto-Calibration (AutoCal)

HMC834LP6GE uses a step tuned type VCO. A simplified step tuned VCO is shown in Figure 28. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or 'stepped' by switching in/out VCO tank capacitors. A more detailed view of a typical VCO subsystem configuration is shown in Figure 29. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the HMC834LP6GE's charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (kvco).

The VCO switches are normally controlled automatically by the HMC834LP6GE using the Auto-Calibration feature. The Auto-Calibration feature is implemented in the internal state machine. It manages the selection of the VCO sub-band (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via register Reg 05h for testing or for other special purpose operation. Other control bits specific to the VCO are also sent via Reg 05h.

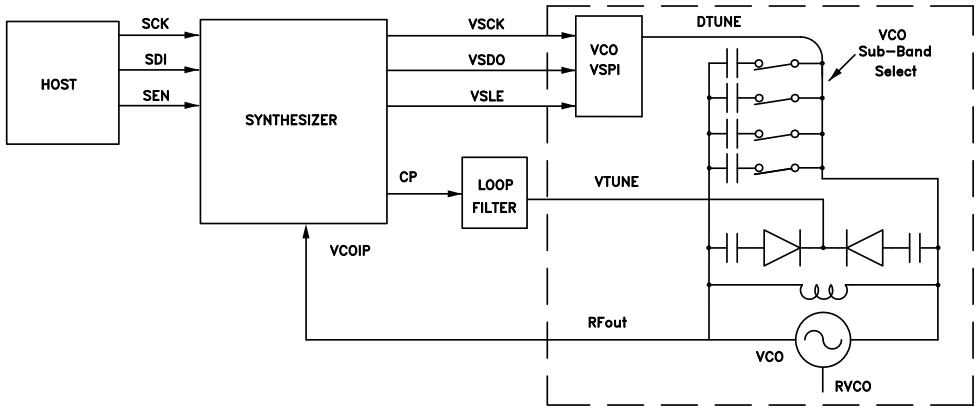

Figure 28. Simplified Step Tuned VCO

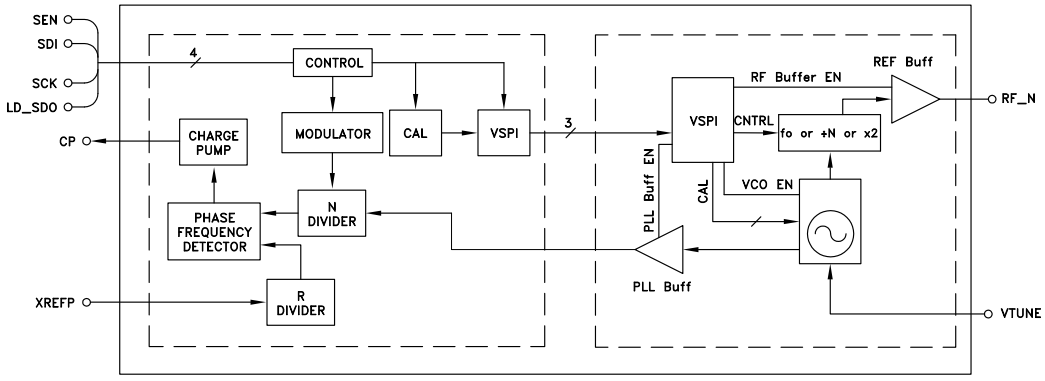

Figure 29. HMC834LP6GE PLL and VCO Subsystems

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC834LP6GE knows which switch position on the VCO is optimum for the desired output frequency. The HMC834LP6GE supports Auto-Calibration (AutoCal) of the step tuned VCO. The AutoCal fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the

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desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a very narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 30. Note how the tuning voltage stays in a narrow range over a wide range of output frequencies.

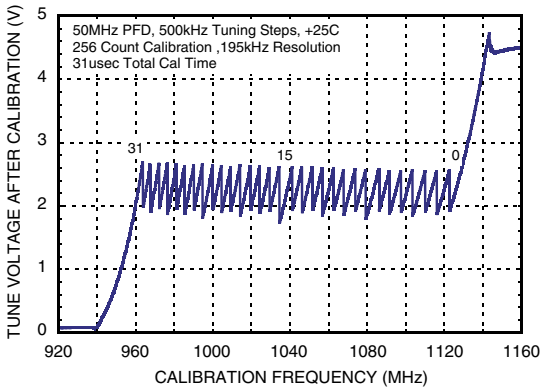

Figure 30. A Typical 5-Bit 32 Switch VCO Tuning Voltage After Calibration

The calibration is normally run automatically once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally have to be concerned about which switch setting is used for a given frequency as this is handled by the AutoCal routine. The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency, and ensures that the VCO will stay locked and perform well over it's full temperature range without additional calibration, regardless of the temperature that the VCO was calibrated at.

Auto-Calibration can also be disabled allowing manual VCO tuning. Refer to section 1.2.2 for a description of manual tuning

1.2.1.1 AutoCal Use of Reg05h

AutoCal transfers switch control data to the VCO subsystem via Reg 05h. The address of the VCO subsystem in Reg 05h is not altered by the AutoCal routine. The address and ID of the VCO subsystem in Reg 05h must be set to the correct value before AutoCal is executed. For more information see section 1.19.

1.2.1.2 Auto-reLock on Lock Detect Failure

It is possible by setting Reg 07h*[13]* to have the VCO subsystem automatically re-run the calibration routine and re-lock itself if Lock Detect indicates an unlocked condition for any reason. With this option the system will attempt to re-Lock only once. Auto-reLock is recommended.

1.2.2 Manual VCO Calibration for Fast Frequency Hopping

If it is desirable to switch frequencies very quickly it is possible to eliminate the AutoCal time by calibrating the VCO in advance and storing the switch number vs frequency information in the host. This can be done by initially locking the PLL with Integrated VCO on each desired frequency using AutoCal, then reading, and storing the VCO switch settings selected. The VCO switch settings are available in Reg 10h[7:0] after every AutoCal operation. The host must then program the VCO switch settings directly when changing frequencies. Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when AutoCal is disabled. Hence frequency changes with manual control and AutoCal disabled, requires a minimum of two serial port transfers to the PLL, once to set the VCO switches, and once to set the PLL frequency.

If AutoCal is disabled Reg 0Ah*[11]=1*, the VCO will update its registers with the value written via Reg 05h

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immediately. The VCO internal transfer requires 16 VSCK clock cycles after the completion of a write to Reg 05h. VSCK and the AutoCal controller clock are equal to the input reference divided by 0, 4,16 or 32 as controlled by Reg 0Ah*[14:13]*.

1.2.2.1 Registers required for Frequency Changes in Fractional Mode

A large change of frequency, in fractional mode (Reg 06h*[11]=1*), may require Main Serial Port writes to:

1. the integer register intg, Reg 03h *(only required if the integer part changes)*
2. the VCO SPI register, Reg 05h
   - required for manual control of VCO if Reg 0Ah*[11]=1 (AutoCal disabled)*
   - required to change the RF Divider value if needed (VCO_Reg 02h)
   - required to turn on/off the doubler mode if needed (VCO_Reg 03h[0])
3. the fractional register, Reg 04h. The fractional register write triggers AutoCal if Reg 0Ah*[11]=0*, and is loaded into the modulator automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah*[11]=1*, the fractional frequency change is loaded into the modulator immediately when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with AutoCal enabled (Reg 0Ah*[11]=0*), usually only require a single write to the fractional register. Worst case, 5 Main Serial Port transfers to the HMC834LP6GE could be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, then the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register Reg 04h for frequency changes.

1.2.2.2 Registers Required for Frequency Changes in Integer Mode

A change of frequency, in integer mode *(*Reg 06h*[11]=0)*, requires Main Serial Port writes to:

1. VCO SPI register, Reg 05h
   - required for manual control of VCO if Reg 0Ah*[11]=1 (AutoCal disabled)*
   - required to change the RF Divider value if needed (VCO_Reg 02h)
   - required to turn on/off the doubler mode if needed (VCO_Reg 03h[0])
2. the integer register Reg 03h.
   - In integer mode, an integer register write triggers AutoCal if Reg 0Ah*[11]=0*, and is loaded into the prescaler automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah*[11]=1*, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally changes to the integer register cause large steps in the VCO frequency, hence the VCO switch settings must be adjusted. AutoCal enabled is the recommended method for integer mode frequency changes. If AutoCal is disabled (Reg 0Ah*[11]=1*), a priori knowledge of the correct VCO switch setting and the corresponding adjustment to the VCO is required before executing the integer frequency change.

1.2.3 VCO AutoCal on Frequency Change

Assuming Reg 0Ah*[11]=0*, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the AutoCal routine for any reason, at the same frequency, simply rewrite the frequency change with the same value and the AutoCal routine will execute again without changing final frequency.

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1.2.4 VCO AutoCal Time & Accuracy

The VCO frequency is counted for T_{mmt}, the period of a single AutoCal measurement cycle.

$$T_{mmt} = T_{xtal} \cdot R \cdot 2^n \quad \text{(EQ 1)}$$

n — is set by Reg 0Ah*[2:0]* and results in measurement periods which are multiples of the PD period, $T_{xtal}R$.

R — is the reference path division ratio currently in use, Reg 02h

T_{xtal} — is the period of the external reference (crystal) oscillator.

The VCO AutoCal counter will, on average, expect to register N counts, rounded down (floor) to the nearest integer, every PD cycle.

N — is the ratio of the target VCO frequency, f_{vco}, to the frequency of the PD, f_{pd}, where N can be any rational number supported by the N divider.

N is set by the integer (N_{int} = Reg 03h) and fractional (N_{frac} = Reg 04h) register contents

$$N = N_{int} + N_{frac} / 2^{24} \quad \text{(EQ 2)}$$

The AutoCal state machine and the data transfers to the internal VCO subsystem SPI (VSPI) run at the rate of the FSM clock, T_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$T_{FSM} = T_{xtal} \cdot 2^m \quad \text{(EQ 3)}$$

m — is 0, 2, 4 or 5 as determined by Reg 0Ah*[14:13]*

The expected number of VCO counts, V, is given by

$$V = floor\ (N \cdot 2^n) \quad \text{(EQ 4)}$$

The nominal VCO frequency measured, f_{vcom}, is given by

$$f_{vcom} = V \cdot f_{xtal} / (2^n \cdot R) \quad \text{(EQ 5)}$$

where the worst case measurement error, f_{err} , is:

$$f_{err} \approx \pm f_{pd} / 2^{n+1} \quad \text{(EQ 6)}$$

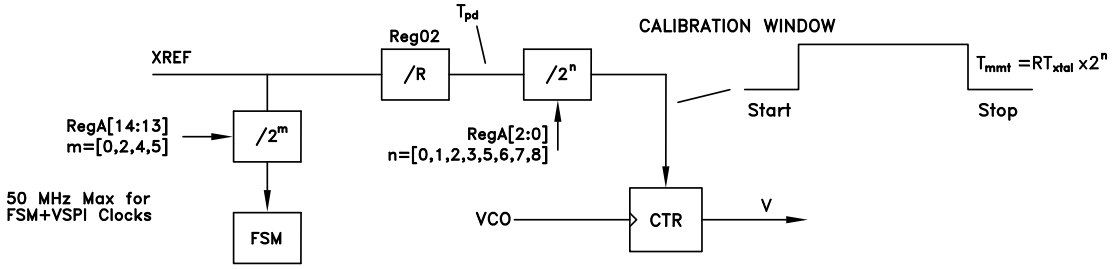

Figure 31. VCO Calibration

A 5-bit step tuned VCO, for example, nominally requires 5 measurements for calibration, worst case 6 measurements, and hence 7 VSPI data transfers of 20 clock cycles each. The measurement has a programmable number of wait states, k, of 100 FSM cycles defined by Reg 0Ah[7:6] = k. Hence total calibration time, worst case, is given by:

$$T_{cal} = k100T_{FSM} + 6T_{PD}\ 2^n + 7 \cdot 20T_{FSM} \quad \text{(EQ 7)}$$

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or equivalently

$$T_{cal} = T_{xtal}\,(6R \cdot 2^{n} + (140+100k) \cdot 2^{m}) \quad \text{(EQ 8)}$$

where k = Reg 0Ah*[7:6] decimal*

For guaranteed hold of lock, across temperature extremes, the resolution should be better than 1/8th the frequency step caused by a VCO sub-band switch change. Better resolution settings will show no improvement.

1.2.4.1 VCO AutoCal Example

The VCO subsystem must satisfy the maximum f_{pd} limited by the two following conditions:

a. N ≥ 16 (f_{int}), N ≥ 20.0 (f_{frac}), where N = f_{VCO}/ f_{pd}

b. f_{pd} ≤ 100 MHz

Suppose the VCO subsystem output frequency is to operate at 2.01 GHz. Our example crystal frequency is f_{xtal} = *50 MHz, R=1, and m=0 (*Figure 31*)*, hence T_{FSM} = 20 ns (50 MHz). Note, when using AutoCal, the maximum AutoCal Finite State Machine (FSM) clock cannot exceed 60 MHz (see Reg 0Ah*[14:13]*). The FSM clock does not affect the accuracy of the measurement, it only affects the time to produce the result. This same clock is used to clock the 16 bit VCO serial port.

If time to change frequencies is not a concern, then one may set the calibration time for maximum accuracy, and therefore not be concerned with measurement resolution.

Using an input crystal of 50 MHz (R=1 and fpd=50 MHz) the times and accuracies for calibration using (EQ 6) and (EQ 8) are shown in Table 1. Where minimal tuning time is 1/8th of the VCO band spacing.

Across all VCOs, a measurement resolution better than 800 kHz will produce correct results. Setting m = 0, n = 5, provides 781 kHz of resolution and adds 8.6 µs of AutoCal time to a normal frequency hop. Once the AutoCal sets the final switch value, 8.64 µs after the frequency change command, the fractional register will be loaded, and the loop will lock with a normal transient predicted by the loop dynamics. Hence we can see in this example that AutoCal typically adds about 8.6 µs to the normal time to achieve frequency lock. Hence, AutoCal should be used for all but the most extreme frequency hopping requirements.

Table 1. AutoCal Example with F_{xtal} = 50 MHz, R = 1, m = 0

Control Value *Reg0Ah[2:0]*	n	2^n	T_{mmt} (µs)	T_{cal} (µs)	F_{err} Max
0	0	1	0.02	4.92	± 25 MHz
1	1	2	0.04	5.04	± 12.5 MHz
2	2	4	0.08	5.28	± 6.25 MHz
3	3	8	0.16	5.76	± 3.125 MHz
4	5	32	0.64	8.64	± 781 kHz
5	6	64	1.28	12.48	± 390 kHz
6	7	128	2.56	20.16	± 195 kHz
7	8	256	5.12	35.52	± 98 kHz

1.2.5 VCO Output Mute Function

The output mute function enables the HMC834LP6GE to disable the VCO output while maintaining the PLL and VCO subsystems fully functional. The mute function provides over 40 dB of isolation throughout the operating range of the HMC834LP6GE. To mute the output of the HMC834LP6GE, the following register writes are necessary:

1. VCO_Reg 03h [2] = 1, to place the VCO subsystem in manual mode
2. VCO_Reg 01h[2] = 1, to disable the VCO subsystem output buffer
3. VCO_Reg 01h [3] = 0, to disable the VCO subsystem limiter.

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Please note that the VCO subsystem registers are not directly accessible. They are written to via PLL Reg 05h. More information about VCO subsystem SPI in section 1.19.

1.3 VCO Built in Test with AutoCal

The frequency limits of the VCO can be measured using the BIST features of the AutoCal machine.

This is done by setting Reg 0Ah[10]=1 which freezes the VCO switches in one position. VCO switches may then be written manually, with the varactor biased at the nominal mid-rail voltage used for AutoCal. For example to measure the VCO maximum frequency use switch 0, written to the VCO subsystem via Reg 05h=[000000000 0000 VCOID]. Where VCOID = '000'b.

If AutoCal is enabled, (Reg 0Ah[11] = 0), and a new frequency is written, AutoCal will run, but with switches frozen. The VCO frequency error relative to the command frequency will be measured and results written to Reg 11h[19:0] where Reg 11h[19] is the sign bit. The result will be written in terms of VCO count error (EQ 4). For example if the expected VCO is 2 GHz, reference is 50 MHz, and n is 6, we expect to measure 2560 counts. If we measure a difference of -5 counts in Reg 11h, then it means we actually measured 2555 counts. Hence the actual frequency of the VCO is 5/2560 low, or 1.99609375 GHz, ±1 Count ~ ±781 kHz.

1.4 Spurious Performance

1.4.1 Integer Operation and Reference Spurious

The VCO always operates at an integer multiple of the PD frequency in an integer synthesizer. In general, spurious signals originating from an integer synthesizer can only occur at multiples of the PD frequency. These unwanted outputs closest to the carrier are often simply referred to as reference sidebands. Unwanted reference harmonics can also exist far from the carrier due to circuit isolation.

Spurs unrelated to the reference frequency must originate from outside sources. External spurious sources can modulate the VCO indirectly through power supplies, ground, or output ports, or bypass the loop filter due to poor isolation of the filter. It can also simply add to the output of the PLL.

Reference spurious levels are typically below -100 dBc with a well designed board layout. A regulator with low noise and high power supply rejection, such as the HMC1060LP3E, is recommended to minimize external spurious sources.

Reference spurious levels of below -100 dBc require superb board isolation of power supplies, isolation of the VCO from the digital switching of the synthesizer and isolation of the VCO load from the synthesizer. Typical board layout, regulator design, eval boards and application information are available for very low spurious operation. Operation with lower levels of isolation in the application circuit board, from those recommended by Hittite, can result in higher spurious levels.

If the application environment contains other interfering frequencies unrelated to the PD frequency, and if the application isolation from the board layout and regulation are insufficient, the unwanted interfering frequencies will mix with the desired synthesizer output and cause additional spurious emissions. The level of these emissions is dependant upon isolation and supply regulation or rejection (PSRR).

1.4.2 Fractional Operation and Spurious

Unlike an integer PLL, spurious signals in a fractional PLL can occur due to the fact that the VCO operates at frequencies unrelated to the PD frequency. Hence intermodulation of the VCO and the PD harmonics can cause spurious sidebands. Spurious emissions are largest when the VCO operates very close to an integer multiple of the PD. When the VCO operates exactly at a harmonic of the PD then, no in-close mixing products are present.

As shown in Figure 32, interference is always present at multiples of the PD frequency, f_{pd}, and the VCO frequency, f_{vco}. The difference, Δ, between the VCO frequency and the nearest harmonic of the reference, will create what are referred to as integer boundary spurs. Depending upon the mode of operation of

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the synthesizer, higher order, lower power spurs may also occur at multiples of integer fractions (sub-harmonics) of the PD frequency. That is, fractional VCO frequencies which are near $nf_{pd} + f_{pd}d/m$, where n, d and m are all integers and d<m (mathematicians refer to d/m as a rational number). We will refer to $f_{pd}d/m$ as an integer fraction. The denominator, m, is the order of the spurious product. Higher values of m produce smaller amplitude spurious at offsets of mΔ and usually when m>4 spurs are small or unmeasurable.

The worst case, in fractional mode, is when d=0, and the VCO frequency is offset from nf_{pd} by less than the loop bandwidth. This is the "in-band integer boundary" case.

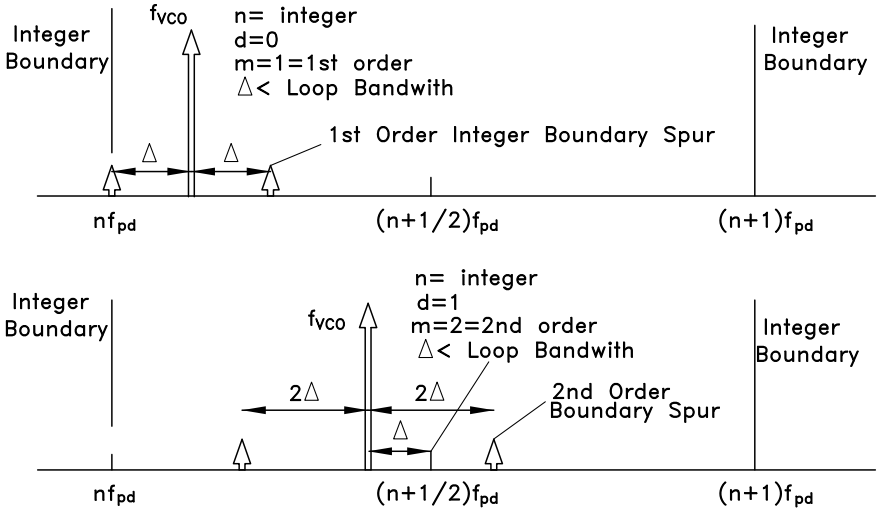

Figure 32. Fractional Spurious Example

Characterization of the levels and orders of these products is not unlike a mixer spur chart. Exact levels of the products are dependent upon isolation of the various synthesizer parts. Hittite can offer guidance about expected levels of spurious with HMC834LP6GE evaluation boards. Regulators with high power supply rejection ratios (PSRR) are recommended, especially in noisy applications.

1.4.2.1 Charge Pump and Phase Detector Spurious Considerations

Charge pump and phase detector linearity are of paramount importance when operating in fractional mode. Any non-linearity degrades phase noise and spurious performance.

We define zero phase error when the reference signal and the divider VCO signal arrive at the Phase Detector at the same time. Phase detector linearity degrades when the phase error is very small and when the random phase errors cause the phase detector to switch back an forth between reference lead and VCO lead.

These switching non-linearities in fractional mode are eliminated by operating the phase detector with an average phase offset such that either the reference or VCO always leads.

A programmable charge pump offset current source is used to add DC current to the loop filter and create the desired phase offset. Positive current causes the VCO to lead, negative current causes the reference to lead.

The offset charge pump is controlled via Reg 09h. The phase offset is scaled from 0 degrees, that is the reference and the VCO path arrive in phase, to 360 degrees, where they arrive a full cycle late. The offset can also be thought of in absolute time difference between the arrivals.

The recommended operating point for the charge pump in fractional mode is one where the time offset at the phase detector is ~2.5ns + $4T_{VCO}$, where T_{VCO} is the RF period at the fractional prescaler input. The required CP offset current should never exceed 25% of the programmed CP current.

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The specific level of charge pump offset current Reg 09h[20:14] is determined by this time offset, the comparison frequency and the charge pump current:

$$\text{Required CP Offset} = \min\left[\left(\left(2.5 \bullet 10^{-9} + 4 \bullet T_{VCO}\right)(\text{sec}) \bullet F_{comparison} \bullet I_{CP}\right), 0.25 \bullet I_{CP}\right] \quad \text{(EQ 9)}$$

where:

T_{VCO}*: is the RF period at the fractional prescaler input*

I_{CP}*: is the full scale current setting of the switching charge pump* Reg 09h*[6:0]* Reg 09h*[13:7]*

Operation with charge pump offset influences the required configuration of the Lock Detect function. Refer to the description of Lock Detect function in section 1.11. Note that this calculation can be performed for the center frequency of the VCO, and does not need refinement for small differences < 25 % in center frequencies.

Another factor in the spectral performance in Fractional Mode is the choice of the Delta-Sigma Modulator mode. Mode A can offer better in-band spectral performance (inside the loop bandwidth) while Mode B offers better out of band performance. See Reg 06h[3:2] for DSM mode selection. Finally, all fractional synthesizers create fractional spurs at some level. Hittite offers the lowest level fractional spurious in the industry in an integrated solution.

1.4.2.2 Spurious Related to Channel Step Size (Channel Spurs)

Many fractional PLLs also create spurious emissions at offsets which are multiples of the channel step size. We refer to these as Channel Spurs. It is common in the industry to set the channel step size by use of the so-called modulus. For example, channel step size of 100 kHz requires a small modulus related to the step size, and often results in 100 kHz Channel Spurs.

The HMC834LP6GE uses a large fixed modulus unrelated to the channel step size. As a result, the HMC834LP6GE has extremely low or unmeasurable Channel Spurs. In addition Exact Frequency Mode (1.12.2.2) allows exact channel step size with no Channel Spurs.

The lack of Channel Spurs means that the HMC834LP6GE has large regions of operation between Integer Boundaries with little or no spurs of any kind. Large spurious free zones enable the HMC834LP6GE to be used with a tunable reference, to effectively move the spur free zones and hence achieve spur-free operation at all frequencies. The resulting PLL is virtually spur-free at all frequencies.

For more information see 1.4.2.3.

1.4.2.3 Spurious Reduction with Tunable Reference

Section 1.4.2 discussed fractional mode Integer Boundary spurious caused by VCO operation near reference harmonics. It is possible, with Hittite fractional synthesizers, to virtually eliminate the integer boundary spurious at a given VCO frequency by changing the frequency of the reference. The reference frequency is normally generated by a crystal oscillator and is not tunable. However, Hittite wideband PLLs with Integrated VCOs, including HMC834LP6GE, can be used as a high-quality tunable reference source, as shown in Figure 33.

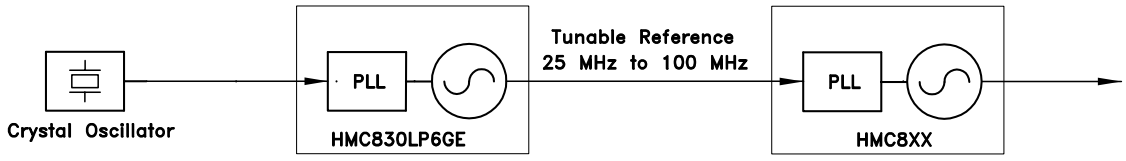

Figure 33. Tunable reference source

With the setup shown in Figure 33, the HMC834LP6GE is capable of operating across all of its frequency range without sacrificing phase noise, while virtually eliminating spurious emissions. Optimum operation requires appropriate configuration of the two synthesizers to achieve this performance. Hittite apps-support can assist with the required algorithms for ultra-low spurious tunable reference applications.

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An HMC830LP6GE tunable reference PLL typically uses a high frequency crystal reference for best performance. Phase noise from the MC830LP6GE tunable reference output at 100 kHz offset varies typically from -145 dBc at 100 MHz output to -157 dBc at 25 MHz output. This performance of HMC830LP6GE as a tunable reference is equivalent to the phase noise of high performance crystal oscillators.

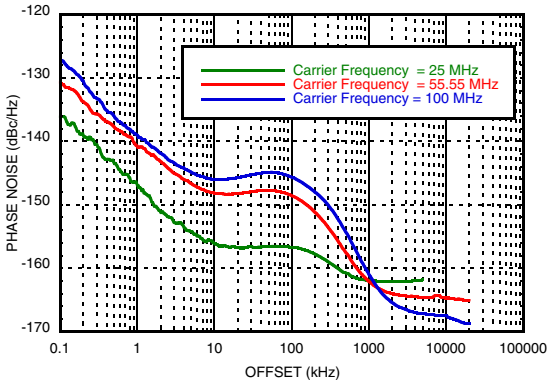

Figure 34. Phase noise performance of the HMC833LP6GE when used with a tunable reference source. (HMC833LP6GE operating at 3 GHz/30, 3 GHz/54, and 1.55 GHz/62 for the 100 MHz, 55.55 MHz, and 25 MHz curves respectively.)

Worst case spurious levels (largest spurs at any offset) of conventional fixed reference vs. a tunable reference can be compared by multiple individual phase noise measurements and summarized on a single plot vs. carrier frequency.

For example, Figure 35 shows the spectrum of a carrier operating at 2000.1 MHz with a 50 MHz fixed reference. This case is 100 kHz away from an Integer Boundary (50 MHz x 40). Worst case spurious can be observed at 100 kHz offset and about -52 dBc in magnitude.

Figure 36 shows the same HMC834LP6GE PLL VCO operating at the same 2000.1 MHz carrier frequency, using a tunable reference at 47.5 MHz generated by HMC830LP6GE. Worst case spurious in this case can be observed at 5 MHz offset and about -100 dBc in magnitude.

The results of Figure 35 and Figure 36 show that the tunable reference source achieves 50 dB better spurious performance, while maintaining essentially the same phase noise performance.

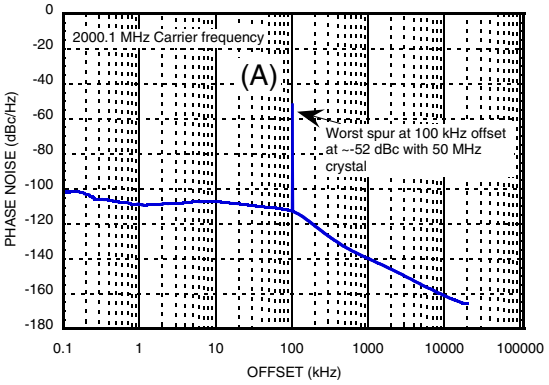

Figure 35. HMC834LP6GE Worst spur at any offset, fixed 50 MHz reference, output frequency = 2000.1 MHz

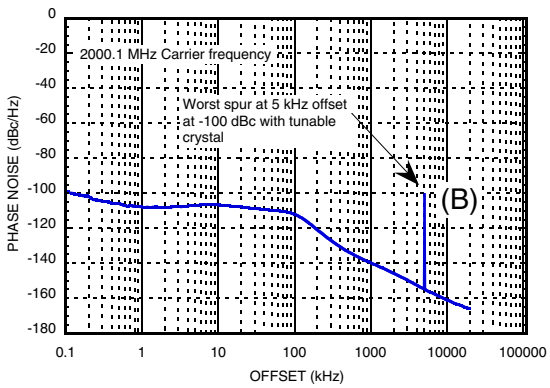

Figure 36. HMC834LP6GE worst spur at any offset, tunable reference (HMC830LP6GE), output frequency = 2000.1 MHz

Many spurious measurements, such as the ones in Figure 35 and Figure 36 can be summarized into a single plot of worst case spurious at any offset vs. carrier frequency as shown in Figure 37. A log frequency display relative to the 2000 MHz fixed reference Integer Boundary was used to emphasize the importance