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HMC852LC3C

v00.0610

28 Gbps, AND / NAND / OR / NOR GATE WITH PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC852LC3C is ideal for:

- Serial Data Transmission up to 28 Gbps
- Digital Logic Systems up to 28 Gbps
- NRZ-to-RZ/RH Conversion
- Differential Encoding
- DPSK & Duobinary Transmitter Modules
- Broadband Test & Measurement

Features

Inputs Terminated Internally in 50 Ohms

Differential or Single-Ended Operation

Fast Rise and Fall Times: 15 / 14 ps

Low Power Consumption: 241 mW typ.

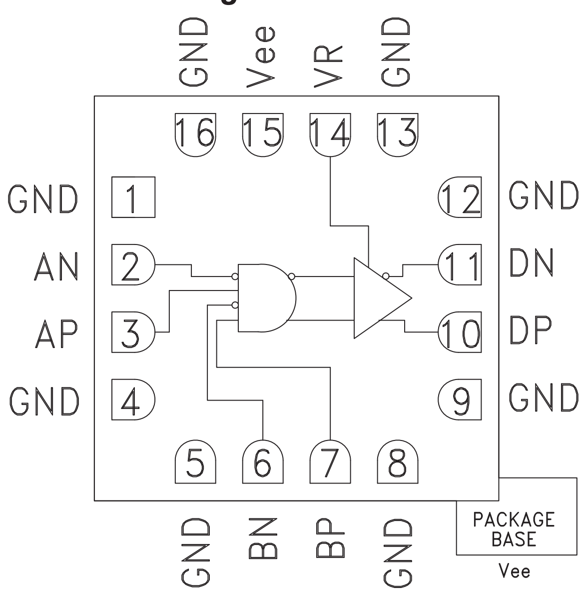
Programmable Differential
Output Voltage Swing: 600 - 1450 mVp-p

Propagation Delay: 98 ps

Single Supply: -3.3 V

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC852LC3C is an AND/NAND/OR/NOR gate function that is designed to support data transmission rates of up to 28 Gbps, and clock frequencies as high as 28 GHz.

All differential inputs to the HMC852LC3C are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. the HMC852LC3C also features an ouput level control pin, VR, which allows for loss compensation or signal level optimization. The HMC852LC3C operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vee = -3.3 V, VR = 0 V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			73		mA
Maximum Data Rate			28		Gbps
Maximum Clock Rate			28		GHz
Input Voltage Range		-1.5		0.5	V
Input Differential Voltage		0.1		2.0	Vp-p
Input Return Loss	Frequency <18 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		600		mVp-p
	Differential, peak-to-peak		1200		mVp-p
Output High Voltage			-25		mV

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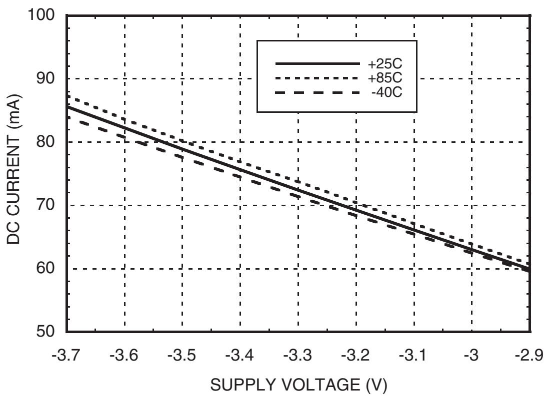
Electrical Specifications *(continued)*

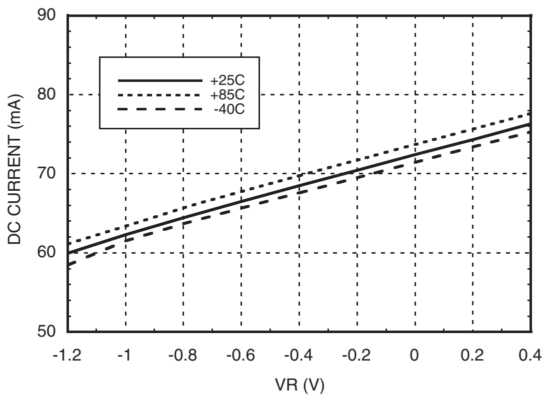
Parameter	Conditions	Min.	Typ.	Max	Units
Output Low Voltage			-625		mV
Output Rise / Fall Time	Differential, 20% - 80%		15 / 14		ps
Output Return Loss	Frequency <22 GHz		10		dB
Small Signal Gain			50		dB
Random Jitter Jr	rms		0.09	0.13	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		2		ps, p-p
Propagation Delay, A to D, Tpda			98		ps
Propagation Delay, B to D, Tpdb			98		ps
VR Pin Current	VR = 0.0 V		3		mA
VR Pin Current	VR = 0.4 V			4.25	mA

[1] Added jitter calculated by de-embedding the source's jitter at 13 Gbps, 2^{15} -1 PRBS input.

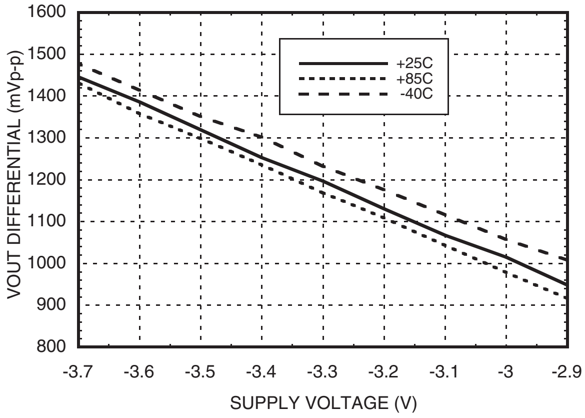
DC Current vs. Supply Voltage [1][2]



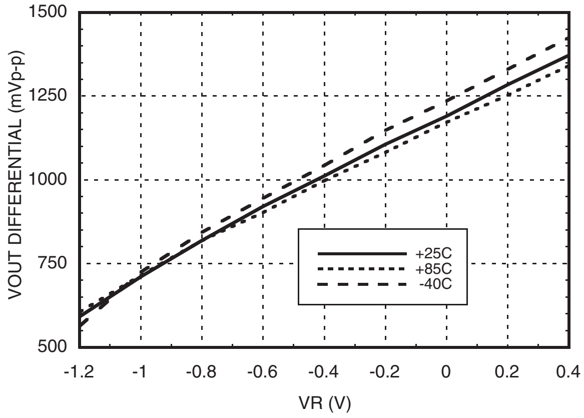
DC Current vs. VR [2][3]



Output Differential Voltage vs. Supply Voltage [1][2]



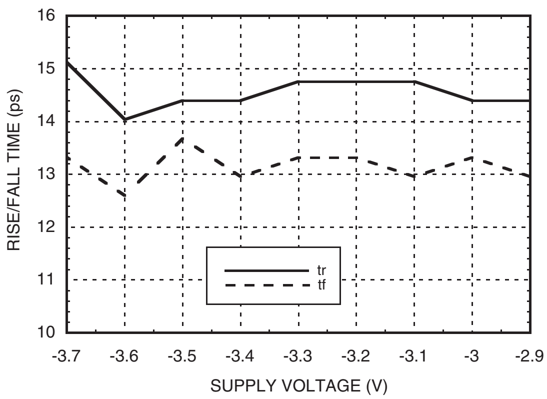
Output Differential Voltage vs. VR [2][3]



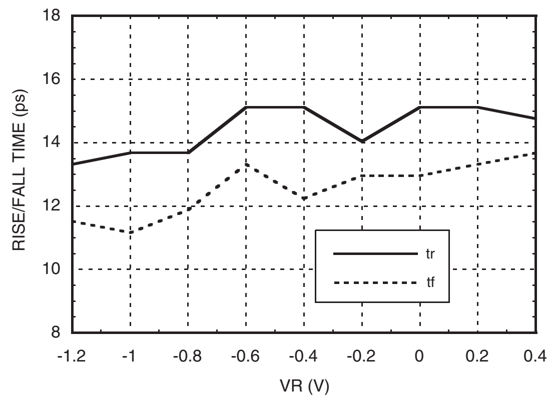
[1] VR = 0.0 V [2] Frequency = 28 GHz [3] Vee = -3.3 V

28 Gbps, AND / NAND / OR / NOR GATE WITH PROGRAMMABLE OUTPUT VOLTAGE

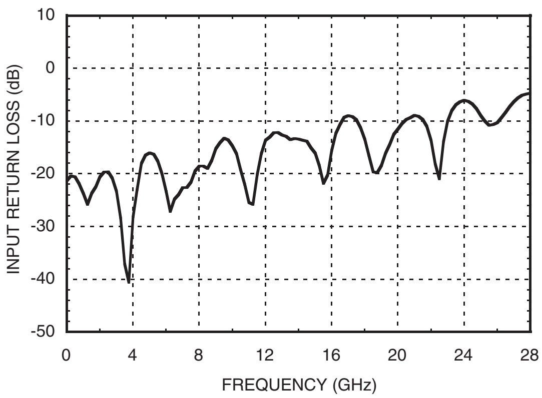
Rise / Fall Time vs. Supply Voltage [1][2]



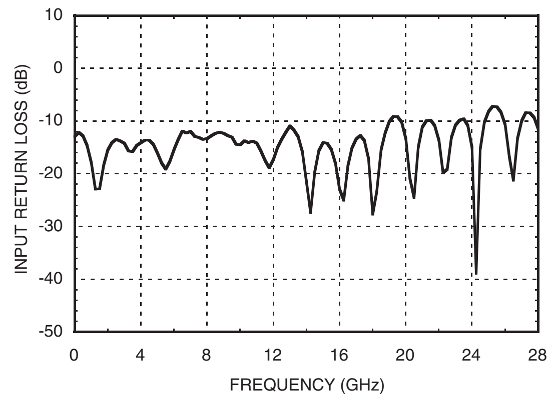
Rise / Fall Time vs. VR [2][3]



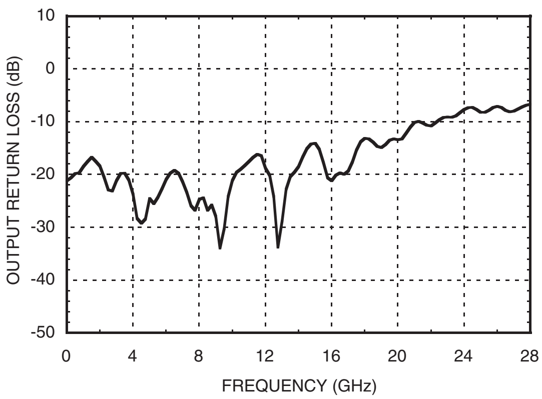
Input Return Loss Port A [1][3][5]



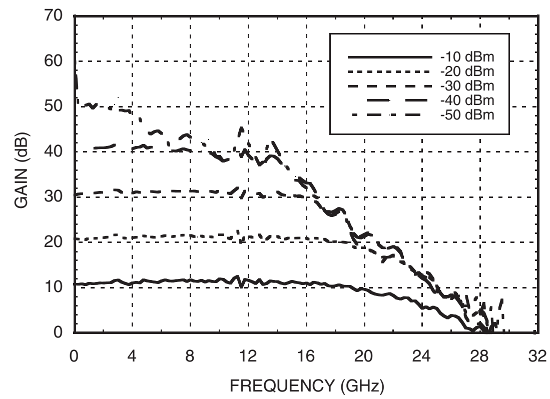
Input Return Loss Port B [1][3][5]



Output Return Loss [1][3][5]

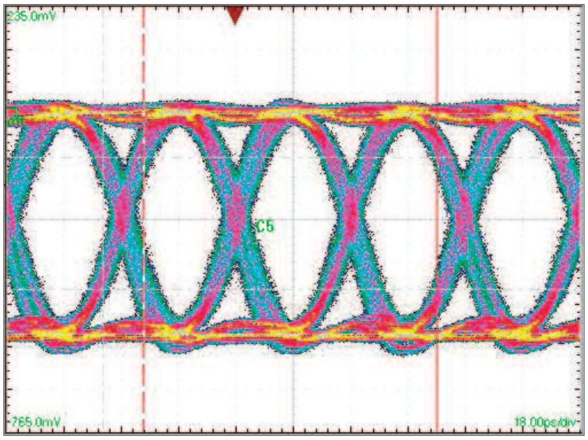


Response vs. Input Power [1][4][5]



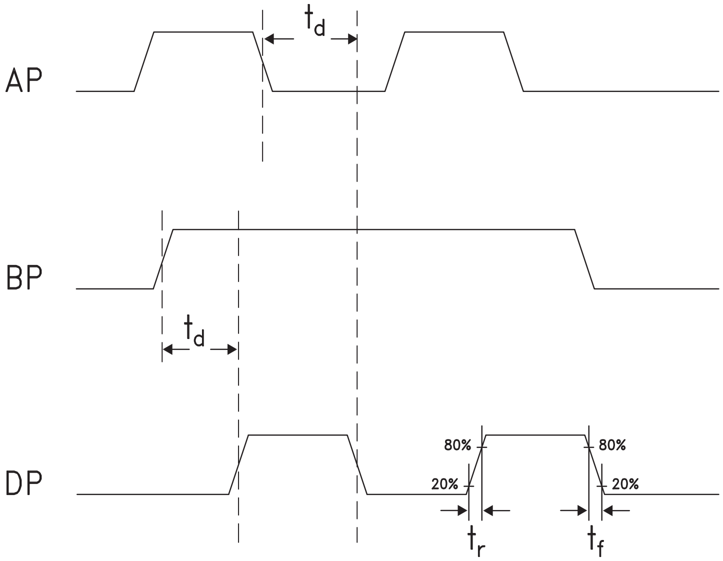
[1] VR = 0.0 V [2] Frequency = 28 GHz [3] Device measured on evaluation board with single-ended time domain gating.
[4] Device measured on evaluation board with single ended time domain port extensions [5] Vee = -3.3 V

Eye Diagram



[1] Test Conditions:
Single ended 400 mV data input. Pattern generated with 2^{15} -1 PN patterns applied to the inputs resulting in a Quasi-Periodic PRBS pattern at 28 Gbps. Measured using Tektronix CSA 8000.

Timing Diagram



Truth Table

Input		Outputs
A	B	D
L	L	L
L	H	L
H	L	L
H	H	H
Notes: A = AP - AN B = BP - BN D = DP - DN	H - Positive voltage level L - Negative voltage level	

28 Gbps, AND / NAND / OR / NOR GATE WITH PROGRAMMABLE OUTPUT VOLTAGE

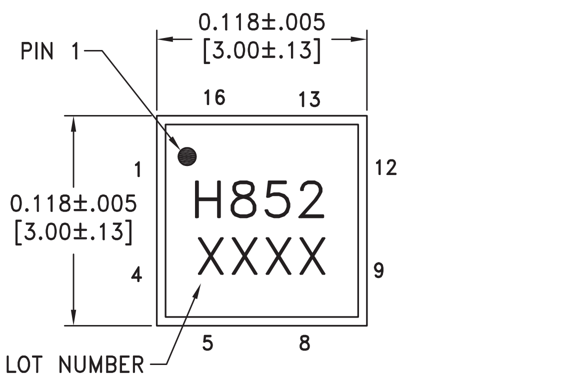
RoHS ✓ EARTH FRIENDLY

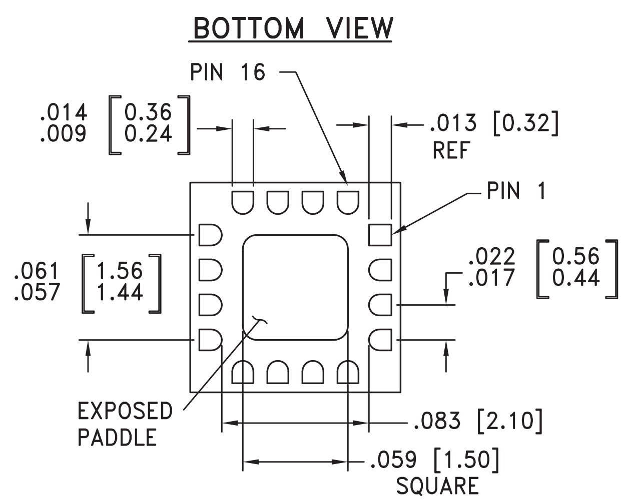
Absolute Maximum Ratings

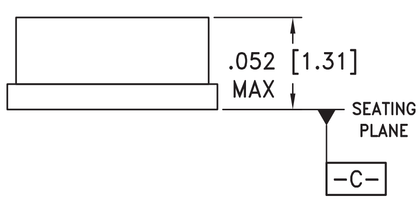
Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j-p}$) Worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing







NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

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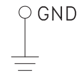
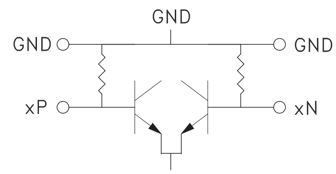
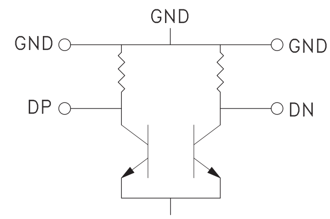
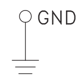
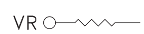
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3 6, 7	AN, AP BN, BP	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
10, 11	DP, DN	Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply.	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per "Output Differential vs. VR" plot.	
15, Package Base	Vee	This pin and the exposed paddle must be connected to the negative voltage supply.	

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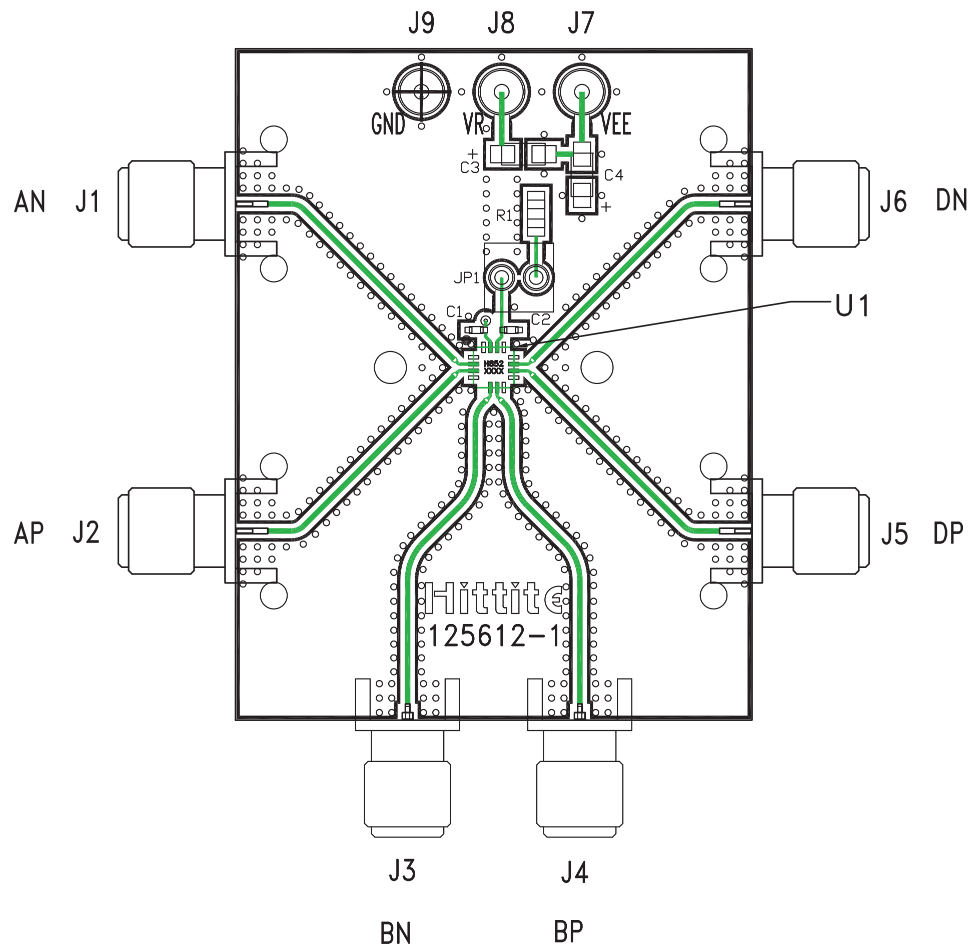
Evaluation PCB



List of Materials for Evaluation PCB 125614 [1]

Item	Description
J1 - J6	PCB Mount K RF Connectors
J7 - J9	DC Pin
JP1	0.1" Header with Shorting Jumper
C1, C2	100 pF Capacitor, 0402 Pkg.
C3, C4	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC852LC3C High Speed Logic, AND / NAND / OR / NOR Gate
PCB [2]	125612 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

Application Circuit