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...heet July 29, 2009 FN4643.4

NTSC/PAL Video Decoder

The HMP8117 is a high quality NTSC and PAL video decoder with internal A/D converters. It is compatible with NTSC M, PAL B, D, G, H, I, M, N, and combination N (N_C) video standards.

Both composite and S-video (Y/C) input formats are supported. A 2-line comb filter plus a user-selectable chrominance trap filter provide high quality Y/C separation. User adjustments include brightness, contrast, saturation, hue, and sharpness.

Vertical blanking interval (VBI) data, such as Closed Captioning, Wide Screen Signalling and Teletext, may be captured and output as BT.656 ancillary data. Closed Captioning and Wide Screen Signalling information may also be read out via the I^2C interface.

The Videolyzer™ feature provides approved Macrovision™ copy-protection bypass and detection.

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG DWG. #
HMP8117CN	HMP8117CN	0 to +70	80 Ld PQFP (Note 2)	Q80.14x20
HMP8117CNZ (Note 1)	HMP8117CNZ	0 to +70	80 Ld PQFP (Note 2) (Pb-free)	Q80.14x20
HMPVIDEVAL/ISA	Evaluation Board: ISA Frame Grabber (Note 3)			

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. PQFP is also known as QFP and MQFP.
3. Evaluation Board descriptions are in the Applications section.

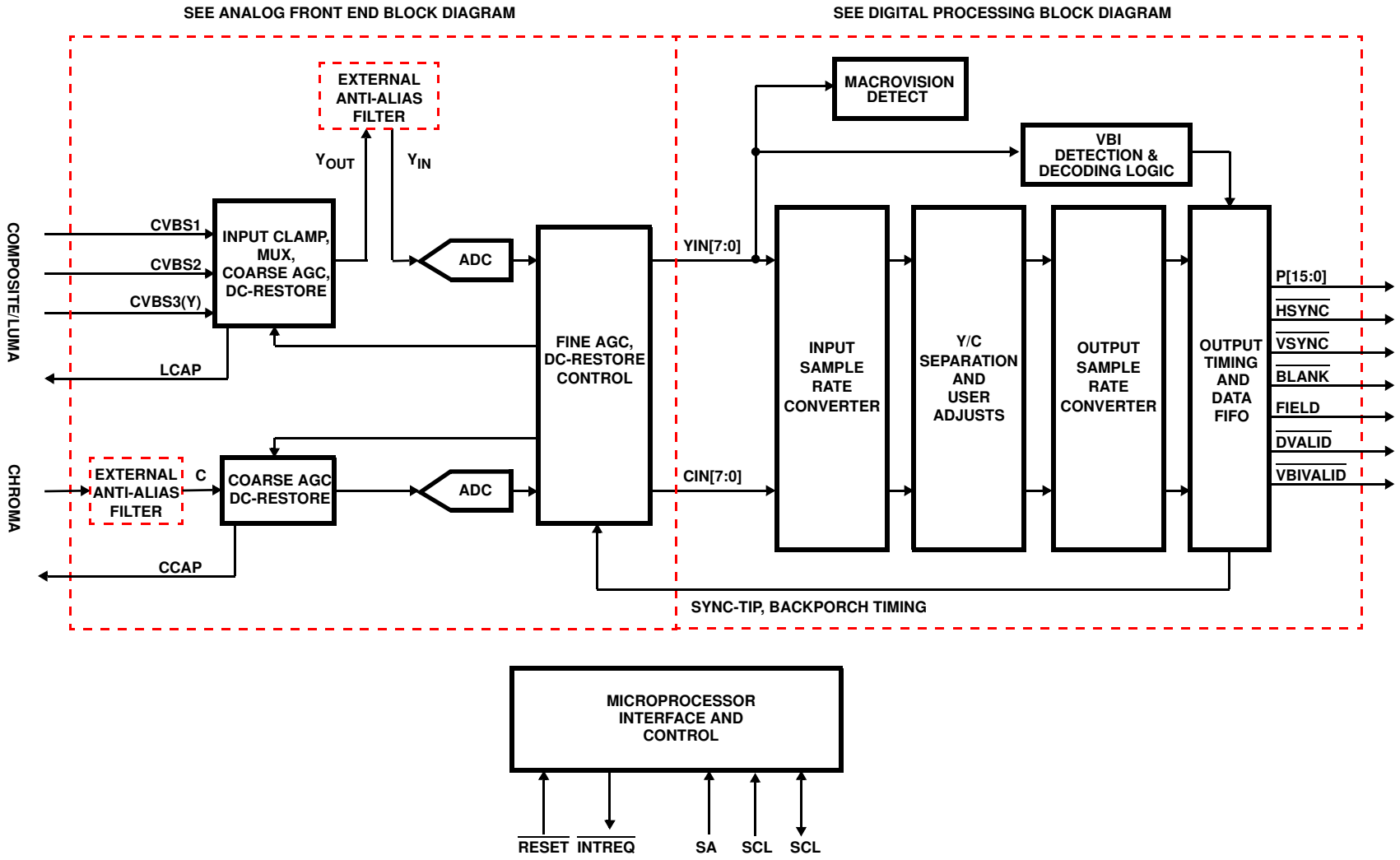
Features

- (M) NTSC and (B, D, G, H, I, M, N, N_C) PAL Operation
  - Optional Auto Detect of Video Standard
  - ITU-R BT.601 (CCIR601) and Square Pixel Operation
- Videolyzer Feature
  - Macrovision™ Bypass and Detection
- Digital Anti-Alias Filter
- Power Down Mode
- Digital Output Formats
  - VMI Compatible
  - 8-bit, 16-bit 4:2:2 YCbCr
  - 15-bit (5, 5, 5), 16-bit (5, 6, 5) RGB
  - Linear or Gamma-Corrected
  - 8-bit BT.656
- Analog Input Formats
  - Three Analog Composite Inputs
  - Analog Y/C (S-video) Input
- "Raw" (Oversampled) VBI Data Capture
- "Sliced" VBI Data Capture Capabilities
  - Closed Captioning
  - Widescreen Signalling (WSS)
  - BT.653 System B, C and D Teletext
  - North American Broadcast Teletext (NABTS)
  - World System Teletext (WST)
- 2-Line (1H) Comb Filter Y/C Separator
- Fast I^2C Interface
- Pb-Free Plus Anneal Available (RoHS Compliant)

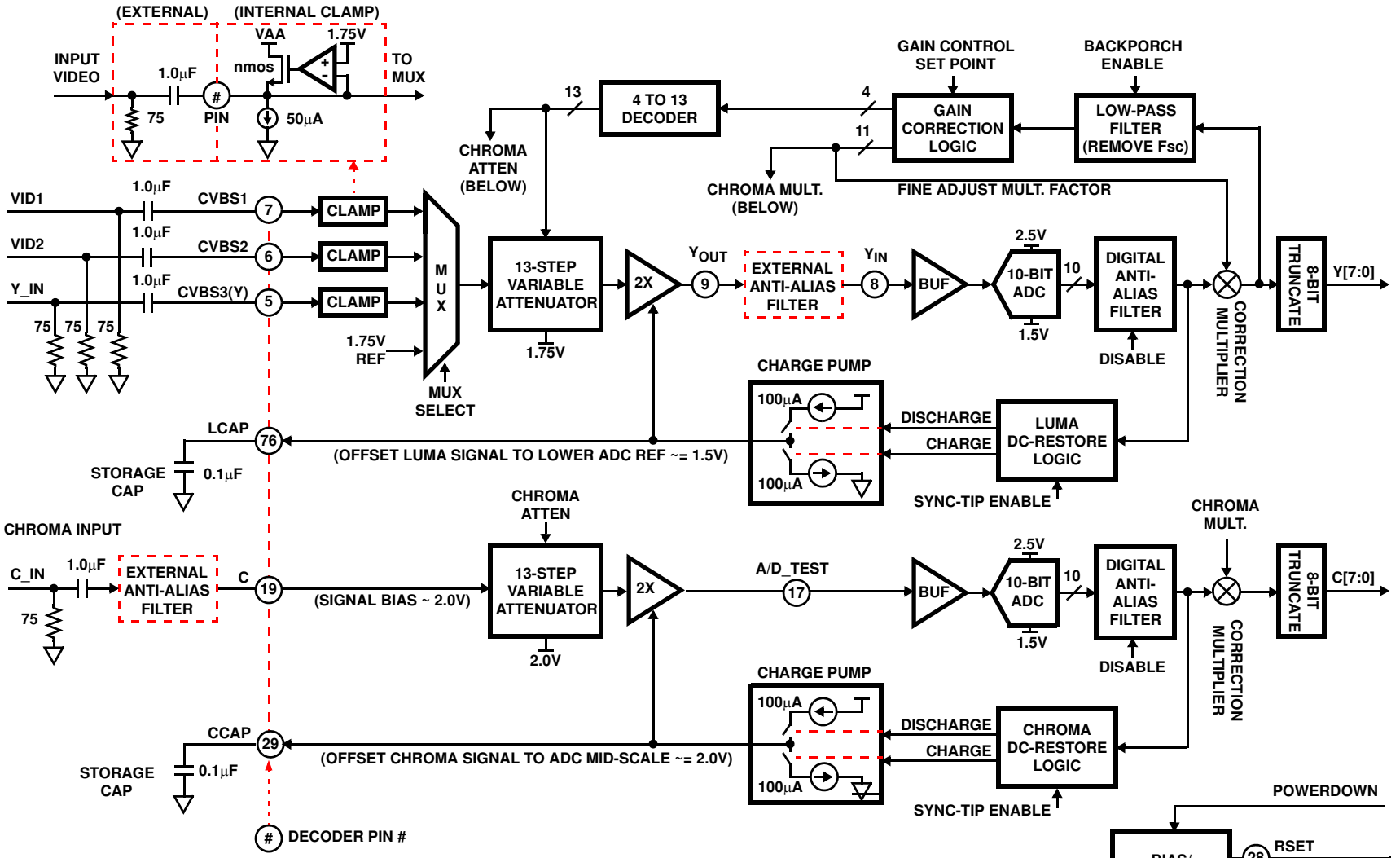
Applications

- Multimedia PCs
- Video Conferencing
- Video Compression Systems
- Video Security Systems
- LCD Projectors and Overhead Panels
- Related Products
  - NTSC/PAL Encoders: HMP8156, HMP8170

Functional Block Diagram



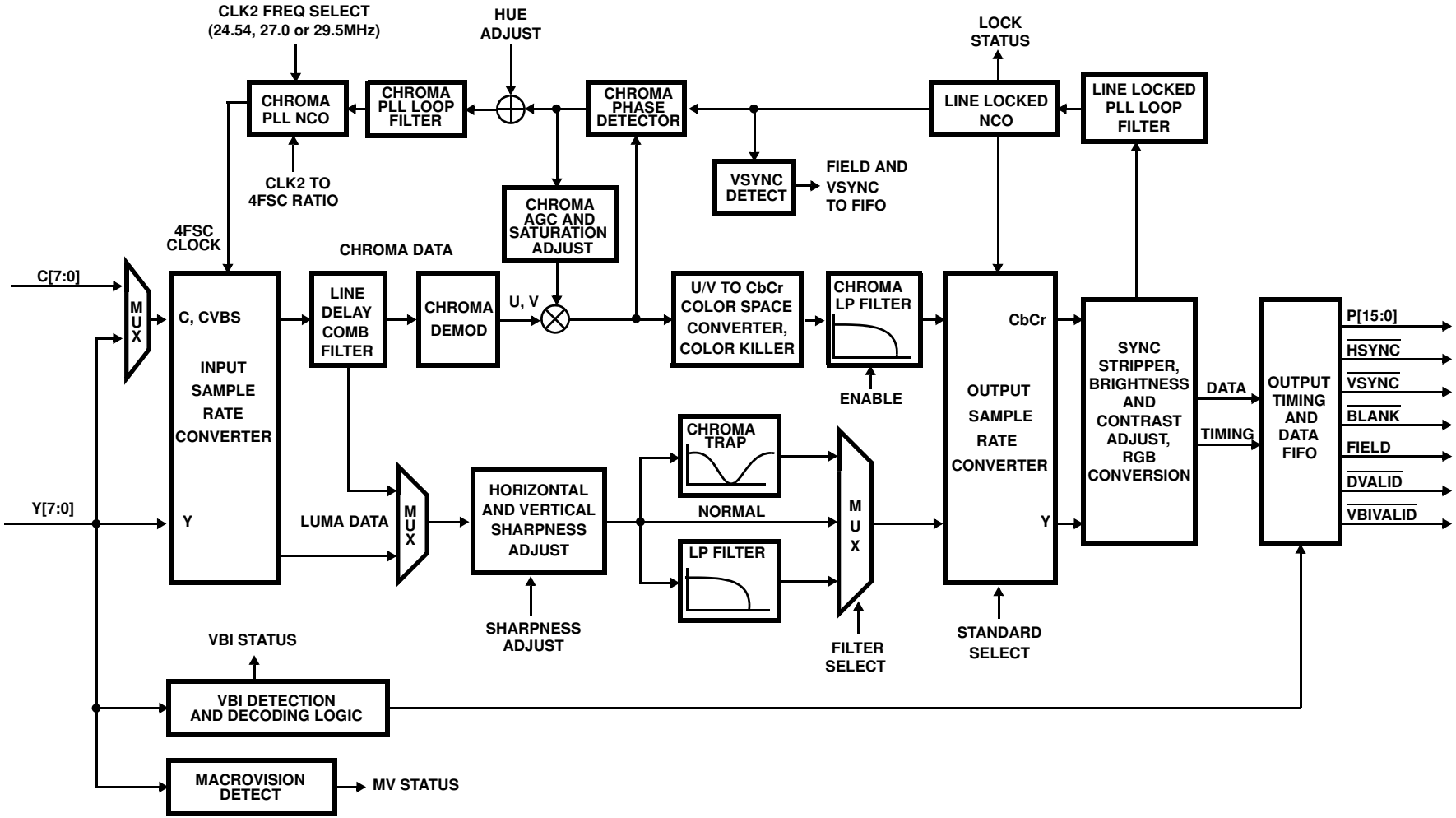
Analog Front End Block Diagram



PIN #	NOMINAL (NTSC) OPERATING CONDITION
5 6 7	CVBSX. SIZE = INPUT. SYNC TIP CLAMPED AT ~= 1.75 VDC.
9 8	Y_{OUT}/Y_{IN}. SIZE = ~1.0 V_{P-P}, SYNC TIP OFFSET ~= 1.5 VDC.
19	C. SIZE = INPUT SIZE. PORCH OFFSET ~= 2.0 VDC.
17	A/D_TEST. SIZE ~= F(LUMA AGC), PORCH OFFSET ~= 2.0VDC.

PIN #	NOMINAL (NTSC) OPERATING CONDITION
76	LCAP. DC-SIGNAL OFFSET ~= 2.4 VDC.
29	CCAP. DC-SIGNAL OFFSET ~= 2.4 VDC.
28	RSET. DC-SIGNAL OFFSET ~= 1.2 VDC.
78	REF_CAP. DC-SIGNAL OFFSET ~= 2.5 VDC.

Digital Processing Block Diagram



Introduction

The HMP8117 is designed to decode baseband composite or S-video NTSC and PAL signals, and convert them to either digital YCbCr or RGB data. In addition to performing the basic decoding operations, these devices include hardware to decode different types of VBI data and to generate full-screen blue, black and color bar patterns.

Digital PLLs are used to synchronize to all NTSC and PAL standards. A chroma PLL is used to maintain color lock for chroma demodulation while a line-locked PLL is used to maintain vertical spatial alignment. The PLLs are designed to maintain lock in the presence of VCR head switches, VCR trick-mode and multi-path noise.

The HMP8117 provides the Videolyzer feature for Macrovision (MV) copy-protection bypass and detection.

External Video Processing

Before a video signal can be digitized the decoder has some external processing considerations that need to be addressed. This section discusses those external aspects of the HMP8117.

Analog Video Inputs

The HMP8117 supports either three composite or two composite and one S-video input.

Three analog video inputs (CVBS 1-3) are used to select which one of three composite video sources are to be decoded. To support S-video applications, the Y channel drives the CVBS3(Y) analog input, and the C channel drives the C analog input.

The analog inputs must be AC-coupled to the video signals, as shown in the Applications section.

Anti-alias Filters

Although a 23 tap digital halfband anti-alias filter is provided for each A/D channel, an external passive filter is recommended for optimum performance. The digital filter has a flat response out to 5.4MHz with an approximate -3dB bandwidth of 6.3MHz using a 27MHz input CLK2 sample rate. For the CVBSx inputs, the filter is connected between the YOUT and YIN pins. For the C (chroma) input, the anti-alias filter should be connected before the C input. Recommended filter configurations are shown on the reference schematic in Figure 20. These filters have flat response out to 4.2MHz with an approximate -3dB bandwidth of 8MHz. If upgrading from the HMP8115 or HMP8112A, the previous filter configurations may be used but with slightly degraded bandwidth. Alternative higher or lower performance filters configurations may substituted.

Digitization of Video

Prior to A/D conversion, the input signal is offset and scaled to known video levels. After digitization, sample rate converters and a comb filter are used to perform color separation and demodulation.

A/D Conversion

Each CVBSX video input channel has a video clamp circuit that is independent of PLL timing. The input clamp provides a coarse signal offset to position the sync tip within the A/D converter sampling range so that the AGC and DC-RESTORE logic can operate.

A/D Conversion

Video data is sampled at the CLK2 frequency then processed by the input sample rate converter. The output levels of the ADC after AGC and DC restoration processing are:

	(M) NTSC (M, N) PAL	(B, D, G, H, I, N_C) PAL
white	196	196
black	66	59
blank	56	59
sync	0	0

AGC and DC Restoration

The AGC amplifier attenuates or amplifies the analog video signal to ensure that the blank level generates code 56 or 59 depending on the video standard. The difference from the ideal blank level of 56 or 59 is used to control the amount of attenuation or gain of the analog video signal. To obtain a stable DC reference for the AGC, a digital low-pass filter removes the chroma burst from the input signal's backporch.

DC restoration positions the video signal so that the sync tip generates a code 0. The internal timing windows for AGC and DC restoration are show in Figure 3. The appropriate windows are automatically determined by the decoder when the input signal is auto-detected or manually selected.

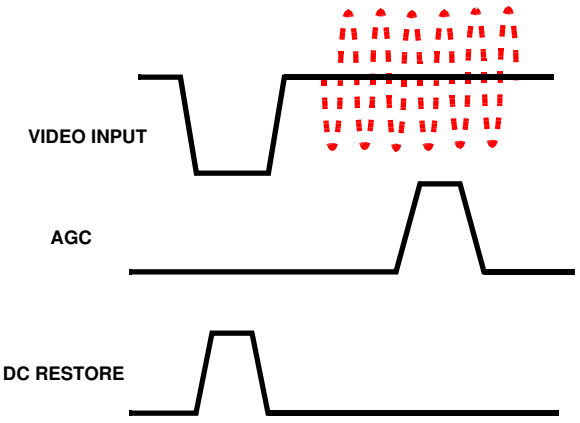


FIGURE 1. AGC AND DC RESTORE INTERNAL TIMING

Input Signal Detection

If no input video signal is detected for 16 consecutive line periods, nominal video timing is generated for the previously detected or programmed video standard. A maskable interrupt is provided for the condition of “Input Signal Loss” allowing the host to enable blue field output if desired.

Vertical Sync and Field Detection

The vertical sync and field detect circuit uses a low time counter to detect the vertical sync sequence in the video data stream. The low time counter accumulates the low time encountered during any sync pulse, including serration and equalization pulses. When the low time count exceeds the vertical sync detect threshold, $\overline{\text{VSYNC}}$ is asserted immediately. FIELD is asserted at the same time that $\overline{\text{VSYNC}}$ is asserted. FIELD is asserted low for odd fields and high for even fields. Field is determined from the location in the video line where VSYNC is detected. If VSYNC is detected in the first half of the line, the field is odd. If VSYNC is detected in the second half of a line, the field is even.

In the case of lost vertical sync or excessive noise that would prevent the detection of vertical sync, the FIELD output will continue to toggle. Lost vertical sync is declared if after 337 lines, a vertical sync period was not detected for 1 or 3 (selectable) successive fields as specified by bit 2 of the GENLOCK CONTROL register 04_H. When this occurs, the PLLs are initialized to the acquisition state.

Y/C Separation

A composite video signal has the luma (Y) and chroma (C) information mixed in the same video signal. The Y/C separation process is responsible for separating the composite video signal into these two components. The HMP8117 utilizes a comb filter to minimize the artifacts that are associated with the Y/C separation process.

Input Sample Rate Converter

The input sample rate converter is used to convert video data sampled at the CLK2 rate to a virtual $4xf_{SC}$ sample rate for comb filtering and color demodulation. An interpolating filter is used to generate the $4xf_{SC}$ samples as illustrated in Figure 2.

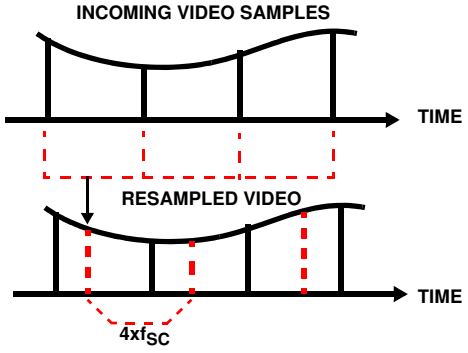


FIGURE 2. SAMPLE RATE CONVERSION

Comb Filter

A 2-line comb filter, using a single line delay, is used to perform part of the Y/C separation process. During S-video operation, the Y signal bypasses the comb filter; the C signal is processed by the comb filter since it is an integral part of the chroma demodulator. During PAL operation, the chroma trap filter should also be enabled for improved performance.

Since a single line store is used, the chroma will normally have a half-line vertical offset from the luma data. This may be eliminated, vertically aligning the chroma and luma samples, at the expense of vertical resolution of the luma. Bit 0 of the OUTPUT FORMAT register 02_H controls this option.

Chroma Demodulation

The output of the comb filter is further processed using a patented frequency domain transform to complete the Y/C separation and demodulate the chrominance.

Demodulation is done at a virtual $4xf_{SC}$ sample rate using the interpolated data samples to generate U and V data. The demodulation process decimates by 2 the U/V sample rate.

Output Sample Rate Converter

The output sample rate converter converts the Y, U and V data from a virtual $4xf_{SC}$ sample rate to the desired output sample rate (i.e., 13.5MHz). It also vertically aligns the samples based on the horizontal sync information embedded in the digital video data stream. The output sample rate is determined by the input video standard and the selected rectangular/square pixel mode. The output pixel rate is 1/2 of the CLK2 input clock frequency. The output format is 4:2:2 for all modes except the RGB modes which use a 4:4:4 output format.

CLK2 Input

The decoder requires a stable clock source for the CLK2 input. For best performance, use termination resistor(s) to minimize pulse overshoot and reflections on the CLK2 input. Since chroma demodulation uses the virtual $4xf_{SC}$, any jitter on CLK2 will be transferred as chrominance error on the output pixels. The CLK2 clock frequency must be one of the valid selections from Table 1 below based on the video standard and desired pixel mode.

TABLE 1. VIDEO STANDARD CLOCK RATE SELECTION SUMMARY

VIDEO FORMAT	VALID CLK2 FREQUENCIES (MHz)	
	RECTANGULAR PIXEL MODE	SQUARE PIXEL MODE
(M) NTSC, (M) PAL	27.00	24.54
(B, D, G, H, I, N, N_C) PAL	27.00	29.50

The CLK2 should be derived from a stable clock source, such as a crystal. CLK2 must have at least a ±50ppm accuracy and at least a 60/40% duty cycle to ensure proper

operation. Use of a PLL to generate a “Line Locked” CLK2 input based on the input video is not recommend. (See the following section.)

Cycle Slipping and Real-Time Pixel Jitter

The decoder’s digital PLL allows it to maintain lock and provide high quality Y/C separation even on the poorest quality input video signals. However, this architecture does not provide a “Line Lock Clock” output and should not be used as a timing master for direct interface to another video encoder in a system.

Since the decoder uses a fixed CLK2 input frequency, the output pixel rate must be periodically adjusted to compensate for any frequency error between CLK2 and the input video signal. This output pixel rate adjustment is referred to as cycle slipping. Since the decoder has an output data FIFO, all cycle slipping can be deferred until the next horizontal blanking interval. This guarantees a consistent number of pixels during the active video region.

Due to cycle slipping, the output timing and data will exhibit a nominal real-time (line-to-line) pixel jitter of one CLK2 period. Although the sample rate converter maintains a 1/8 pixel vertical sample alignment, the output data must be routed to a frame buffer or video compression chip in order remove the effects of cycle slipping. (The frame buffer or compression chip serves as a time base corrector.)

By directly interfacing the decoder to a video encoder, the output video signal will directly reflect the real-time pixel jitter effects of the decoder output timing. The jitter effects can be visualized on a CRT monitor using a static image containing patterns with sharp vertical edges. The edges will appear more “ragged” when compared to the input video signal. The severity of this visual effect relates directly to the frequency error between CLK2 and the input video signal. It is nearly impossible to completely match CLK2 with the input video signal. Therefore, a direct decoder to encoder interface is not recommended.

The use of an external PLL to generate a “Line Locked” CLK2 input derived from the input video signal is also not recommended, since this will defeat the internal digital PLL and result in pixel decoding errors.

Digital Processing of Video

Once the luma and chroma have been separated the HMP8117 then performs programmable modifications (i.e. contrast, coring, color space conversions, color AGC, etc.) to the decoded video signal.

UV to CbCr Conversion

The baseband U and V signals are scaled and offset to generate a nominal range of 16-240 for both the Cb and Cr data.

Digital Color Gain Control

There are four types of color gain control modes available: no gain control, automatic gain control, fixed gain control, and freeze automatic gain control.

If “no gain control” is selected, the amplitude of the color difference signals (CbCr) is not modified, regardless of variations in the color burst amplitude. Thus, a gain of 1x is always used for Cb and Cr.

If “automatic gain control” is selected, the amplitude of the color difference signals (CbCr) is compensated for variations in the color burst amplitude. The burst amplitude is averaged with the two previous lines having a color burst to limit line-to-line variations. A gain of 0.5x to 4x is used for Cb and Cr.

If “fixed gain control” is selected, the amplitude of the color difference signals (CbCr) is multiplied by a constant, regardless of variations in the color burst amplitude. The constant gain value is specified by the COLOR GAIN register $1C_H$. A gain of 0.5x to 4x is used for Cb and Cr. Limiting the gain to 4x limits the amount of amplified noise.

If “freeze automatic gain control” is selected, the amplitude of the color difference signals (CbCr) is multiplied by a constant. This constant is the value the AGC circuitry generated when the “freeze automatic gain” command was selected.

Color Killer

If “enable color killer” is selected, the color output is turned off when the running average of the color burst amplitude is below approximately 25% of nominal for four consecutive fields. When the running average of the color burst amplitude is above approximately 25% of nominal for four consecutive fields, the color output is turned on. The color output is also turned off when excessive phase error of the chroma PLL is present.

If “force color off” is selected, color information is never present on the outputs.

If “force color on” is selected, color information is present on the outputs regardless of the color burst amplitude or chroma PLL phase error.

Y Processing

The black level is subtracted from the luminance data to remove sync and any blanking pedestal information. Negative values of Y are supported at this point to allow proper decoding of “below black” luminance levels.

Scaling is done to position black at 8-bit code 0 and white at 8-bit code 219.

A chroma trap filter may be used to remove any residual color subcarrier from the luminance data. The center frequency of the chroma trap is automatically determined from the video standard being decoded. The chroma trap should be disabled during S-video operation to maintain maximum luminance bandwidth. Alternately, a 3MHz low-pass filter may be used to

remove high-frequency Y data. This may make a noisy image more pleasing to the user, although softer.

Coring of the high-frequency Y data may be done to reduce low-level high frequency noise.

Coring of the Y data may also be done to reduce low-level noise around black. This forces Y data with the following values to a value of 0:

coring = 1: ± 1
coring = 2: ± 1, ± 2
coring = 3: ± 1, ± 2. ± 3

High-frequency components of the luminance signal may be "peaked" to control the sharpness of the image. Maximum gain may be selected to occur at either 2.6MHz or the color subcarrier frequency. This may be used to make the displayed image more pleasing to the user. It should not be used if the output video will be compressed, as the circuit introduces high-frequency components that will reduce the compression ratio.

The brightness control adds or subtracts a user-specified DC offset to the Y data. The contrast control multiplies the Y data by a user-specified amount. These may be used to make the displayed image more pleasing to the user.

Finally, a value of 16 is added to generate a nominal range of 16 (black) to 235 (white).

CbCr Processing

The CbCr data is low-pass filtered to either 0.85MHz or 1.5MHz.

Coring of the CbCr data may be done to reduce low-level noise around zero. This forces CbCr data with the following values to a value of 128.

coring = 1: 127, 129
coring = 2: 126, 127, 129, 130
coring = 3: 125, 126, 127, 129, 130, 131

The saturation control multiplies the CbCr data by a user-specified amount. This may be used to make the displayed image more pleasing to the user. The CbCr data may also be optionally multiplied by the contrast value to avoid color shifts when changing contrast.

The hue control provides a user-specified phase offset to the color subcarrier during decoding. This may be used to correct slight hue errors due to transmission.

YCbCr Output Format Processing

Y has a nominal range of 16 to 235. Cb and Cr have a nominal range of 16 to 240, with 128 corresponding to zero. Values less than 1 are made 1 and values greater than 254 are made 254.

While $\overline{\text{BLANK}}$ is asserted, Y is forced to have a value of 16, with Cb and Cr forced to have a value of 128, unless VBI data is present.

RGB Output Format Processing

The 4:2:2 YCbCr data is converted to 4:4:4 YCbCr data and then converted to either 15-bit or 16-bit gamma-corrected RGB (R′G′B′) data. While $\overline{\text{BLANK}}$ is asserted, RGB data is forced to a value of 0.

15-Bit R′G′B′

The following YCbCr to R′G′B′ equations are used to maintain the proper black and white levels:

R′ = 0.142(Y - 16) + 0.194(Cr - 128)
G′ = 0.142(Y - 16) - 0.099(Cr - 128) - 0.048(Cb - 128)
B′ = 0.142(Y - 16) + 0.245(Cb - 128)

The resulting 15-bit R′G′B′ data has a range of 0 to 31. Values less than 0 are made 0 and values greater than 31 are made 31.

The 15-bit R′G′B′ data may be converted to 15-bit linear RGB, using the following equations. Although the PAL specifications specify a gamma of 2.8, a gamma of 2.2 is normally used. The HMP8117 allows the selection of the gamma to be either 2.2 or 2.8, independent of the video standard.

for gamma = 2.2:

for R′G′B′ < 0.0812*31
R = (31)((R′/31)/4.5)
G = (31)((G′/31)/4.5)
B = (31)((B′/31)/4.5)

for R′G′B′ >= 0.0812*31
$R = (31)(((R'/31) + 0.099)/1.099)^{2.2}$
$G = (31)(((G'/31) + 0.099)/1.099)^{2.2}$
$B = (31)(((B'/31) + 0.099)/1.099)^{2.2}$

for gamma = 2.8:

$R = (31)(R'/31)^{2.8}$
$G = (31)(G'/31)^{2.8}$
$B = (31)(B'/31)^{2.8}$

16-Bit R′G′B′

The following YCbCr to R′G′B′ equations are used to maintain the proper black and white levels:

R′ = 0.142(Y - 16) + 0.194(Cr - 128)
G′ = 0.288(Y - 16) - 0.201(Cr - 128) - 0.097(Cb - 128)
B′ = 0.142(Y - 16) + 0.245(Cb - 128)

The resulting 16-bit R′G′B′ data has a range of 0 to 31 for R′ and B′, and a range of 0 to 63 for G′. Values less than 0 are made 0; R′ and B′ values greater than 31 are made 31, G′ values greater than 63 are made 63.

The 16-bit R′G′B′ data may be converted to 16-bit linear RGB, using the following equations. Although the PAL specifications specify a gamma of 2.8, a gamma of 2.2 is normally used. The HMP8117 allows the selection of the gamma to be either 2.2 or 2.8, independent of the video standard.

for gamma = 2.2:

for R′B′ < 0.0812*31, G′ < 0.0812*63

R = (31)((R′/31)/4.5)

G = (63)((G′/63)/4.5)

B = (31)((B′/31)/4.5)

for R′B′ >= 0.0812*31, G′ >= 0.0812*63

$R = (31)(((R'/31) + 0.099)/1.099)^{2.2}$

$G = (63)(((G'/63) + 0.099)/1.099)^{2.2}$

$B = (31)(((B'/31) + 0.099)/1.099)^{2.2}$

for gamma = 2.8:

$R = (31)(R'/31)^{2.8}$

$G = (63)(G'/63)^{2.8}$

$B = (31)(B'/31)^{2.8}$

Built-in Video Generation

The decoder can be configured to output a full-screen of built-in blue, black or 75% color bar patterns. The type of pattern generated is determined by bits 2-1 of the OUTPUT FORMAT register 02_H. When built-in video generation is not desired, the bits need to be set for normal operation to pass decoded video.

If the decoder is currently locked to a video source on the input, the output data timing will be based on the input video source. If an input video source is not detected, internally-generated output data timing will be used. The following table lists the data codes output for each built-in video pattern in YCbCr format.

TABLE 2. BUILT-IN VIDEO PATTERN DATA CODES

PATTERN: COLOR	Y	Cb	Cr
75% Color Bar: White	$B4_H$	80_H	80_H
Yellow	$A2_H$	$2C_H$	$8E_H$
Cyan	83_H	$9C_H$	$2C_H$
Green	70_H	48_H	$3A_H$
Magenta	54_H	$B8_H$	$C6_H$
Red	41_H	64_H	$D4_H$
Blue	23_H	$D4_H$	72_H
Black	10_H	80_H	80_H
Blue Screen: Blue	$4B_H$	$D9_H$	88_H
Black Screen: Black	10_H	80_H	80_H

Pixel Port Timing

The the timing and format of the output data and control signals is presented in the following sections. Refer to the section “CYCLE SLIPPING AND REAL-TIME PIXEL JITTER” for PLL and interface considerations.

$\overline{HSYNC}$ and $\overline{VSYNC}$ Timing

The $\overline{HSYNC}$ and $\overline{VSYNC}$ output timing is VMI v1.4 compatible. Figures 3-6 illustrate the video timing. The leading edge of $\overline{HSYNC}$ is synchronous to the video input signal and has a fixed latency due to internal pipeline processing. The pulse width of the $\overline{HSYNC}$ is defined by the END HSYNC register 36_H, where the trailing edge of $\overline{HSYNC}$ has a programmable delay of 0-510 CLK2 cycles from the leading edge.

The leading edge of $\overline{VSYNC}$ is asserted approximately half way through the first serration pulse of each field. An accumulator is used to detect a low-time period within the serration pulse. Since the leading edge of $\overline{VSYNC}$ is detected, it should not be used for timing with respect to $\overline{HSYNC}$ or $\overline{BLANK}$.

The trailing edge of $\overline{VSYNC}$ implements the VMI handshake with $\overline{HSYNC}$ in order to determine field information without using the FIELD pin. For an odd field, the trailing edge of $\overline{VSYNC}$ is 5 ±1 CLK2 cycles after the trailing edge of the $\overline{HSYNC}$ that follows the last equalization pulse. Refer to Figures 3 and 5. For an even field, the trailing edge of $\overline{VSYNC}$ is 5 ±1 CLK2 cycles after the leading edge of the $\overline{HSYNC}$ that follows the last equalization pulse. Refer to Figures 4 and 6.

Field Timing

When field information can be determined from the input video source, the FIELD output pin reflects the video source field state. When field information cannot be determined from the input video source, the FIELD output pin alternates its state at the beginning of each field. FIELD changes state 5±1 CLK2 cycles before the leading edge of $\overline{VSYNC}$.

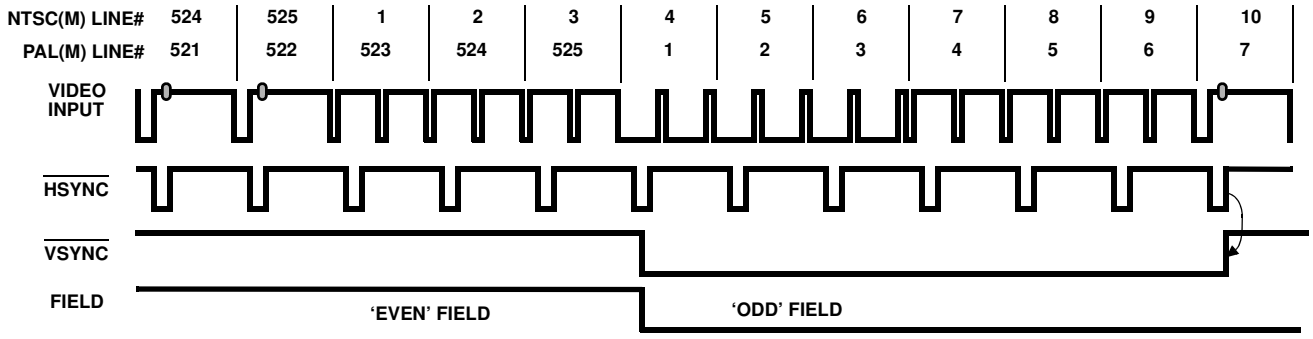


FIGURE 3. NTSC(M) AND PAL(M) ODD FIELD TIMING

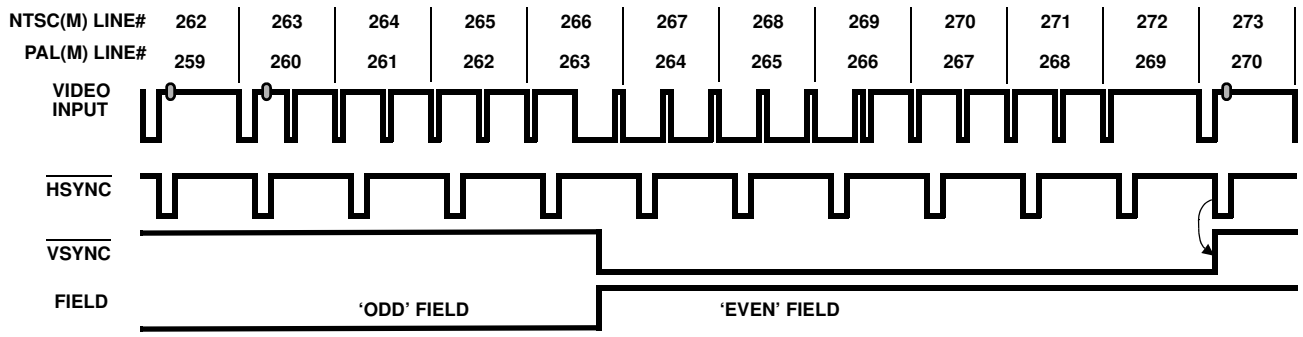


FIGURE 4. NTSC(M) AND PAL(M) EVEN FIELD TIMING

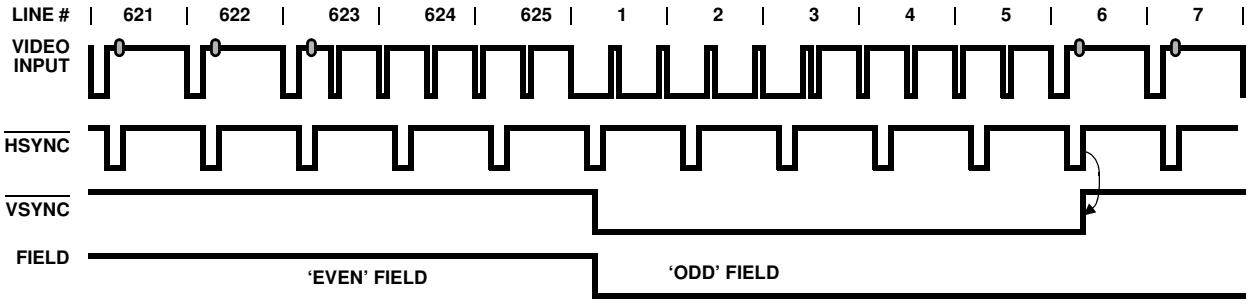


FIGURE 5. PAL(B, D, G, H, I, N, N_C) ODD FIELD TIMING

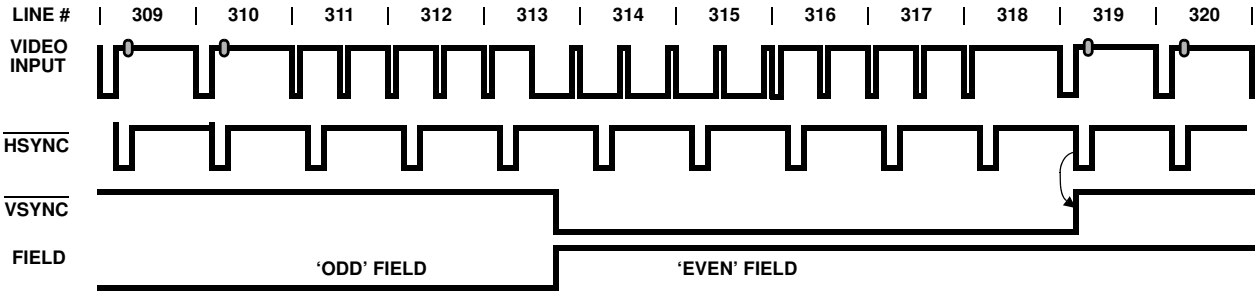


FIGURE 6. PAL(B, D, G, H, I, N, N_C) EVEN FIELD TIMING

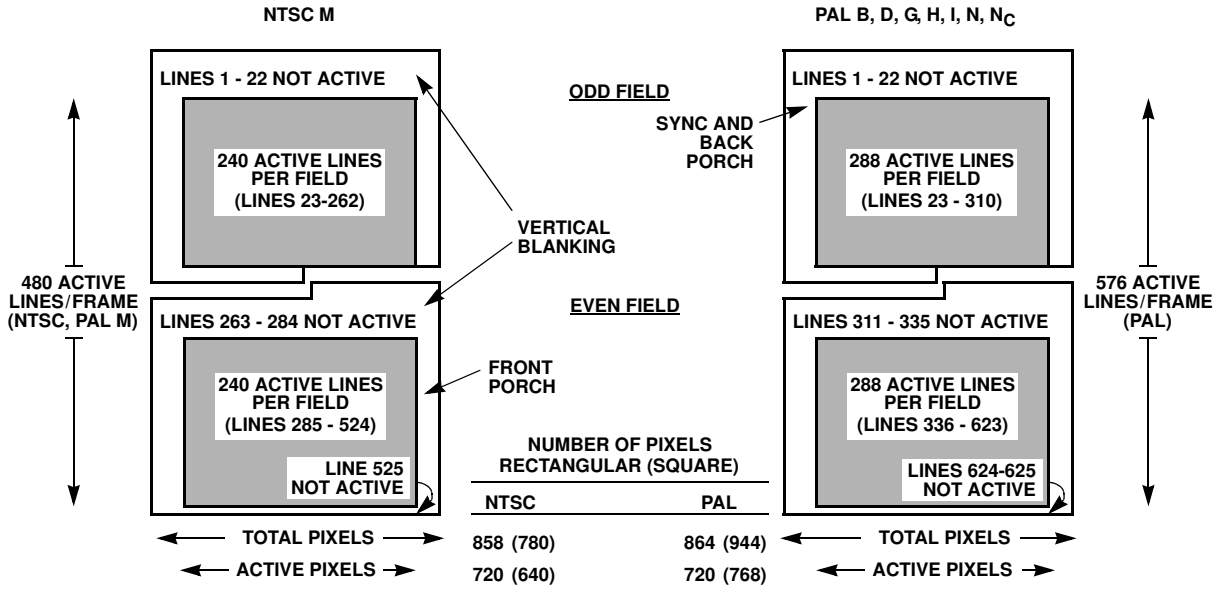
$\overline{\text{BLANK}}$ and $\overline{\text{DVALID}}$ Timing

$\overline{\text{DVALID}}$ is asserted when P15-P0 contain valid data. The behavior of the $\overline{\text{DVALID}}$ output is determined by bit 4 (DVLD_LTC) and bit 5 (DLVD_DCYC) of the GENLOCK CONTROL register 04_H for each video output mode.

The $\overline{\text{BLANK}}$ output pin is used to distinguish the blanking interval period from active video data. The blanking intervals are programmable in both horizontal and vertical dimensions. Reference Figure 7 for active video timing and use Table 3 for typical blanking programming values.

During active scan lines, $\overline{\text{BLANK}}$ is asserted when the horizontal pixel count matches the value in the START H_BLANK register $31_H/30_H$. The pixel counter is 000_H at the leading edge of the sync tip after a fixed pipeline delay. Since blanking normally occurs on the front porch, (prior to count 000H) the START H_BLANK count must be programmed with a large value from the previous line. Refer to the Last Pixel Count from Table 3. $\overline{\text{BLANK}}$ is negated when the horizontal pixel count matches the value in the END H_BLANK register 32_H. Note that horizontally, $\overline{\text{BLANK}}$ is programmable with two pixel resolution.

START V_BLANK register $34_H/33_H$ and END V_BLANK register 35_H determine which scan lines are blanked for each field. During inactive scan lines, $\overline{\text{BLANK}}$ is asserted during the entire scan line. Half-line blanking of the output video cannot be done.



NOTE:

4. The line numbering for PAL (M) is the NTSC (M) line count minus 3 per the video standards.

FIGURE 7. TYPICAL ACTIVE VIDEO REGIONS

TABLE 3. TYPICAL VALUES FOR H_BLANK AND V_BLANK REGISTERS

VIDEO STANDARD (MSB/LSB)	ACTIVE PIXELS/ LINE	TOTAL PIXELS/ LINE	LAST PIXEL COUNT	START H_BLANK (31H/30H)	END H_BLANK (32H)	START V_BLANK (34H/33H)	END V_BLANK (35H)
RECTANGULAR PIXELS							
NTSC (M), PAL (M)	720	858	857 (0359_H)	842 ($034A_H$)	122 ($7A_H$)	259 (0103_H)	19 (13_H)
PAL (B, D, G, H, I, N, N_C)	720	864	863 ($035F_H$)	852 (0354_H)	132 (84_H)	310 (0136_H)	22 (16_H)
SQUARE PIXELS							
NTSC (M), PAL (M)	640	780	779 ($030B_H$)	758 ($02F6_H$)	118 (76_H)	259 (0103_H)	19 (13_H)
PAL (B, D, G, H, I, N, N_C)	768	944	943 ($03AF_H$)	922 ($039A_H$)	154 ($9A_H$)	310 (0136_H)	22 (16_H)

TABLE 4. PIXEL OUTPUT FORMATS

PIN NAME	8-BIT, 4:2:2, YCbCr	16-BIT, 4:2:2, YCbCr	15-BIT, RGB, (5,5,5)	16-BIT, RGB, (5,6,5)	BT.656
P0	0 [0]	Cb0, Cr0 [$D0_{n+1}$]	B0 [$D0_{n+1}$]	B0 [$D0_{n+1}$]	0 [0]
P1	0 [0]	Cb1, Cr1 [$D1_{n+1}$]	B1 [$D1_{n+1}$]	B1 [$D1_{n+1}$]	0 [0]
P2	0 [0]	Cb2, Cr2 [$D2_{n+1}$]	B2 [$D2_{n+1}$]	B2 [$D2_{n+1}$]	0 [0]
P3	0 [0]	Cb3, Cr3 [$D3_{n+1}$]	B3 [$D3_{n+1}$]	B3 [$D3_{n+1}$]	0 [0]
P4	0 [0]	Cb4, Cr4 [$D4_{n+1}$]	B4 [$D4_{n+1}$]	B4 [$D4_{n+1}$]	0 [0]
P5	0 [0]	Cb5, Cr5 [$D5_{n+1}$]	G0 [$D5_{n+1}$]	G0 [$D5_{n+1}$]	0 [0]
P6	0 [0]	Cb6, Cr6 [$D6_{n+1}$]	G1 [$D6_{n+1}$]	G1 [$D6_{n+1}$]	0 [0]
P7	0 [0]	Cb7, Cr7 [$D7_{n+1}$]	G2 [$D7_{n+1}$]	G2 [$D7_{n+1}$]	0 [0]
P8	Y0, Cb0, Cr0 [D0]	Y0 [$D0_n$]	G3 [$D0_n$]	G3 [$D0_n$]	YCbCr Data, Ancillary Data, SAV and EAV Sequences [D0-D7, where P8 corresponds to D0]
P9	Y1, Cb1, Cr1 [D1]	Y1 [$D1_n$]	G4 [$D1_n$]	G4 [$D1_n$]	
P10	Y2, Cb2, Cr2 [D2]	Y2 [$D2_n$]	R0 [$D2_n$]	G5 [$D2_n$]	
P11	Y3, Cb3, Cr3 [D3]	Y3 [$D3_n$]	R1 [$D3_n$]	R0 [$D3_n$]	
P12	Y4, Cb4, Cr4 [D4]	Y4 [$D4_n$]	R2 [$D4_n$]	R1 [$D4_n$]	
P13	Y5, Cb5, Cr5 [D5]	Y5 [$D5_n$]	R3 [$D5_n$]	R2 [$D5_n$]	
P14	Y6, Cb6, Cr6 [D6]	Y6 [$D6_n$]	R4 [$D6_n$]	R3 [$D6_n$]	
P15	Y7, Cb7, Cr7 [D7]	Y7 [$D7_n$]	0 [$D7_n$]	R4 [$D7_n$]	

NOTE:

5. Definitions in brackets are port definitions during raw VBI data transfers. Refer to the section on teletext for more information on raw VBI.

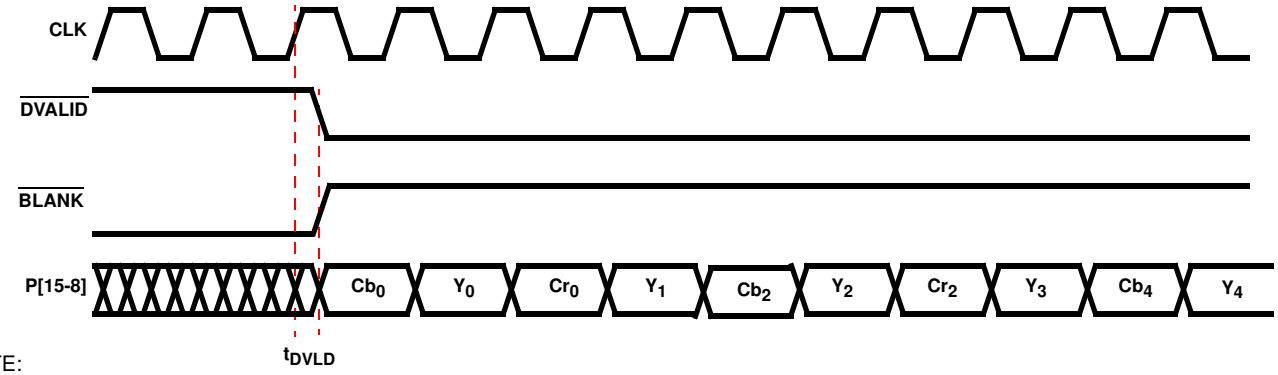
Pixel Output Port

Pixel data is output via the P0-P15 pins. Refer to Table 4 for the output pin definition as a function of the output mode. Refer to the section “CYCLE SLIPPING AND REAL-TIME PIXEL JITTER” for PLL and interface considerations.

8-Bit YCbCr Output

Each YCbCr data byte is output following each rising edge of CLK2. The YCbCr data is multiplexed as [Cb Y Cr Y′ Cb Y Cr Y′...], with the first active data each scan line containing Cb data. The pixel output timing is shown in Figures 8 and 9.

$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and $\overline{\text{FIELD}}$ are output following the rising edge of CLK2. When $\overline{\text{BLANK}}$ is asserted and $\overline{\text{VBIVALID}}$ is deasserted, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr. The behavior of the $\overline{\text{DVALID}}$ output is determined by bit 4 (DVLD_LTC) of the GENLOCK CONTROL register 04_H.



NOTE:

6. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period, but the values are forced to blanking levels.

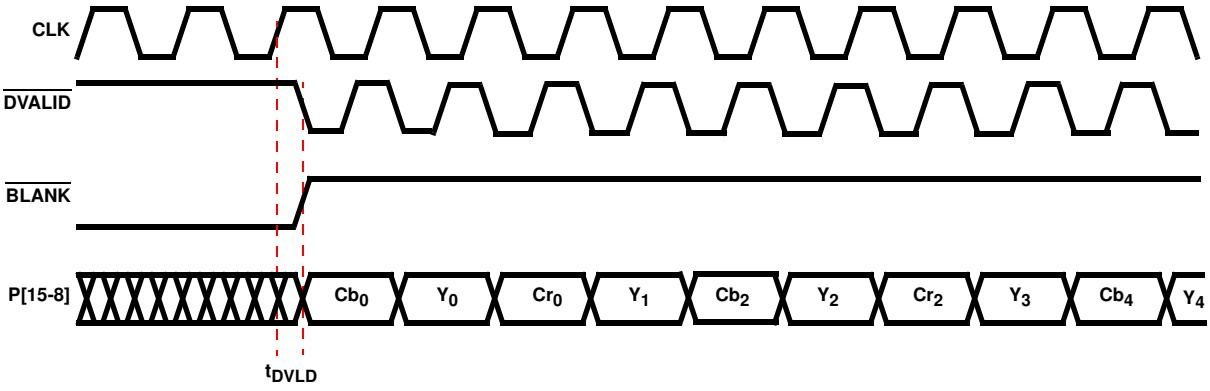
FIGURE 8. OUTPUT TIMING FOR 8-BIT YCbCr MODE (DVLD_LTC = 0)

16-Bit YCbCr, 15-Bit RGB, or 16-RGB Output

For 16-bit YCbCr, 15-bit RGB data, or 16-bit RGB output modes, the data is output following the rising edge of CLK2 with $\overline{\text{DVALID}}$ asserted. Either linear or gamma-corrected RGB data may be output. The pixel output timing is shown in Figures 10 to 13.

$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and $\overline{\text{FIELD}}$ are output following the rising edge of CLK2. When $\overline{\text{BLANK}}$ is asserted and $\overline{\text{VBIVALID}}$ is deasserted, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr; the RGB outputs have a value of 0.

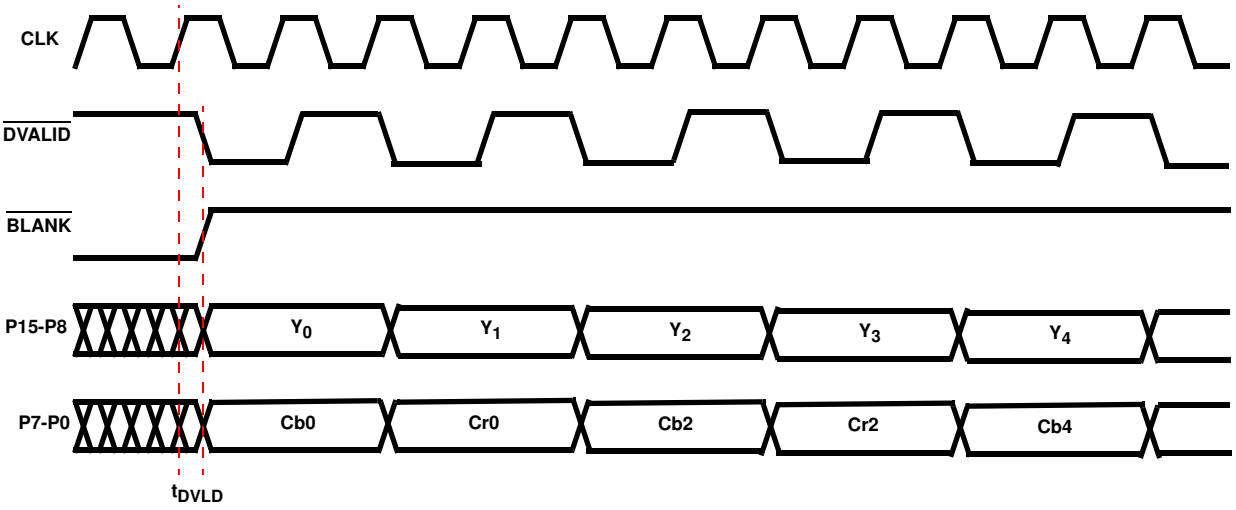
The behavior of the $\overline{\text{DVALID}}$ output is determined by bit 4 (DVLD_LTC) and bit 5 (DLVD_DCYC) of the GENLOCK CONTROL register 04_H.



NOTES:

7. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period, but the values are forced to blanking levels.
8. When DVLD_LTC is set to 1, the polarity of $\overline{\text{DVALID}}$ needs to be set to active low, otherwise $\overline{\text{DVALID}}$ will stay low during active video and be gated with the clock only during the blanking interval.

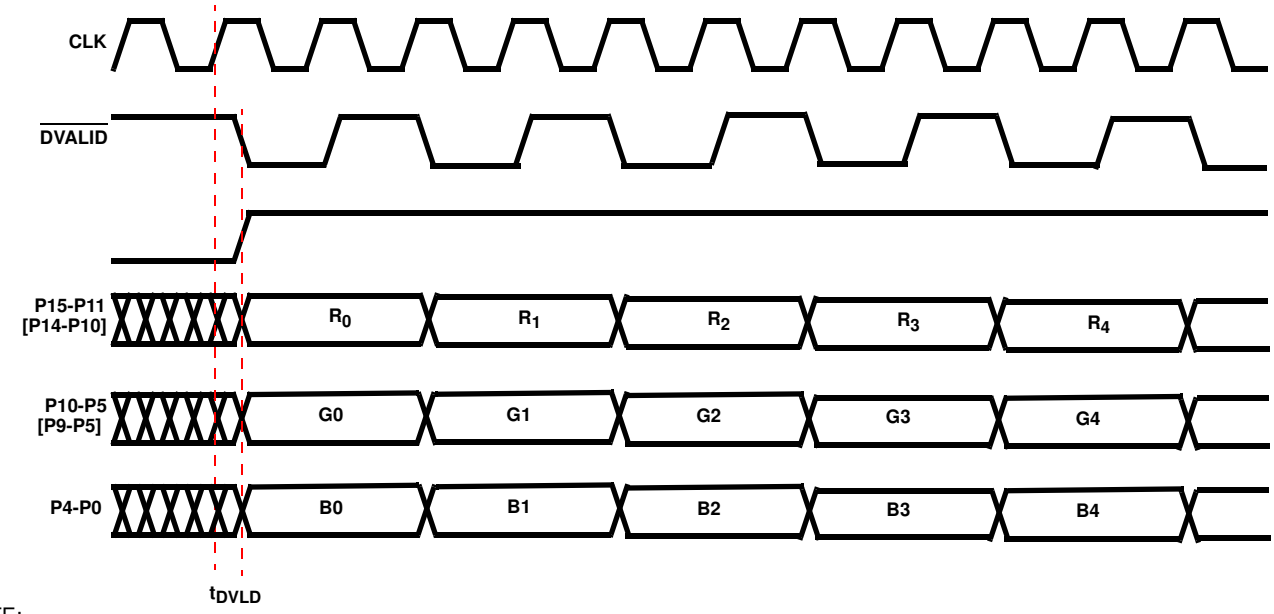
FIGURE 9. OUTPUT TIMING FOR 8-BIT YCbCr MODE (DVLD_LTC = 1)



NOTES:

9. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling.
10. $\overline{BLANK}$ is asserted per Figure 7.

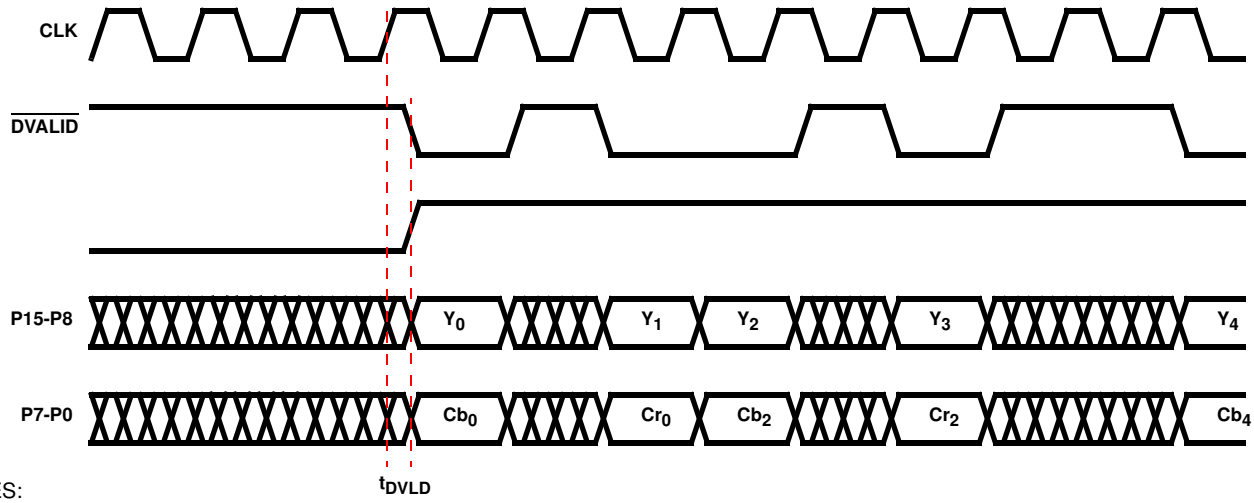
FIGURE 10. OUTPUT TIMING FOR 16-BIT YCbCr MODE (DVLD_LTC = 0, DVLD_DCYC = 0)



NOTE:

11. $\overline{BLANK}$ is asserted per Figure 7.

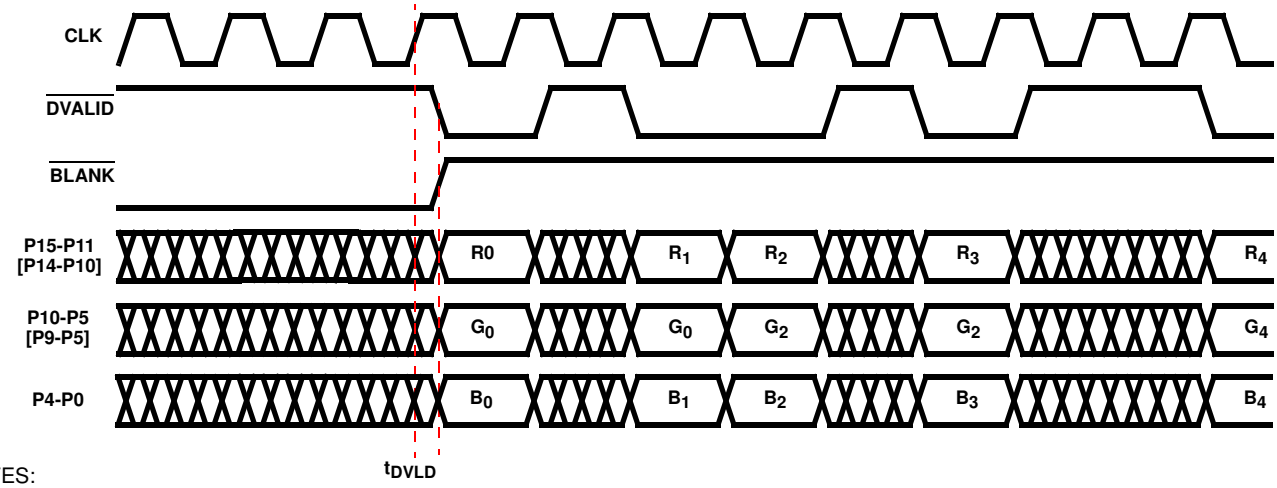
FIGURE 11. OUTPUT TIMING FOR 16-BIT [15-BIT] RGB MODE (DVLD_LTC = 0, DVLD_DCYC = 0)



NOTES:

12. Y_0 is the first active luminance pixel of a line. Cb_0 and Cr_0 are first active chrominance pixels in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling.
13. $\overline{\text{BLANK}}$ is asserted per Figure 7.
14. $\overline{\text{DVALID}}$ is asserted for every valid pixel during both active and blanking regions.

FIGURE 12. OUTPUT TIMING FOR 16-BIT YCbCr MODE (DVLD_LTC = 0, DVLD_DCYC = 1)



NOTES:

15. $\overline{\text{BLANK}}$ is asserted per Figure 7.
16. $\overline{\text{DAVLID}}$ is asserted for every valid pixel during both active and blanking regions. $\overline{\text{DVALID}}$ is not a 50% duty cycle synchronous output and will appear to jitter as the Output Sample Rate converter adjusts the output timing for various data rates and clock frequency inputs.

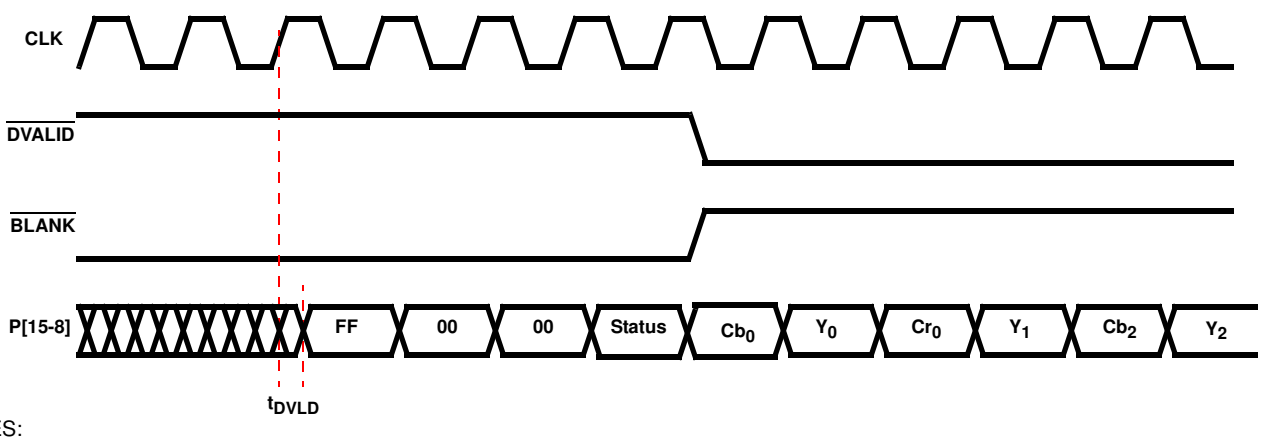
FIGURE 13. OUTPUT TIMING FOR 16-BIT [15-BIT] RGB MODE (DVLD_LTC = 0, DVLD_DCYC = 1)

8-Bit BT.656 Output

For the BT.656 output mode, data is output following each rising edge of CLK2. The BT.656 EAV and SAV formats are shown in Table 5 and the pixel output timing is shown in Figure 14. The EAV and SAV timing is determined by the programmed horizontal and vertical blank timing.

$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and FIELD are output following the rising edge of CLK2.

During the blanking intervals, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr, unless ancillary data is present.



NOTES:

17. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period.
18. Notice that $\overline{\text{DVALID}}$ is not asserted during the preamble and that $\overline{\text{BLANK}}$ is still asserted.
19. See table 5 for Status bit definitions.

FIGURE 14. OUTPUT TIMING FOR 8-BIT BT.656 MODE

TABLE 5. BT.656 EAV AND SAV SEQUENCES

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
Status Word	1	F	V	H	P3	P2	P1	P0

NOTES:

20. P3 = V xor H; P2 = F xor H; P1 = F xor V; P0 = F xor V xor H
21. F: “0” = field 1; “1” = field 2
22. V: “1” during vertical blanking
23. H: “0” at SAV (start of active video); “1” at EAV (end of active video)

Advanced Features

In addition to digitizing an analog video signal the HMP8117 has hardware to process different types of Vertical Blanking Interval (VBI) data as described in the following sections.

“Sliced” VBI Data Capture

The HMP8117 implements “sliced” data capture of select types of VBI data. The VBI decoders incorporate detection hysteresis to prevent them from rapidly turning on and off due to noise and transmission errors. In order to handle real-world signals, the VBI decoders also compensate for DC offsets and amplitude variations.

Closed Captioning

During closed captioning capture, the scan lines containing captioning information are monitored. If closed captioning is enabled and captioning data is present, the caption data is loaded into the caption data registers.

DETECTION OF CLOSED CAPTIONING

The closed caption decoder monitors the appropriate scan lines looking for the clock run-in and start bits used by captioning. If found, it locks to the clock run-in, the caption data is sampled and loaded into shift registers, and the data is then transferred to the caption data registers.

If the clock run-in and start bits are not found, it is assumed the scan line contains video data unless other VBI information is detected, such as teletext.

Once the clock run-in and start bits are found on the appropriate scan line for four consecutive odd fields, the Closed Captioning odd field Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive odd fields.

Once the clock run-in and start bits are found on the appropriate scan line for four consecutive even fields, the Closed Captioning even field Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive even fields.

READING THE CAPTION DATA

The caption data registers may be accessed in two ways: via the I^2C interface or as BT.656 ancillary data.

CAPTIONING DISABLED ON BOTH LINES

In this case, any caption data present is ignored.

The Caption odd field Read status bit and the Caption even field Read status bit are always a “0”.

ODD FIELD CAPTIONING

In this case, any caption data present on line 284 (or line 281 or 335 in the PAL modes) is ignored. Caption data present on line 21 (or line 18 or 22 in the PAL modes) is captured into a shift register then transferred to CLOSED CAPTION_ODD_A register 20_H and CLOSED CAPTION_ODD_B register 21_H.

The Caption even field Read status bit is always a “0”. The Caption odd field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. It is set to “0” after the data has been read out.

EVEN FIELD CAPTIONING

In this case, any caption data present on line 21 (or line 18 or 22 in the PAL modes) is ignored. Caption data present on line 284 (or line 281 or 335 in the PAL modes) is captured into a shift register then transferred to CLOSED CAPTION_EVEN_A register 22_H and CLOSED CAPTION_EVEN_B register 23_H.

The Caption odd field Read status bit is always a “0”. The Caption even field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers. It is set to “0” after the data has been read out.

ODD AND EVEN FIELD CAPTIONING

Caption data present on line 21 (or line 18 or 22 in the PAL modes) is captured into a shift register then transferred to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. Caption data present on line 284 (or line 281 or 335 in the PAL modes) is captured into a shift register then transferred to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers.

The Caption odd field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. It is set to “0” after the data has been read out.

The Caption even field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers. It is set to “0” after the data has been read out.

Widescreen Signalling (WSS)

During WSS capture (ITU-R BT.1119 and EIAJ CPX-1204), the scan lines containing WSS information are monitored. If WSS is enabled and WSS data is present, the WSS data is loaded into the WSS data registers.

DETECTION OF WSS

The WSS decoder monitors the appropriate scan lines looking for the run-in and start codes used by WSS. If found, it locks to the run-in code, the WSS data is sampled and loaded into shift registers, and the data is then transferred to the WSS data registers.

If the run-in and start codes are not found, it is assumed the scan line contains video data unless other VBI information is detected, such as teletext.

Once the run-in and start codes are found on the appropriate scan line for four consecutive odd fields, the WSS Line 20 Detect status bit is set to “1”. It is reset to “0” when the run-in and start codes are not found on the appropriate scan lines for four consecutive odd fields.

Once the run-in and start codes are found on the appropriate scan line for four consecutive even fields, the WSS Line 283 Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive even fields.

READING THE WSS DATA

The WSS data registers may be accessed in two ways: via the I^2C interface or as BT.656 ancillary data.

WSS DISABLED ON BOTH LINES

In this case, any WSS data present is ignored.

The WSS odd field Read status bit and the WSS even field Read status bit are always a “0”.

ODD FIELD WSS

In this case, any WSS data present on line 283 (or line 280 or 336 in the PAL modes) is ignored. WSS data present on line 20 (or line 17 or 23 in the PAL modes) is captured into a shift register then transferred to the WSS_ODD_A and WSS_ODD_B data registers.

The WSS even field Read status bit is always a “0”. The WSS odd field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_ODD_A and WSS_ODD_B registers. It is set to “0” after the data has been read out.

EVEN FIELD WSS

In this case, any WSS data present on line 20 (or line 17 or 23 in the PAL modes) is ignored. WSS data present on line 283 (or line 280 or 336 in the PAL modes) is captured into a shift register then transferred to the WSS_EVEN_A and WSS_EVEN_B data registers.

The WSS odd field Read status bit is always a “0”. The WSS even field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_EVEN_A and WSS_EVEN_B registers. It is set to “0” after the data has been read out.

ODD AND EVEN WSS

WSS data present on line 20 (or line 17 or 23 in the PAL modes) is captured into a shift register then transferred to the WSS_ODD_A and WSS_ODD_B registers. WSS data present on line 283 (or line 280 or 336 in the PAL modes) is captured into a shift register then transferred to the WSS_EVEN_A and WSS_EVEN_B registers.

The WSS odd field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_ODD_A and WSS_ODD_B registers. It is set to “0” after the data has been read out.

The WSS even field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_EVEN_A and WSS_EVEN_B registers. It is set to “0” after the data has been read out.

BT.656 Ancillary Data

Through the BT.656 interface the HMP8117 can generate non-active video data which contains CC, WSS, teletext or Real-Time Control Interface (RTCI) information. Teletext and RTCI data is only available as BT.656 ancillary data.

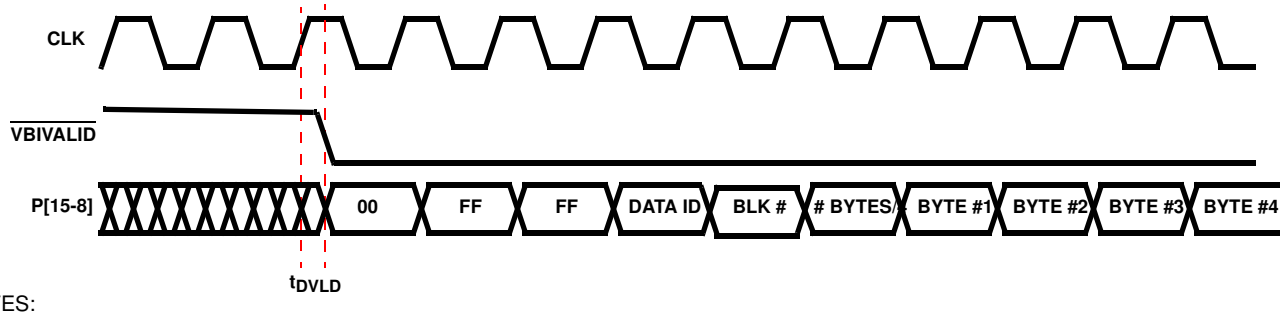
$\overline{\text{VBIVALID}}$ Output Timing

The $\overline{\text{VBIVALID}}$ output is asserted when outputting Closed Captioning, Wide Screen Signalling, Teletext or RTCI data as BT.656 ancillary data. It is asserted during the entire BT.656 ancillary data packet time, including the preamble.

BT.656 Closed Captioning and Wide Screen Signalling

Table 6 illustrates the format when outputting the caption data registers as BT.656 ancillary data. The ancillary data is present during the horizontal blanking interval after the line containing the captioning information.

Table 7 illustrates the format when outputting the WSS data registers as BT.656 ancillary data. The ancillary data is present during the horizontal blanking interval after the line containing the WSS information.



NOTES:

24. BT.656 VBI ancillary starts with a 00H, FFH and FFH sequence which is opposite to the SAV/EAV sequence of FFH, 00H and 00H.
25. During active VBI data intervals, $\overline{\text{DVALID}}$ is deasserted and $\overline{\text{BLANK}}$ is asserted.

FIGURE 15. OUTPUT TIMING FOR BT.656 VBI DATA TRANSFERS (CC, WSS, TELETEXT, RTCI)

TABLE 6. READING THE CLOSED CAPTION DATA AS BT.656 ANCILLARY DATA

PIXEL OUTPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{\text{P14}}$	ep	1	1	0	0	0	0 = odd field data 1 = even field data
Data Block Number	$\overline{\text{P14}}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{\text{P14}}$	ep	0	0	0	0	0	1
Caption Data	$\overline{\text{P14}}$	ep	0	0	bit 15	bit 14	bit 13	bit 12
	$\overline{\text{P14}}$	ep	0	0	bit 11	bit 10	bit 9	bit 8
	$\overline{\text{P14}}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{\text{P14}}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	$\overline{\text{P14}}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

26. ep = even parity for P8-P13.
27. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

TABLE 7. OUTPUTTING THE SLICED WSS DATA AS BT.656 ANCILLARY DATA

PIXEL OUTPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	0	1	0 = odd field data 1 = even field data
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	0	0	0	1	0
WSS Data	$\overline{P14}$	ep	0	0	0	0	bit 13	bit 12
	$\overline{P14}$	ep	0	0	bit 11	bit 10	bit 9	bit 8
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
WSS CRC Data	$\overline{P14}$	ep	0	0	0	0	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

28. ep = even parity for P8-P13.

29. WSS CRC data = “00 0000” during PAL operation.

30. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

Teletext

The HMP8117 supports ITU-R BT.653 625-line and 525-line teletext system B, C and D capture. NABTS (North American Broadcast Teletext Specification) is the same as BT.653 525-line system C, which is also used to transmit Intel Intercast™ information. WST (World System Teletext) is the same as BT.653 system B. Figure 16 shows the basic structure of a video signal that contains teletext data.

The scan lines containing teletext information are monitored. If teletext is enabled and teletext data is present, the teletext data is output as BT.656 ancillary data.

DETECTION OF TELETEXT

The teletext decoder monitors the scan lines, looking for the 16-bit clock run-in (sometimes referred to as the clock synchronization code) used by teletext. If found, it locks to the clock run-in, the teletext data is sampled and loaded into shift registers, and the data is then transferred to internal holding registers.

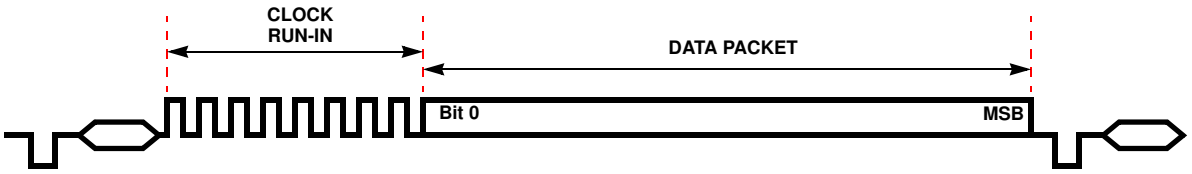
If the clock run-in is not found, it is assumed the scan line contains video data unless other VBI information is detected, such as WSS.

If a teletext clock run-in is found before line 23 or line 289 for NTSC and (M) PAL, or line 336 for (B, D, G, H, I, N, N_C) PAL, the VBI Teletext Detect status bit is immediately set to “1”. If not found by these lines, the status bit is immediately reset to “0”.

ACCESSING THE TELETEXT DATA

The teletext data must be output as BT.656 ancillary data. The I^2C interface does not have the bandwidth to output teletext information when needed.

Table 8 illustrates the teletext BT.656 ancillary data format and Figure 15 depicts the portion of the incoming teletext signal which is sliced and output as part of the ancillary data stream. The teletext data is present during the horizontal blanking interval after the line containing the teletext information. The actual BT.656 bytes that contain teletext data only contain 4 bits of the actual data packet. Note that only the data packet of Figure 16 is sent as ancillary data; the clock run-in is not included in the data stream.



NOTES:

31. The MSB is bit number: 271 for system C, 279 for system B 525-line and 343 for system B 625-line.
32. The clock run-in is 16 bits wide for both systems and is not included in the BT.656 ancillary data stream.
33. The bit rate is 5.727272 Mbits/s for system B and C on 525/60 systems and 6.9375 and 5.734375 Mbits/second respectively for 625/50 systems.
34. Teletext VBI Video Signal

FIGURE 16. TELETEXT VBI VIDEO SIGNAL

TABLE 8. OUTPUTTING THE SLICED TELETEXT DATA AS BT.656 ANCILLARY DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	1	0	0
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	1	0	1	1	0
Teletext Data (B, 625-line = 43 bytes) (B, 525-line = 35 bytes) (C = 34 bytes)	$\overline{P14}$	ep	0 = 525-line 1 = 625-line	0 = system B 1 = system C	bit 343	bit 342	bit 341	bit 340
	$\overline{P14}$	ep	0	0	bit 339	bit 338	bit 337	bit 336
	:							
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
Reserved	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

35. ep = even parity for P8-P13.
36. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.
37. For 525-line system B, bits 280-343 are “0”.
38. For system C, bits 272-343 are “0”.

“RAW” VBI DATA CAPTURE

“Raw” data capture of VBI data during blanked scan lines may be optionally implemented. In this instance, the active line time of blanked scan lines are sampled at the CLK2 rate, and output onto the pixel outputs. This permits software decoding of the VBI data to be done.

The line mask registers specify on which scan lines to generate “raw” VBI data. If the RAW VBI All bit is enabled, all the video lines are treated as raw VBI data, excluding the equalization and serration lines.

The start and end timing of capturing “raw” VBI data on a scan line is determined by the Start and End Raw VBI Registers. This allows the proper capture of “raw” VBI data regardless of the BLANK# output timing for active video.

The blanking level is subtracted from the “raw” VBI data samples, and the result is output onto the pixel outputs.

Note both “sliced” and “raw” VBI data may be available on the same line.

During NTSC operation, the first possible line of VBI data is lines 10 and 272, and the last possible lines are the last blanked scan lines. Lines 1-9 and 264-271 are always blanked.

During PAL (B, D, G, H, I, N, N_C) operation, the first possible line of VBI data are lines 6 and 318, and the last possible lines are the last blanked scan lines. Lines 623-5 and 311-317 are always blanked.

TABLE 9. OUTPUTTING RTCI AS BT.656 ANCILLARY DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	1	0	1
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	0	0	0	1	1
HPLL Increment	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
FSCPLL Increment	$\overline{P14}$	ep	PSW	0	bit 31	bit 30	bit 29	bit 28
	$\overline{P14}$	ep	F2 = 0	F1 = 0	bit 27	bit 26	bit 25	bit 24
	:							
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

39. ep = even parity for P8-P13.

40. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

During PAL (M) operation, the first possible line of VBI data is lines 7 and 269, and the last possible lines are the last blanked scan lines. Lines 523-6 and 261-268 are always blanked.

Real Time Control Interface

The Real Time Control Interface (RTCI) outputs timing information for a NTSC/PAL encoder as BT.656 ancillary data. This allows the encoder to generate “clean” output video.

RTCI information via BT.656 ancillary data is shown in Table 9. If enabled, this transfer occurs once per line and is completed before the start of the SAV sequence.

The PSW bit is always a “0” for NTSC encoding. During PAL encoding, it indicates the sign of V (“0” = negative; “1” = positive) for that scan line.

Host Interface

All internal registers may be written to or read by the host processor at any time, except for those bits identified as read-only. The bit descriptions for the control registers are listed beginning with Table 10.

The HMP8117 supports the fast-mode (up to 400kbps) I^2C interface consisting of the SDA and SCL pins. The device acts as a slave for receiving and transmitting data over the serial interface. When the interface is not active, SCL and SDA must be pulled high using external 4kΩ pull-up resistors. The SA input pin determines the slave address for the HMP8117. If the SA pin is pulled low, the address is $1000100x_B$. If the SA pin is pulled high through a 10kΩ pull-up resistor, the address is $1000101x_B$. (This ‘x’ bit in the address is the I^2C read flag.)

Data is placed on the SDA line when the SCL line is low and held stable when the SCL line is pulled high. Changing the state of the SDA line while SCL is high will be interpreted as either an I^2C bus START or STOP condition as indicated by Figure 18.

During I^2C write cycles, the first data byte after the slave address is treated as the control register sub address and is written into the internal address register. Any remaining data bytes sent during an I^2C write cycle are written to the control registers, beginning with the register specified by the address register as given in the first byte. The address register is then auto-incremented after each additional data byte sent on the I^2C bus during a write cycle. Writes to reserved bits within registers or reserved registers are ignored.

In order to perform a read from a specific control register within the HMP8117, an I^2C bus write must first be performed to properly setup the address register. Then an I^2C bus read can be performed to read from the desired control register(s). As a result of needing the write cycle for a read cycle there are actually two START conditions as shown in Figure 19. The address register is then auto-incremented after each byte read during the I^2C read cycle. Reserved registers return a value of 00_H.

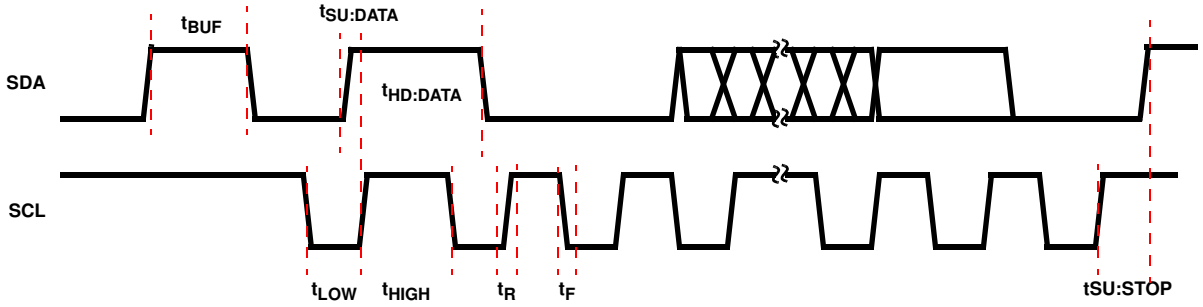


FIGURE 17. I^2C TIMING DIAGRAM

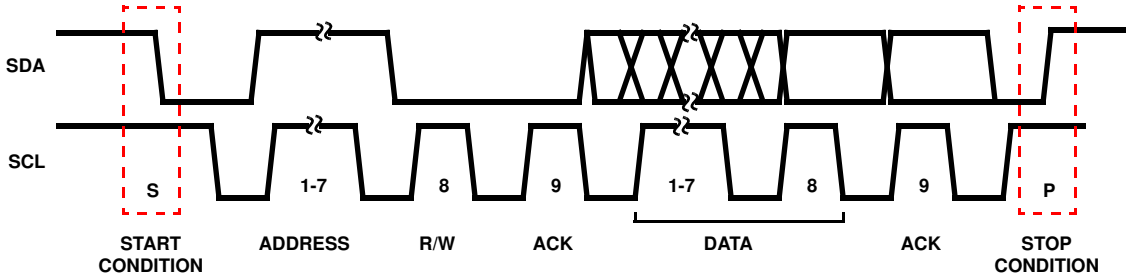


FIGURE 18. I^2C SERIAL DATA FLOW

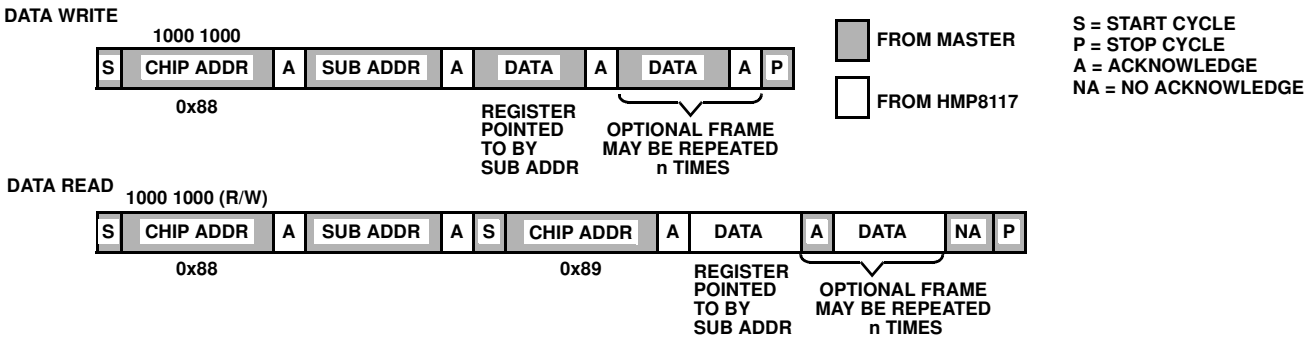


FIGURE 19. REGISTER WRITE/READ FLOW

Control Registers

TABLE 10. CONTROL REGISTER SUMMARY

SUB-ADDRESS	CONTROL REGISTER	RESET/ DEFAULT VALUE	USE VALUE	COMMENTS
00_H	Product ID	16_H or 17_H		Returns last two digits of part number in hex format.
01_H	Input Format	19_H		Defaults to auto-detect of input video standard.
02_H	Output Format	00_H		Defaults to 16-bit YCbCr data format.
03_H	Output Control	00_H	$C0_H$	Set Bits 7-6 to enable data and timing outputs.
04_H	Genlock Control	09_H		Defaults to 27MHz CLK2, Rectangular Pixel Mode
05_H	Analog Input Control	10_H		Defaults to input signal select = CVBS1.
06_H	Color Processing	52_H		
08_H	Luma Processing	04_H		
$0A_H$	Sliced VBI Data Enable	00_H		
$0B_H$	Sliced VBI Data Output	00_H		
$0C_H$	VBI Data Status	00_H		
$0E_H$	Video Status	00_H		
$0F_H$	Interrupt Mask	00_H		
10_H	Interrupt Status	00_H		
11_H	Raw VBI Control	00_H		
12_H	Raw VBI Start Count	$7A_H$		
$14_H/13_H$	Raw VBI Stop Count MSB/LSB	$03_H/4A_H$		
15_H	Raw VBI Line Mask_7_0	FE_H		
16_H	Raw VBI Line Mask_15_8	$1F_H$		
17_H	Raw VBI Line Mask_18_16	00_H		
18_H	Brightness	00_H		
19_H	Contrast	80_H		
$1A_H$	Hue	00_H		
$1B_H$	Saturation	80_H		
$1C_H$	Color Gain Adjust	40_H		
$1D_H$	Video Gain Adjust	80_H		
$1E_H$	Sharpness	10_H		
$1F_H$	Host Control	00_H		Set bit 7 for Soft Reset. Set bit 6 for Power Down.
20_H-23_H	Closed Caption Data Registers	80_H		
24_H-29_H	WSS Data & CRC Registers	00_H		
$31_H/30_H$	Start H_BLANK MSB/LSB	$03_H/4A_H$	Table 3	$\overline{\text{BLANK}}$ programming changes for each video standard.
32_H	End H_BLANK	$7A_H$	Table 3	(same as above)
$34_H/33_H$	Start V_BLANK MSB/LSB	$01_H/02_H$	Table 3	(same as above)
35_H	End V_BLANK	12_H	Table 3	(same as above)
36_H	End HSYNC	30_H	Table 3	(same as above)
37_H	HSYNC Detect Window	20_H	90_H	A wider window tolerates poorly timed video sources.
41_H	MV Control	26_H		
42_H	Reserved	00_H	30_H	Set bits 5-4 to 11_B for optimum performance.
50_H	Programmable Fractional Gain	$0C_H$	21_H	A slower PFG improves AGC stability.
51_H	MV Stripe Gate	14_H		
52_H	Reserved	02_H	22_H	Set bit 5 to “1” for optimum performance.
53_H	AGC Hysteresis	00_H	$F0_H$	Larger hysteresis improves AGC stability.
$7F_H$	Device Revision	01_H		Production baseline revision is 01_H.
Sub-Addresses: 40_H, 43_H-$4F_H$ are reserved. Reads from these registers may return non-zero values.				
Sub-Addresses: 07_H, 09_H, $0D_H$, $2A_H$-$2F_H$, 38_H-$3F_H$ and 54_H-$7E_H$ are unused. Reads from these registers return 00_H. Writes are ignored.				

TABLE 11. PRODUCT ID REGISTER

SUB ADDRESS = 00_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Product ID	This 8-bit register specifies the last two digits of the product number. Data written to this read-only register is ignored.	17_H

TABLE 12. INPUT FORMAT REGISTER

SUB ADDRESS = 01_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Reserved		0_B
6-5	Video Timing Standard	These bits are read only unless bit 4 = “0”. 00 = (M) NTSC 01 = (B, D, G, H, I, N) PAL 10 = (M) PAL 11 = Combination (N) PAL; also called (N_C) PAL	00_B
4	Auto Detect Video Standard	0 = Manual selection of video timing standard 1 = Auto detect of video timing standard	1_B
3	Setup Select	Typically, this bit should be a “1” during (M) NTSC and (M, N) PAL operation. Otherwise, it should be a “0”. 0 = Video source has a 0 IRE blanking pedestal 1 = Video source has a 7.5 IRE blanking pedestal	1_B
2-1	Reserved		00_B
0	Adaptive Sync Slice Enable	This bit specifies whether to use fixed or adaptive sync slicing. Adaptive sync slicing automatically determines the midpoint of the sync amplitude to determine timing. 0 = Fixed sync slicing 1 = Adaptive sync slicing	1_B

TABLE 13. OUTPUT FORMAT REGISTER

SUB ADDRESS = 02_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Output Color Format	000 = 16-bit 4:2:2 YCbCr100 = 16-bit RGB 001 = 8-bit 4:2:2 YCbCr101 = reserved 010 = 8-bit parallel BT.656110 = reserved 011 = 15-bit RGB111 = reserved	000_B
4-3	RGB Gamma Select	These bits are ignored except during RGB output modes. 00 = Linear RGB (gamma of input source = 2.2) 01 = Linear RGB (gamma of input source = 2.8) 10 = Gamma-corrected RGB (gamma = gamma of input source) 11 = reserved	00_B
2-1	Output Color Select	00 = Normal operation10 = Output black field 01 = Output blue field11 = Output 75% color bars	00_B
0	Reserved	Set to “0” for proper operation. Vertical Pixel Siting control is not supported.	0_B

TABLE 14. OUTPUT CONTROL REGISTER

SUB ADDRESS = 03_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Video Data Output Enable	This bit is used to enable the P0-P15 outputs. 0 = Outputs 3-stated. 1 = Outputs enabled	0_B
6	Video Timing Output Enable	This bit is used to enable the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$, FIELD, $\overline{\text{VBIVALID}}$, $\overline{\text{DVALID}}$, and $\overline{\text{INTREQ}}$ outputs. 0 = Outputs 3-stated. 1 = Outputs enabled	0_B
5	FIELD Polarity	0 = Active low (low during odd fields). 1 = Active high (high during odd fields)	0_B
4	$\overline{\text{BLANK}}$ Polarity	0 = Active low (low during blanking). 1 = Active high (high during blanking)	0_B
3	$\overline{\text{HSYNC}}$ Polarity	0 = Active low (low during horizontal sync). 1 = Active high (high during horizontal sync)	0_B
2	$\overline{\text{VSYNC}}$ Polarity	0 = Active low (low during vertical sync). 1 = Active high (high during vertical sync)	0_B
1	$\overline{\text{DVALID}}$ Polarity	0 = Active low (low during valid pixel data). 1 = Active high (high during valid pixel data)	0_B
0	$\overline{\text{VBIVALID}}$ Polarity	0 = Active low (low during VBI data). 1 = Active high (high during VBI data)	0_B

TABLE 15. GENLOCK CONTROL REGISTER

SUB ADDRESS = 04_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Aspect Ratio Mode	0 = Rectangular (BT.601) pixels 1 = Square pixels	0_B
6	Freeze Output Timing Enable	Setting this bit to a “1” freezes the output timing at the end of the field. Resetting this bit to a “0” resumes normal operation at the start of the next field. 0 = Normal operation 1 = Freeze output timing	0_B
5	$\overline{\text{DVALID}}$ Duty Cycle Control (DVLD_DCYC)	This bit is ignored during the 8-bit YCbCr and BT.656 output modes. During 16-bit YCbCr, 15-bit RGB, or 16-bit RGB output modes, this bit is defined as: 0 = $\overline{\text{DVALID}}$ has 50/50 duty cycle at the pixel output data rate 1 = $\overline{\text{DVALID}}$ goes active based on line-lock. This will cause $\overline{\text{DVALID}}$ to not have a 50/50 duty cycle. This bit is intended to be used in maintaining backward compatibility with the HMP8112A $\overline{\text{DVALID}}$ output timing.	0_B
4	$\overline{\text{DVALID}}$ Line Timing Control (DVLD_LTC)	During 16-bit YCbCr, 15-bit RGB, or 16-bit RGB output modes, this bit is defined as: 0 = $\overline{\text{DVALID}}$ present only during active video time on active scan lines 1 = $\overline{\text{DVALID}}$ present the entire scan line time on all scan lines During the 8-bit YCbCr and BT.656 output modes, this bit defines the $\overline{\text{DVALID}}$ output as: 0 = Normal timing 1 = $\overline{\text{DVALID}}$ signal ANDed with CLK2	0_B
3	Missing $\overline{\text{HSYNC}}$ Detect Select	This bit specifies the number of missing horizontal sync pulses before entering horizontal lock acquisition mode. 0 = 12 pulses 1 = 1 pulse	1_B
2	Missing $\overline{\text{VSYNC}}$ Detect Select	This bit specifies the number of missing vertical sync pulses before entering vertical lock acquisition mode. 0 = 3 pulses 1 = 1 pulse	0_B
1-0	CLK2 Frequency	This bit indicates the frequency of the CLK2 input clock. 00 = 24.54MHz10 = 29.5MHz 01 = 27.0MHz11 = Reserved	01_B

TABLE 16. ANALOG INPUT CONTROL REGISTER

SUB ADDRESS = 05_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Lock Loss Video Gain Select	If bits 5-4 do not equal “01”, these bits indicate what mode the AGC circuitry will be after loss of sync. If bits 5-4 equal “01”, these bits are ignored. 00 = Automatic gain control: bits 5-4 will be reset to “01” 01 = Maintain fixed gain: bits 5-4 will not be changed 10 = Normal AGC switching to fixed gain after lock achieved: bits 5-4 will not be reset to “01” unless they indicated “freeze automatic gain control” 11 = reserved	00_B
5-4	Video Gain Control Select	00 = Fixed 1x gain 01 = Automatic gain control 10 = Fixed gain control. (Use gain factor from Video Gain Adjust register $1D_H$.) 11 = Freeze automatic gain control	01_B
3	Digital Anti-Alias Filter Control	0 = Internal digital anti-alias filter is active. 1 = Internal digital anti- alias filter is bypassed. (Not Recommended)	0_B
2-0	Video Signal Input Select	000 = CVBS1 001 = CVBS2 010 = CVBS3 011 = S-video 1XX = reserved	000_B

TABLE 17. COLOR PROCESSING REGISTER

SUB ADDRESS = 06_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Digital Color Gain Control Select	00 = No gain control (gain = 1x) 01 = Automatic gain control 10 = Fixed gain control. (Use gain factor from Color Gain Adjust register $1C_H$.) 11 = Freeze automatic gain control	01_B
5-4	Color Killer Select	00 = Force color on 01 = Enable color killer 10 = reserved 11 = Force color off	01_B
3-2	Color Coring Select	Coring may be used to reduce low-level noise in the CbCr signals. 00 = No coring 01 = 1 code coring 10 = 2 code coring 11 = 3 code coring	00_B
1	Contrast Control Select	This bit specifies whether the contrast control affects just the Y data (“0”) or both the Y and CbCr data (“1”). To avoid color shifts when changing contrast, this bit should be a “1”. 0 = Contrast controls only Y data 1 = Contrast controls Y and CbCr data	1_B
0	Color Low-Pass Filter Select	This bit selects the bandwidth of the CbCr data. 0 = 850kHz 1 = 1.5MHz	0_B