



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### FEATURES

- Xilinx Virtex-4 FPGA-based buffer memory board
- Used for capturing digital data from high speed ADC evaluation boards to simplify evaluation
- 64 kB FIFO depth
- Parallel input at 644 MSPS SDR and 800 MSPS DDR
- Supports 1.8 V, 2.5 V, and 3.3 V CMOS and LVDS interfaces
- Supports multiple ADC channels up to 18 bits
- Measures performance with VisualAnalog
  - Real-time FFT and time domain analysis
  - Analyzes SNR, SINAD, SFDR, and harmonics
- Simple USB port interface (2.0)
- Supports ADCs with serial port interfaces (SPI)
- FPGA reconfigurable via JTAG, on-board EPROM, or USB
- On-board regulator circuit speeds setup
  - 5 V, 3 A switching power supply included
- Compatible with Windows 98 (2nd edition), Windows 2000, Windows ME, and Windows XP

### EQUIPMENT NEEDED

- Analog signal source and antialiasing filter
- Low jitter clock source
- High speed ADC evaluation board and ADC data sheet
- PC running Windows 98 (2nd edition), Windows 2000, Windows ME, or Windows XP
- Latest version of VisualAnalog
- USB 2.0 port recommended (USB 1.1 compatible)

### PRODUCT HIGHLIGHTS

1. Easy to Set Up. Connect the included power supply along with the CLK and AIN signal sources to the two evaluation boards. Then connect to the PC via the USB port and evaluate the performance instantly.
2. USB Port Connection to PC. PC interface is via a USB 2.0 connection (1.1 compatible) to the PC. A USB cable is provided in the kit.
3. 64 kB FIFO. The on-board FPGA contains an integrated FIFO to store data captured from the ADC for subsequent processing.
4. Up to 644 MSPS SDR/800 MSPS DDR Encode Rates on Each Channel. Multichannel ADCs with encode rates up to 644 MSPS SDR and 800 MSPS DDR can be used with the ADC capture board.
5. Supports ADCs with Serial Port Interface or SPI. Some ADCs include a feature set that can be changed via the SPI. The ADC capture board supports these SPI-driven features through the existing USB connection to the computer without additional cabling needed.
6. VisualAnalog™. VisualAnalog supports the HSC-ADC-EVALC hardware platform as well as enabling virtual ADC evaluation using ADIsimADC™, Analog Devices proprietary behavioral modeling technology. This allows rapid comparison between multiple ADCs, with or without hardware evaluation boards. For more information, see AN-737 at [www.analog.com/VisualAnalog](http://www.analog.com/VisualAnalog).

### FUNCTIONAL BLOCK DIAGRAM

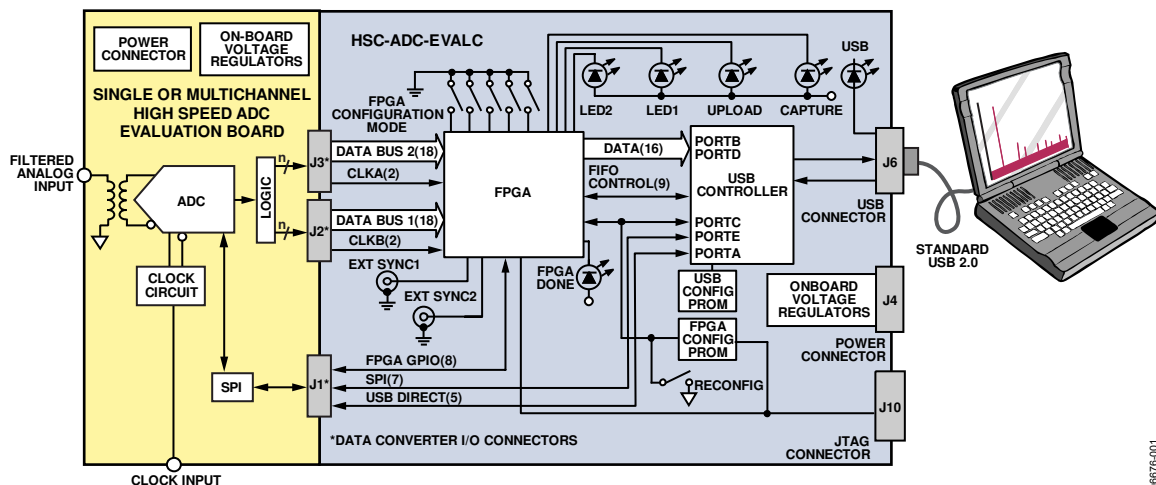


Figure 1.

### Rev. 0

Evaluation boards are only intended for device evaluation and not for production purposes. Evaluation boards as supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose. No license is granted by implication or otherwise under any patents or other intellectual property by application or use of evaluation boards. Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Analog Devices reserves the right to change devices or specifications at any time without notice. Trademarks and registered trademarks are the property of their respective owners. Evaluation boards are not authorized to be used in life support devices or systems.

# HSC-ADC-EVALC

## TABLE OF CONTENTS

Features .....	1	Theory of Operation .....	8
Equipment Needed.....	1	Configuration .....	8
Product Highlights .....	1	Input Circuitry.....	8
Functional Block Diagram .....	1	Data Capture.....	8
Revision History .....	2	Code Description .....	8
Product Description.....	3	FPGA Configuration and Customization.....	8
Evaluation Board Description.....	3	Evaluation Board Schematics and Artwork.....	9
Evaluation Board Hardware.....	4	HSC-ADC-EVALC Schematics.....	9
HSC-ADC-EVALC ADC Capture Board Easy Start .....	4	PCB Layout .....	23
Power Supplies .....	4	I/O Connector—J1, J2, and J3 Pin Mapping .....	24
Connection and Setup .....	4	Ordering Information.....	28
Jumpers .....	5	Bill of Materials (RoHS Compliant) .....	28
HSC-ADC-EVALC ADC Capture Board Features.....	6	Ordering Guide .....	30
HSC-ADC-EVALC Supported ADC Evaluation Boards.....	7	ESD Caution.....	30

## REVISION HISTORY

4/07—Revision 0: Initial Version

## PRODUCT DESCRIPTION

The Analog Devices, Inc. high speed converter evaluation platform (HSC-ADC-EVALC) includes the latest version of VisualAnalog and an FPGA-based buffer memory board to capture blocks of digital data from the Analog Devices high speed analog-to-digital converter (ADC) evaluation boards. The ADC capture board is connected to the PC through a USB port and is used with VisualAnalog to quickly evaluate the performance of high speed ADCs. Users can view an FFT for a specific analog input and encode rate to analyze SNR, SINAD, SFDR, and harmonic information.

The ADC capture board is easy to set up. Additional equipment needed includes an Analog Devices high speed ADC evaluation board, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is enabled instantly on the PC.

The ADC capture board enables numerous expansion and evaluation possibilities by virtue of its powerful reconfigurable FPGA core.

The system can acquire digital data at speeds up to 644 MSPS single data rate (SDR) and 800 MSPS double data rate (DDR).

The FPGA contains an integrated FIFO memory that allows capture of data record lengths up to a total of 64 kB. A USB 2.0 microcontroller communicating with VisualAnalog allows for easy interfacing to newer computers using the USB 2.0 (USB 1.1 compatible) interface.

## EVALUATION BOARD DESCRIPTION

The ADC capture board provides all of the support circuitry required to accept two 18-bit channels from an ADC's parallel CMOS or LVDS outputs. Various functions such as FPGA configuration load options and I/O logic levels can be selected by proper connection of various jumpers or switches (see Table 1). When using the HSC-ADC-EVALC in conjunction with an ADC evaluation board, it is critical that the signal sources used for the ADC board's analog input and clock have very low phase noise (<1 ps rms jitter) to achieve the ultimate performance of the converter.

Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 5 to Figure 20 for complete schematics and layout plots.



## EVALUATION BOARD HARDWARE

### HSC-ADC-EVALC ADC CAPTURE BOARD

#### EASY START

##### Requirements

- HSC-ADC-EVALC ADC capture board, VisualAnalog, 5 V wall transformer, and USB cable
- High speed ADC evaluation board and ADC data sheet
- Power supply for ADC evaluation board
- Analog signal source and appropriate filtering
- Low jitter clock source applicable for specific ADC evaluation, typically <1 ps rms jitter
- PC running Windows® 98 (2nd edition), Windows 2000, Windows ME, or Windows XP
- PC with a USB 2.0 port recommended (USB 1.1 compatible)

##### Easy Start Steps

##### Important Note

Administrative rights for the Windows operating systems are needed during the entire easy start procedure.

Completion of every step before reverting to a normal user mode is recommended.

1. Install VisualAnalog from the CD provided in the ADC capture board kit or download the latest version from the Web. For the latest updates to the software, check the Analog Devices website at [www.analog.com/FIFO](http://www.analog.com/FIFO).
2. Connect the ADC capture board to the ADC evaluation board. If an adapter is required, insert the adapter between the ADC evaluation board and the ADC capture board.
3. Connect the provided USB cable to the ADC capture board and to an available USB port on the computer.
4. Refer to Table 1 for setting the ADC capture board's I/O logic level to match the level coming from the ADC evaluation board. 1.8 V is default; 2.5 V and 3.3 V are jumper selectable. Most evaluation boards can be used with the default settings.
5. The ADC capture board is supplied with a wall mount switching power supply. Connect the supply end to an ac wall outlet rated for 100 Vac to 240 Vac at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J4.
6. Once the USB cable is connected to both the computer and the HSC-ADC-EVALC board, and power is applied, the USB driver starts to install. The **Found New Hardware Wizard** opens and prompts you through the automated install process.
7. (Optional) Verify in the Windows device manager that **Analog Devices ADC-HSC-EVALC** is listed under the USB hardware.
8. Refer to the instructions included in the respective ADC data sheet found at [www.analog.com/FIFO](http://www.analog.com/FIFO) for more information about connecting the ADC evaluation board's power supply and other requirements. After verification of power supply connections, apply power to the ADC evaluation board and check the voltage levels on the ADC board to make sure they are correct.
9. Make sure the evaluation boards are powered on before connecting the analog input and clock. Connect the appropriate analog input (which should be filtered with a band-pass filter) and low jitter clock signal.
10. Refer to the *VisualAnalog User Manual* at [www.analog.com/FIFO](http://www.analog.com/FIFO) for detailed software operating instructions.

#### POWER SUPPLIES

The ADC capture board is supplied with a wall mount switching power supply that provides a 5 V, 3 A maximum output. Connect the supply to the rated 100 Vac to 240 Vac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J4. On the PC board, the supply is fused and conditioned before connecting to the regulators that supply the proper bias to the entire ADC capture board.

#### CONNECTION AND SETUP

The ADC capture board has two 40-pin connectors (J2 and J3) that accept two 18-bit channels of parallel CMOS or LVDS inputs from the ADC (see Figure 2). The third 40-pin connector (J1) is used to pass SPI and other USB/FPGA control signals across to adjacent ADC evaluation boards that support these features.

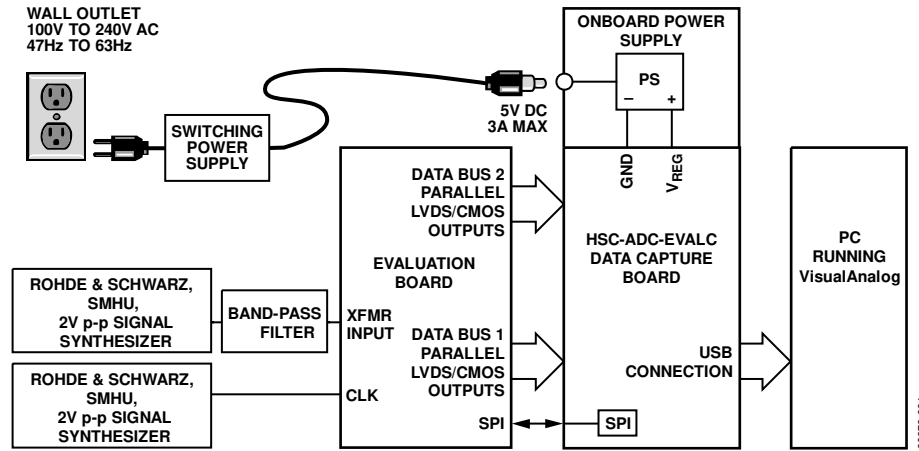


Figure 2. Example Setup Using ADC Evaluation Board and HSC-ADC-EVALC ADC Capture Board

## JUMPERS

### Default Settings

Table 1 lists the default settings for the HSC-ADC-EVALC evaluation kit.

Table 1. Jumper Configurations

Jumper Number	Description
J9, Pin 1 to Pin 2 (1.8 V)	Default. Sets FPGA I/O voltage to 1.8 V logic (hardwired, do not remove).
J9, Pin 3 to Pin 4 (2.5 V)	Install single jumper here to set FPGA I/O voltage to 2.5 V logic.
J9, Pin 5 to Pin 6 (3.3 V)	Install single jumper here to set FPGA I/O voltage to 3.3 V logic.

Table 2. FPGA Configuration Mode

U4 DIP Switch Setting	M0	M1	M2	M3	M4
FPGA Configured via EEPROM	On	On	On	Reserved	Reserved
FPGA Configured via USB (Default)	On	Off	Off	Reserved	Reserved

# HSC-ADC-EVALC

## HSC-ADC-EVALC ADC CAPTURE BOARD FEATURES

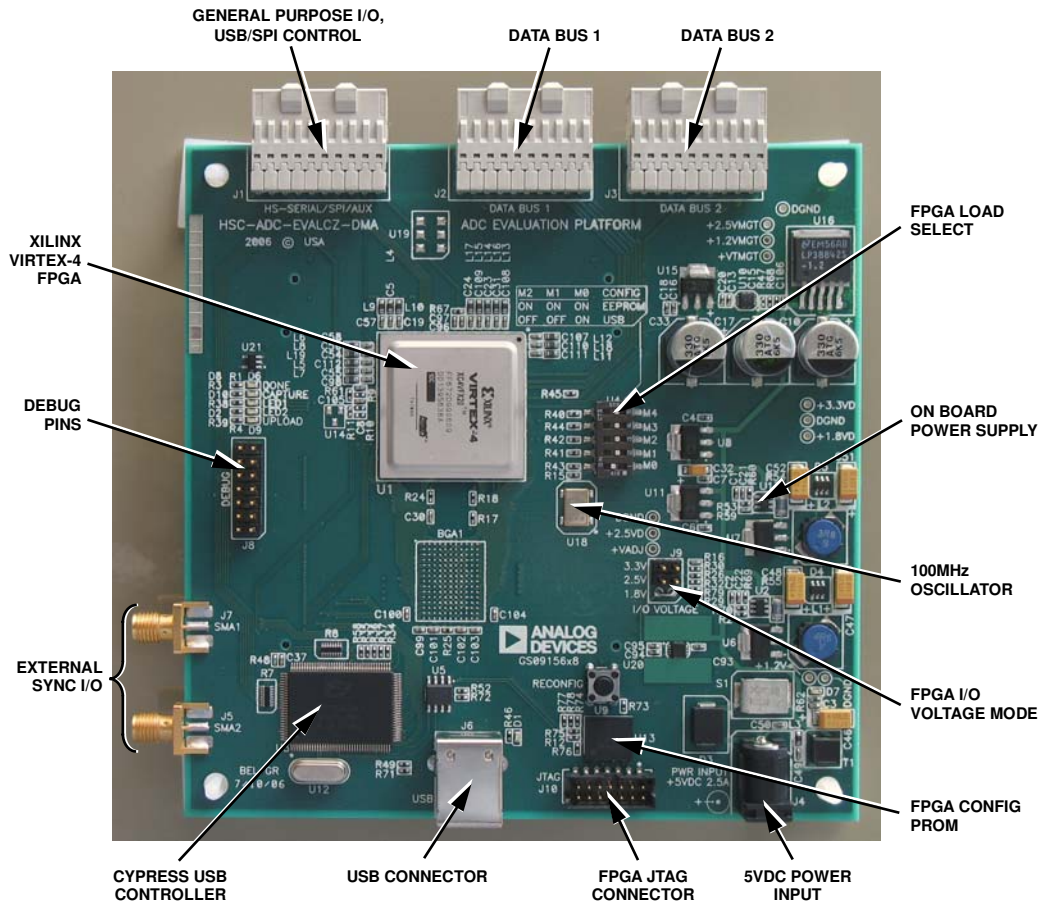


Figure 3. HSC-ADC-EVALC Components (Top View)

06876-002

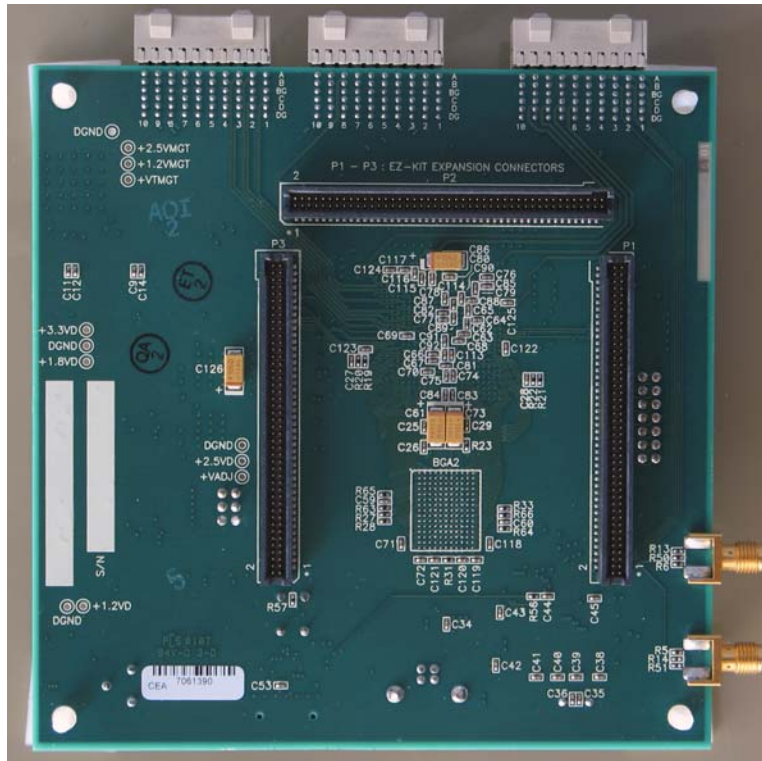


Figure 4. HSC-ADC-EVALC Components (Bottom View)

### HSC-ADC-EVALC SUPPORTED ADC EVALUATION BOARDS

Refer to the Analog Devices ADC capture board product page at [www.analog.com/FIFO](http://www.analog.com/FIFO) for a list of HSC-ADC-EVALC-compatible ADC evaluation boards. Some legacy ADC boards may require interposer cards to facilitate proper pin mapping to the ADC capture board. If needed, the interposer part number is noted in the compatibility table at [www.analog.com/FIFO](http://www.analog.com/FIFO) for the respective data converter.



## THEORY OF OPERATION

The HSC-ADC-EVALC evaluation platform is based around the Virtex-4 FPGA (XC4VFX20-10FFG672C) from Xilinx®, which can be programmed through VisualAnalog to operate with a variety of data converters. Another key component, the Cypress USB device (U3), communicates with a host PC and provides the SPI interface used for configuration.

### CONFIGURATION

Some converter devices require programming for mode or feature selection, which the SPI controller accomplishes using SPI-accessible register maps. U3 drives the 4-wire SPI (SCLK, SDI, SDO, CSB<sup>1</sup>) signals to the converter board via connector (J1). For more information on serial port interface (SPI) functions, consult the user manual titled *Interfacing to High Speed ADCs via SPI* at [www.analog.com/FIFO](http://www.analog.com/FIFO).

The SPI interface designed on the Cypress IC can communicate with up to five different SPI-enabled devices including the FPGA. The CLK and SDI/SDO data lines are common to all SPI devices. The desired SPI-enabled device is selected for control by using one of the five active low chip select (CS) pins. This functionality is controlled by selecting a SPI channel in the SPI Controller software.

At power-up, VisualAnalog attempts to autodetect the converter that is attached to the ADC capture board using the SPI interface. If a recognized device is found, VisualAnalog selects the appropriate FPGA configuration; otherwise, the user is prompted to make the device selection. In either case, VisualAnalog then programs the FPGA using the SPI interface of U3. The configurations typically program a FIFO data capture function within the FPGA.

### INPUT CIRCUITRY

The parallel data input pins of the FPGA, which interface to the converter, are configurable. They can operate with 1.8 V, 2.5 V, or 3.3 V logic levels and can accept LVDS or CMOS inputs. Each channel of the ADC capture board requires a clock signal to capture data. These clock signals are normally provided by the attached ADC evaluation board and are passed along with the data through one or more pins on Connector J2 and/or

Connector J3. Refer to the HSC-ADC-EVALC I/O connector pin mappings shown in Figure 21 and Figure 22.

### DATA CAPTURE

The process of filling the FIFO and reading the data back requires several steps.

1. VisualAnalog initiates the FIFO fill process by resetting the FIFOs.
2. The 48 MHz USB read clock (RCLK) is then suspended to ensure that it does not add noise to the ADC input.
3. VisualAnalog waits approximately 30 ms to allow for data capture before beginning the readback process. This wait time is an adjustable parameter in VisualAnalog.
4. VisualAnalog reads the data from the FIFO through the USB interface to the PC.

### CODE DESCRIPTION

FPGA configuration files are provided by ADI for all ADCs supported by the HSC-ADC-EVALC evaluation platform. These files are designed and tested to facilitate quick performance evaluations of Analog Devices data converters. No additional FPGA programming is required from the user for typical operation.

### FPGA CONFIGURATION AND CUSTOMIZATION

Users can manually customize or update the FPGA code through a JTAG connector (J10) provided on the ADC capture board, as shown in Figure 17. However, Analog Devices provides no support or guarantee of performance if the provided code is customized by the user.

The HSC-ADC-EVALC hardware platform may contain additional circuit functions to support future developments and capabilities. These functions are not supported beyond the scope of this data sheet and the Analog Devices supplied data-capture FPGA routines at this time.

Additional FPGA programming support may be available through the user's local Xilinx representative or distributor.

<sup>1</sup> Note that CSB1 is the default CSB line used.

## EVALUATION BOARD SCHEMATICS AND ARTWORK

### HSC-ADC-EVALC SCHEMATICS

#### TYCO AND DSP EZ-KIT CONNECTOR TO FPGA

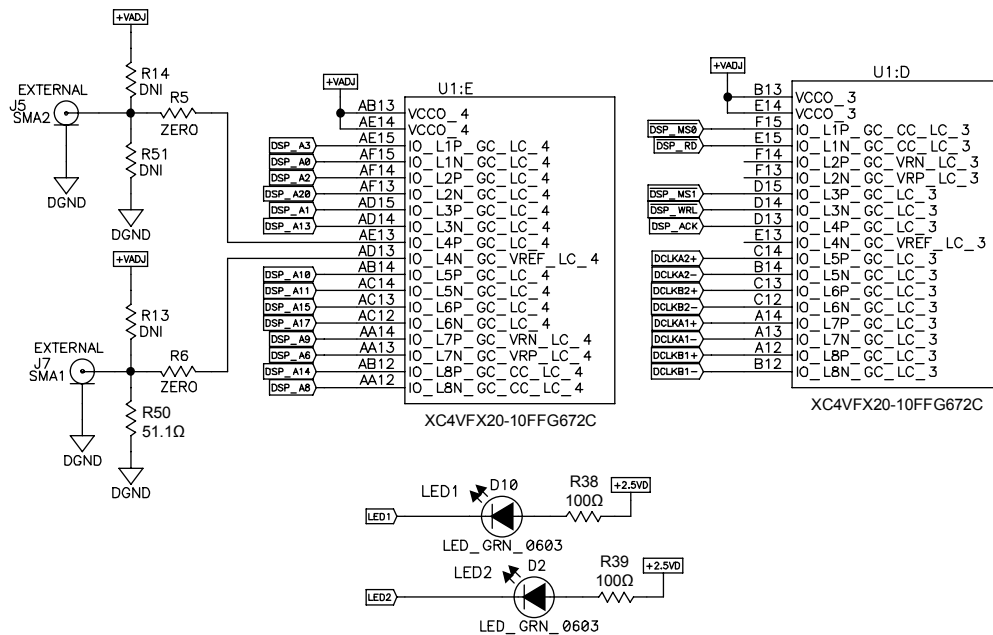
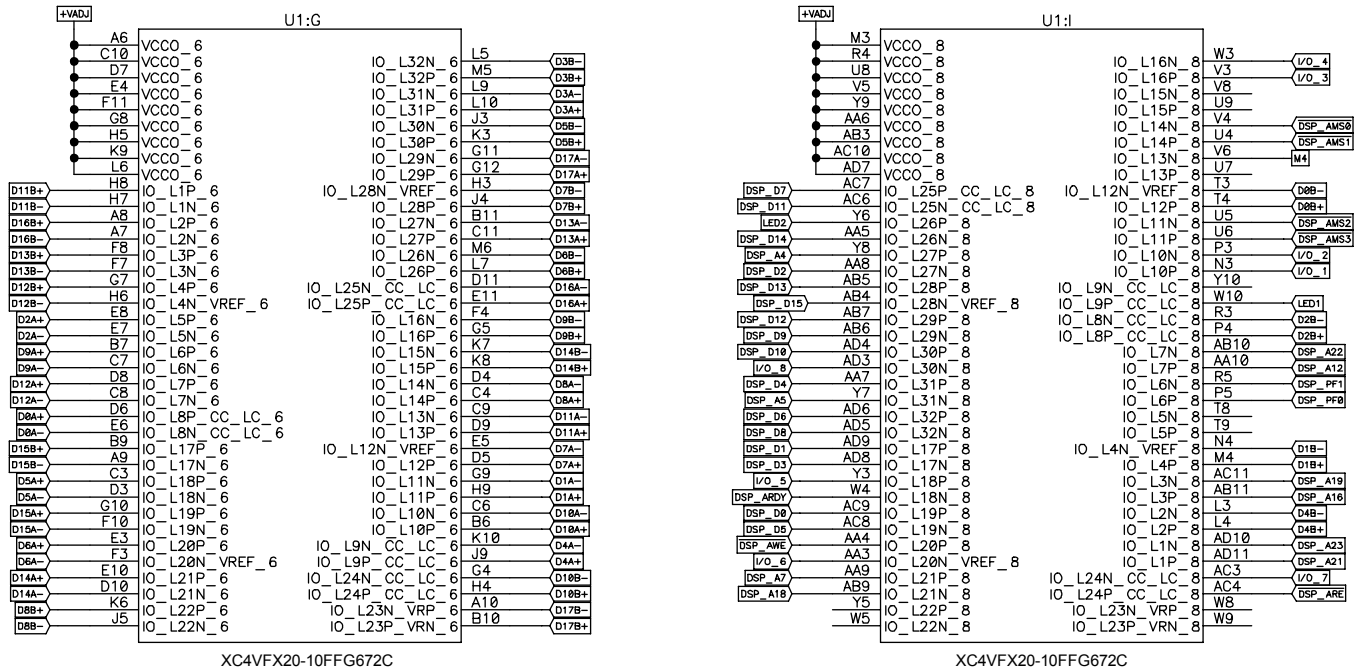


Figure 5.

## SRAM ADDRESS AND CONTROL

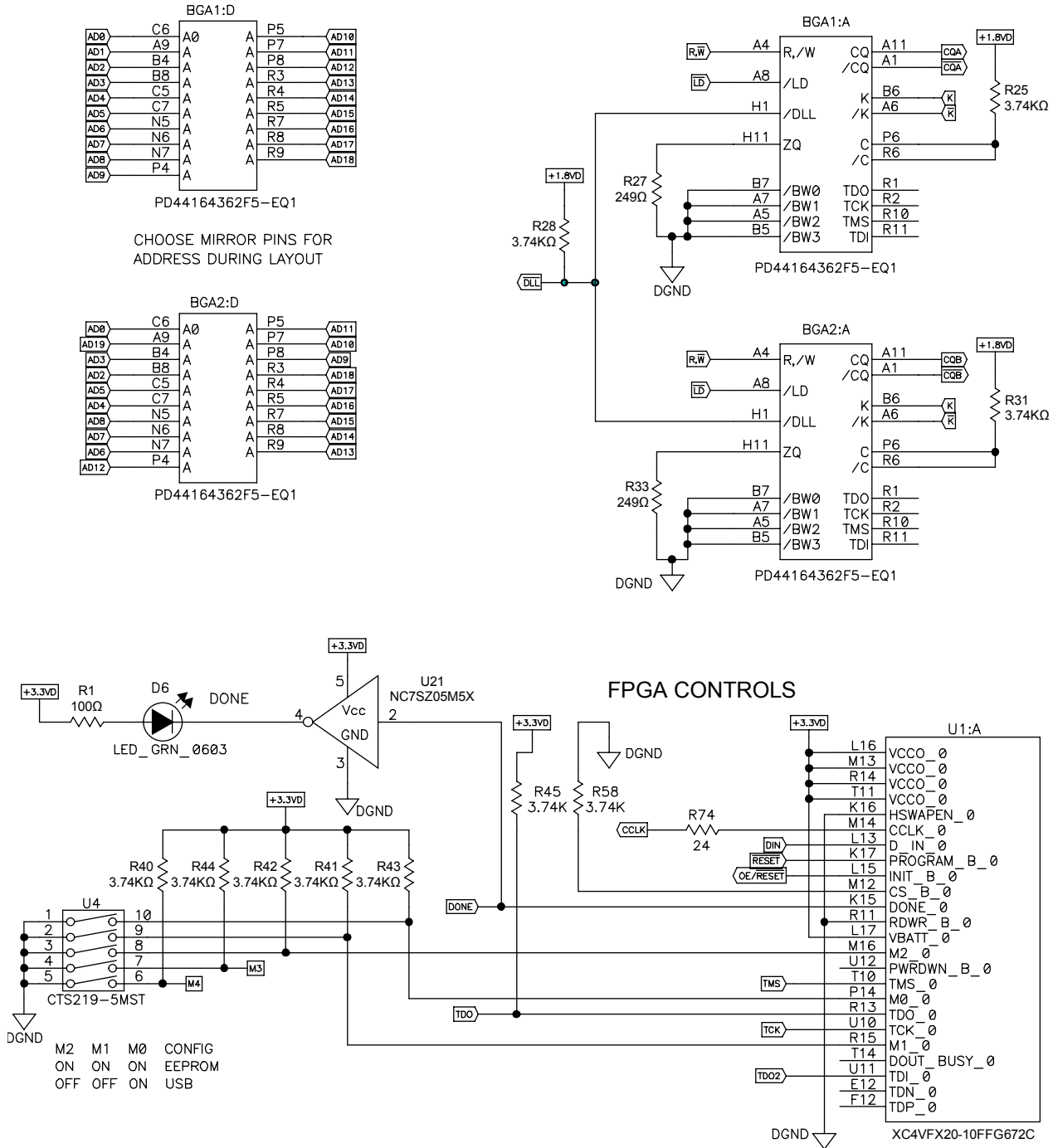


Figure 6.

## FPGA TO SRAM DATA

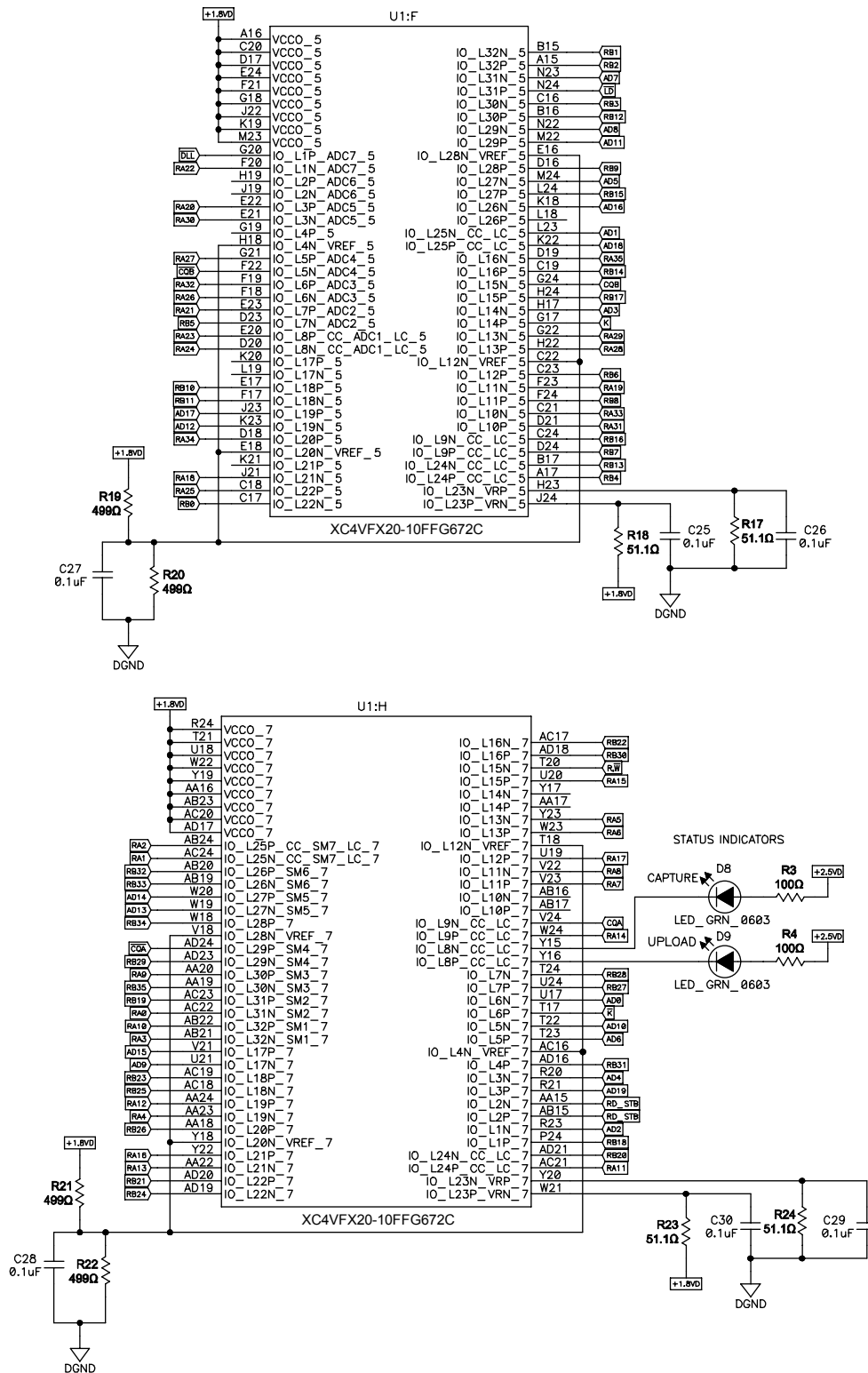


Figure 7.

06676-007

## AD19 TO BE USED WITH HIGHER DENSITY SRAM DEVICES

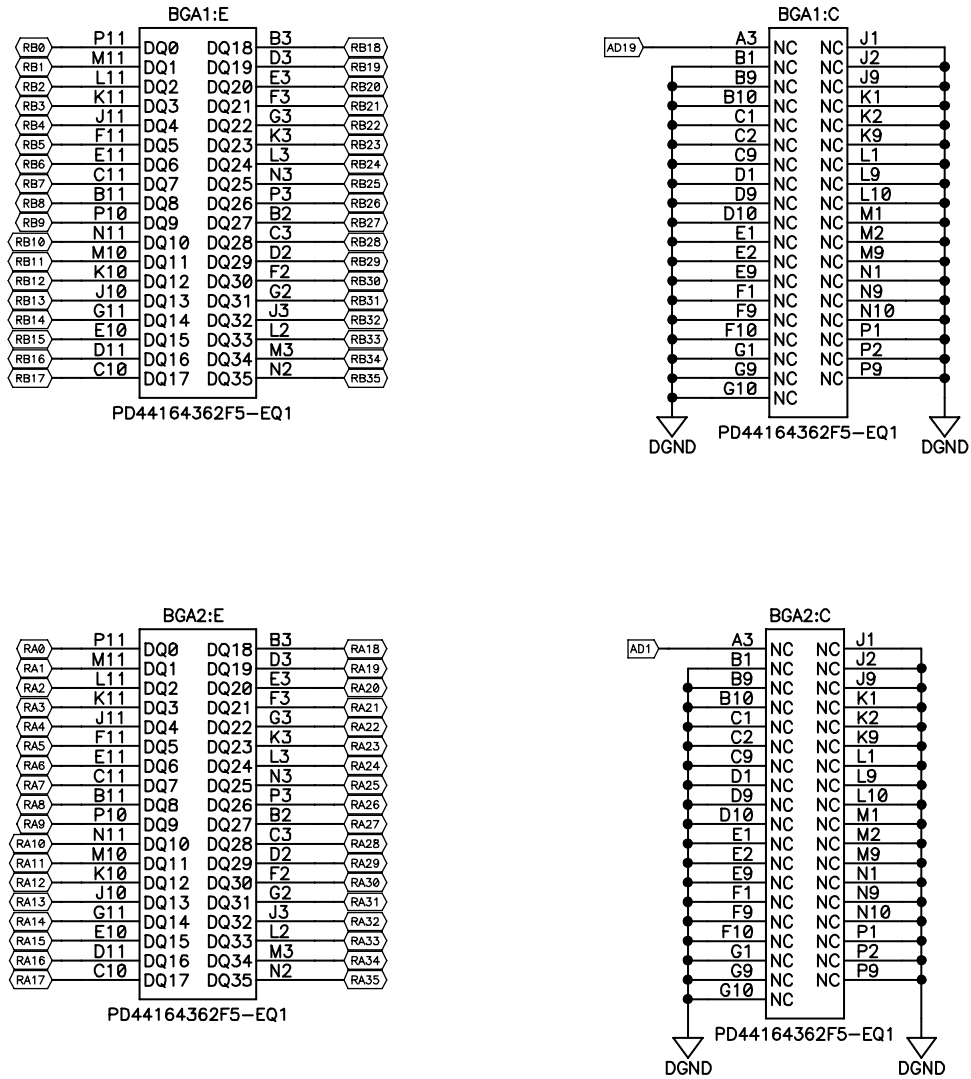


Figure 8.

066776-008



## SRAM AND FPGA POWER

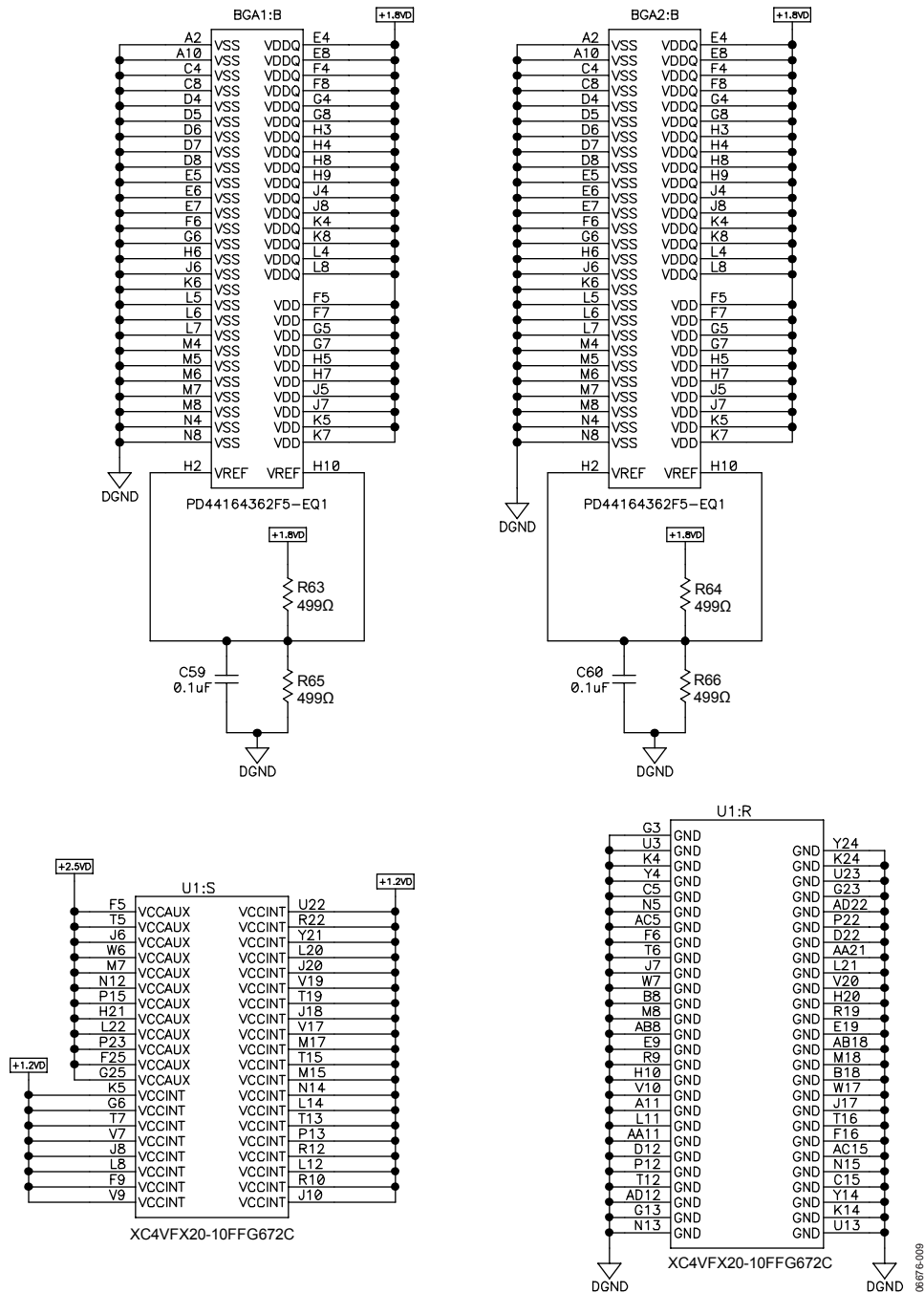
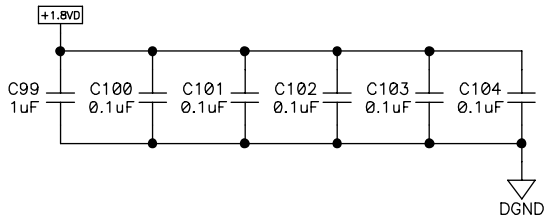


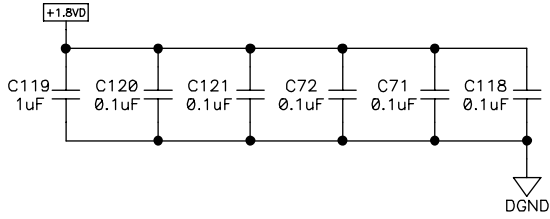
Figure 9.

# HSC-ADC-EVALC

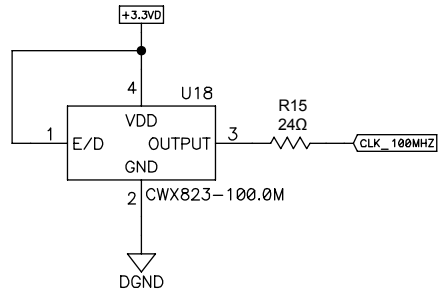
## SRAM A BYPASS CAP



## SRAM B BYPASS CAP



## REFCLK Oscillator for IDELAYCTRL



## FPGA BYPASS CAP

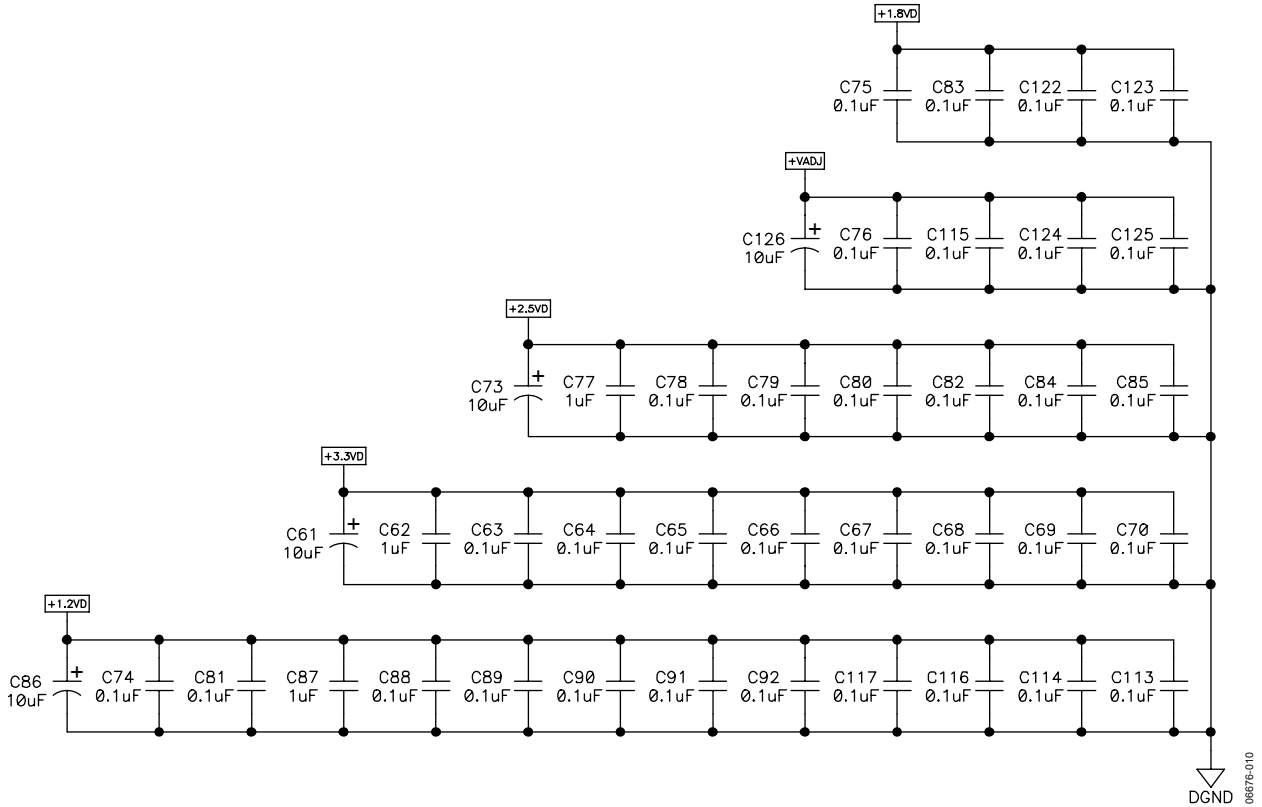
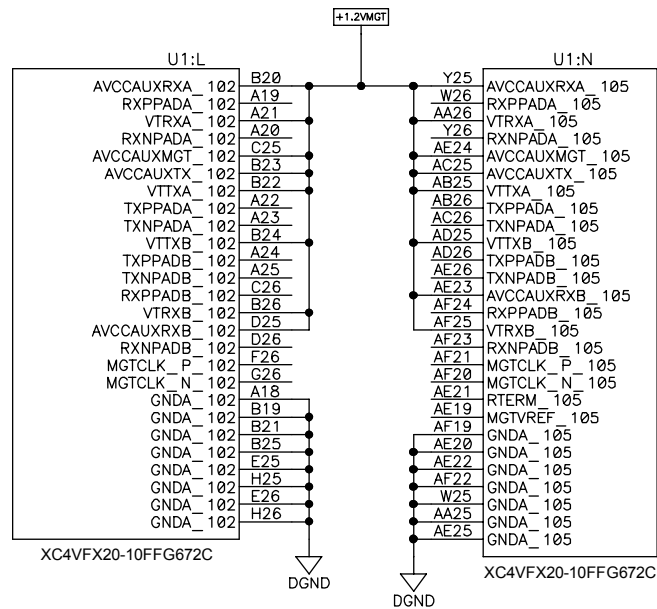


Figure 10.

## UNUSED ROCKET I/O CONNECTIONS



## DEBUG PINS

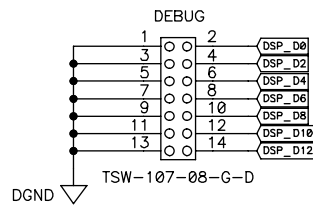


Figure 11.

06876-011



## USB CONNECTIONS

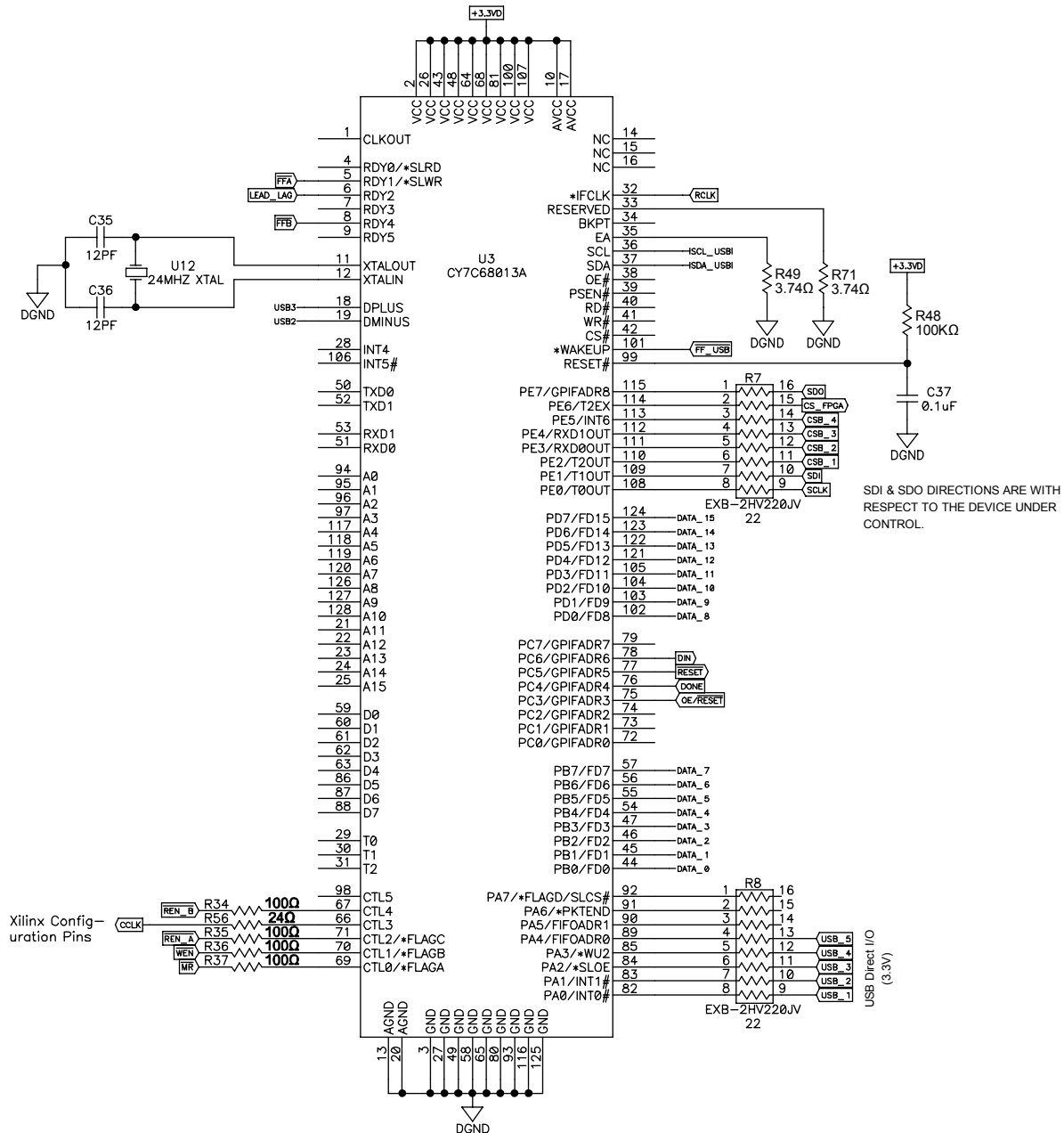


Figure 13.

06676-013



## USB CONNECTIONS (CONTINUED)

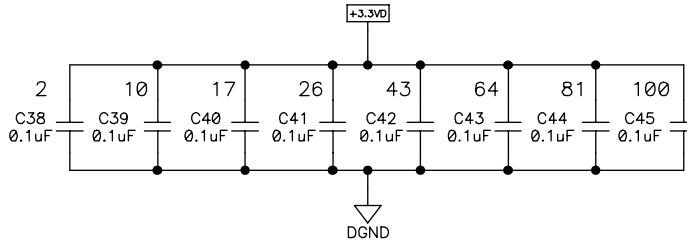
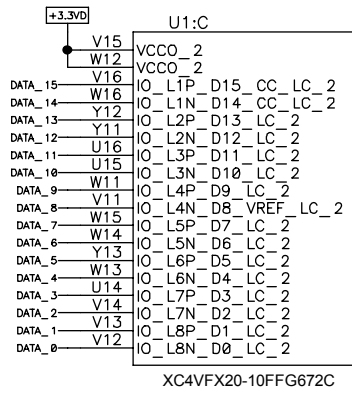
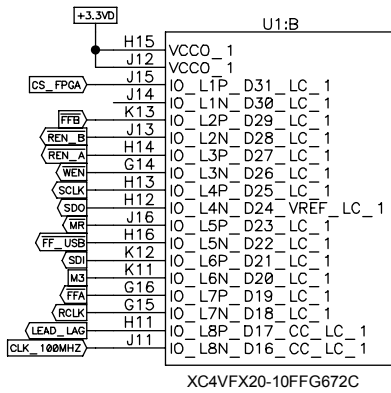
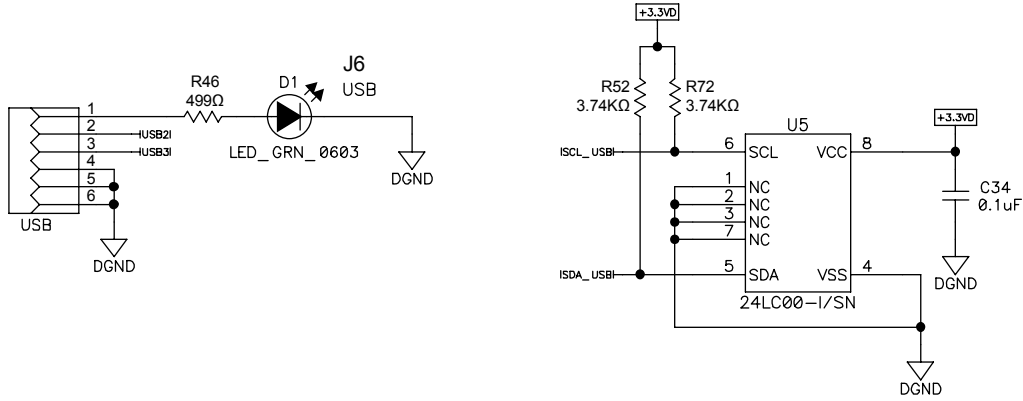


Figure 14.

06876-014

## EZ-KIT EXPANSION INTERFACE – FOR DSPs

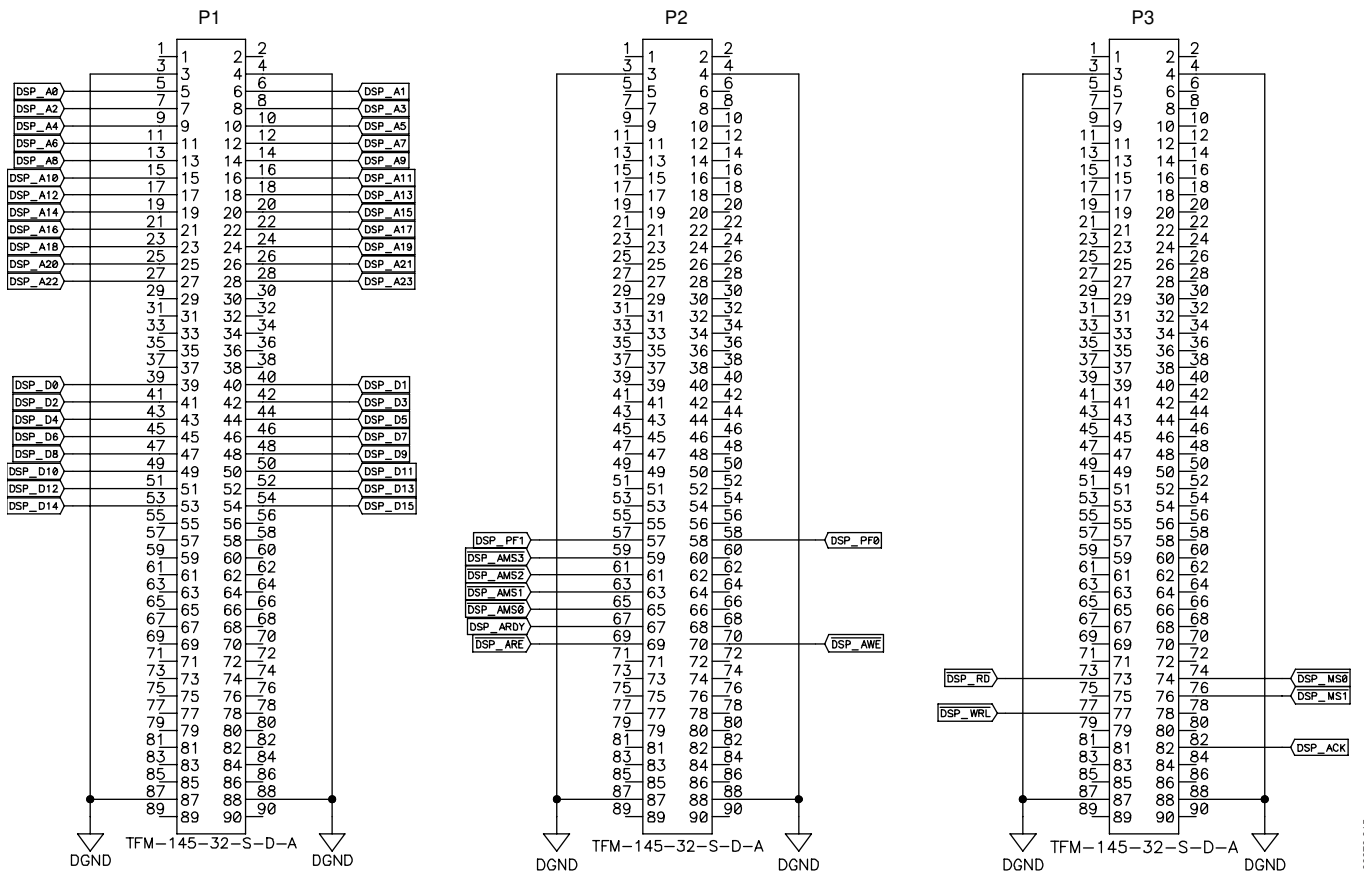
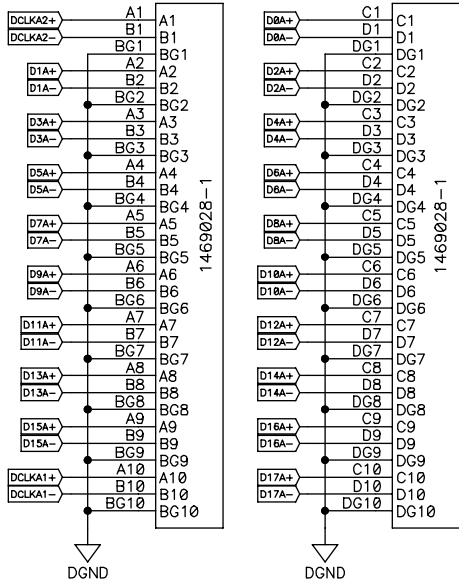


Figure 15.

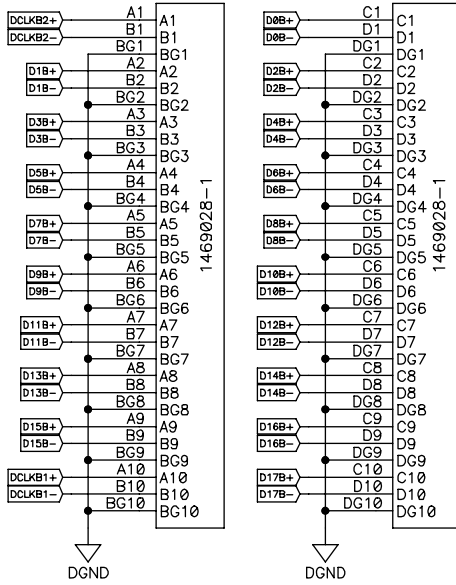
06876-015

TYCO HM – Zd CONNECTORS

J3  
DATA BUS 2



J2  
DATA BUS 1



J1  
HS-SERIAL/SPI/AUX

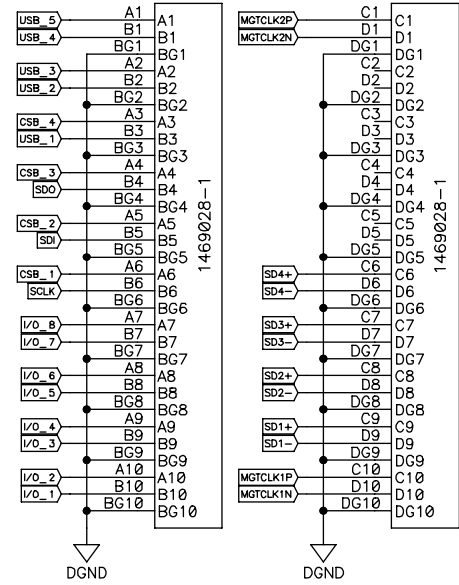
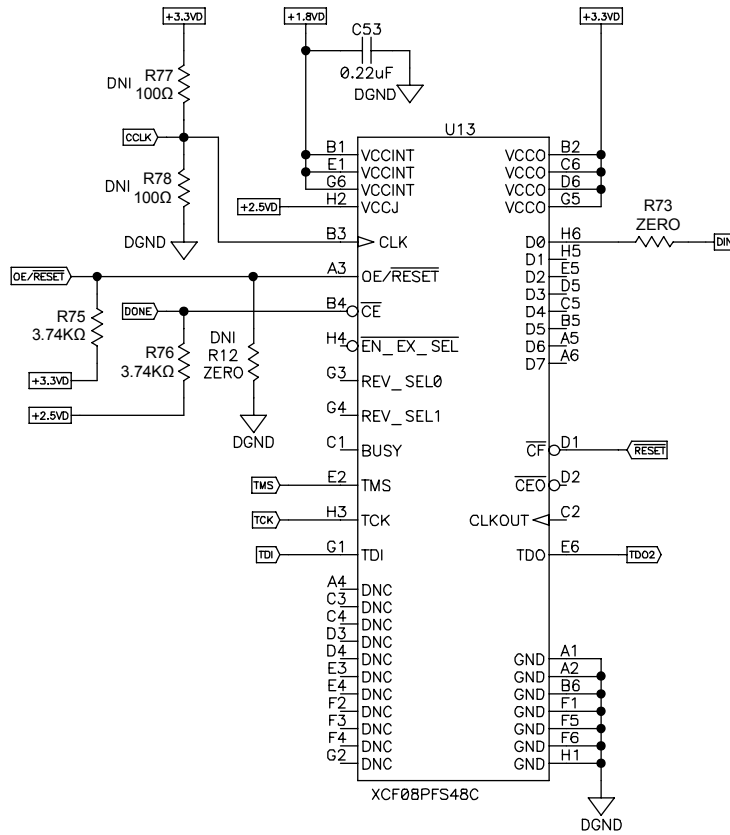
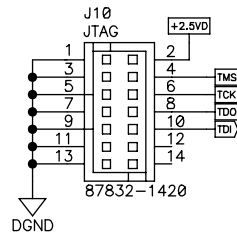


Figure 16.

CONFIGURATION EEPROM



JTAG CONNECTOR



EEPROM HARDWARE RECONFIGURATION PUSHBUTTON

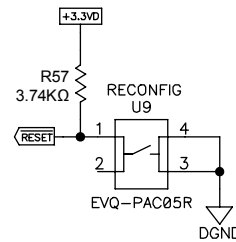


Figure 17.

08676-017

## POWER AND VOLTAGE REGULATORS

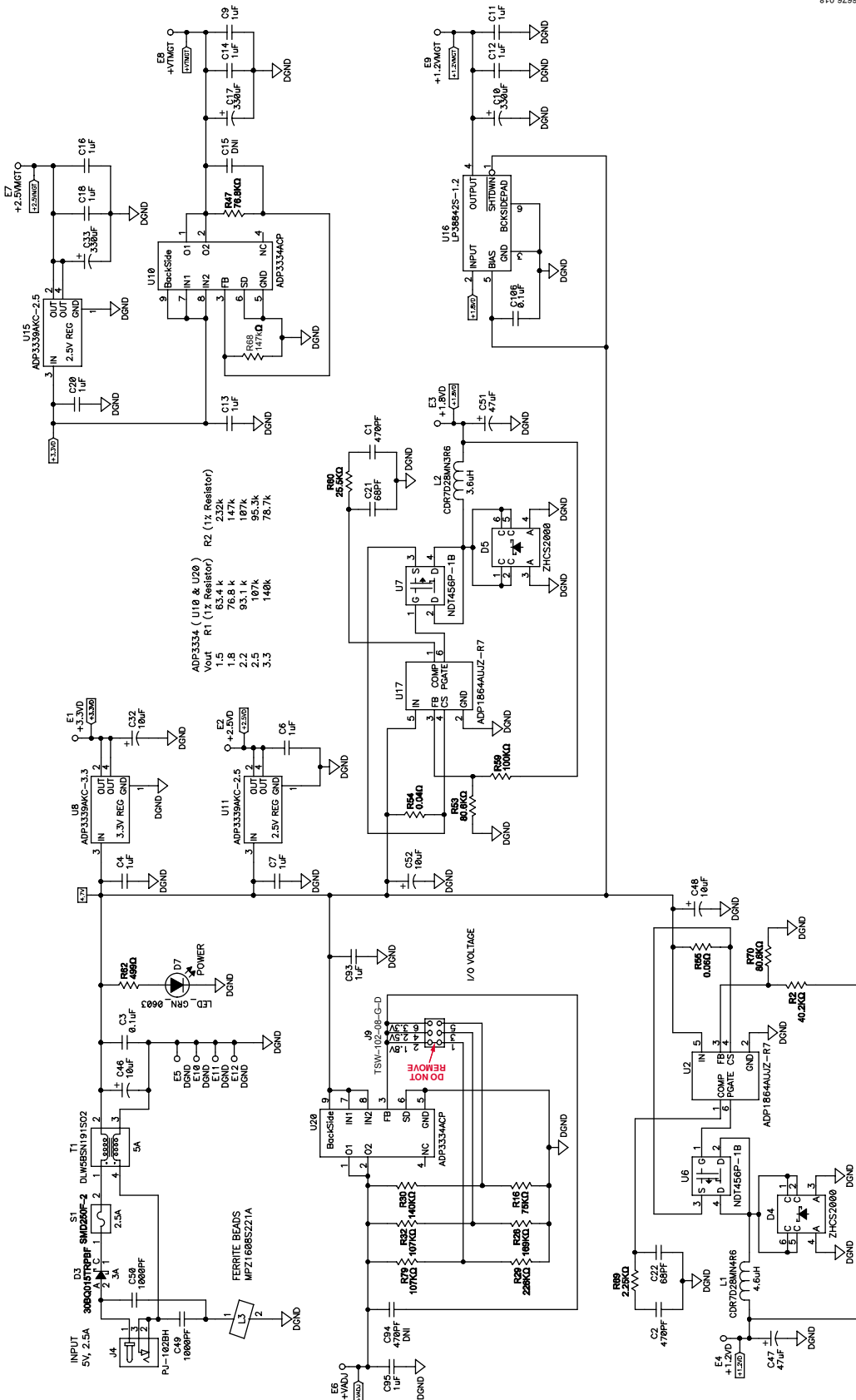
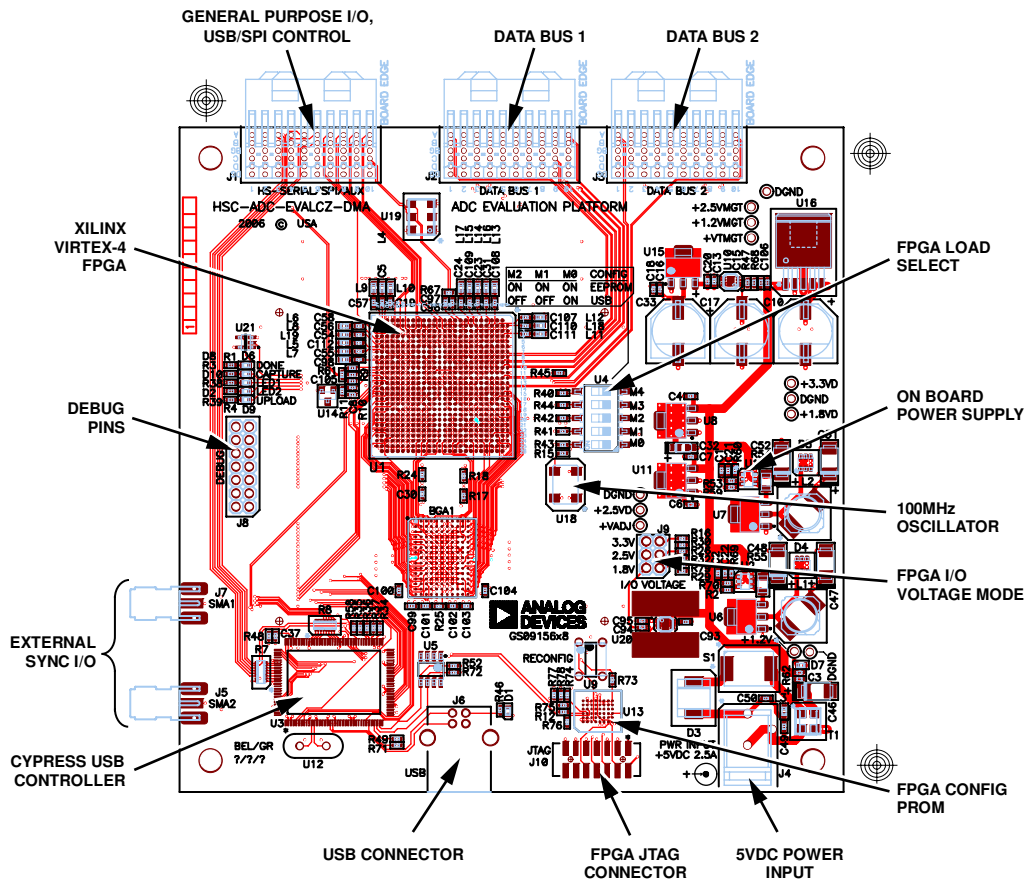


Figure 18.

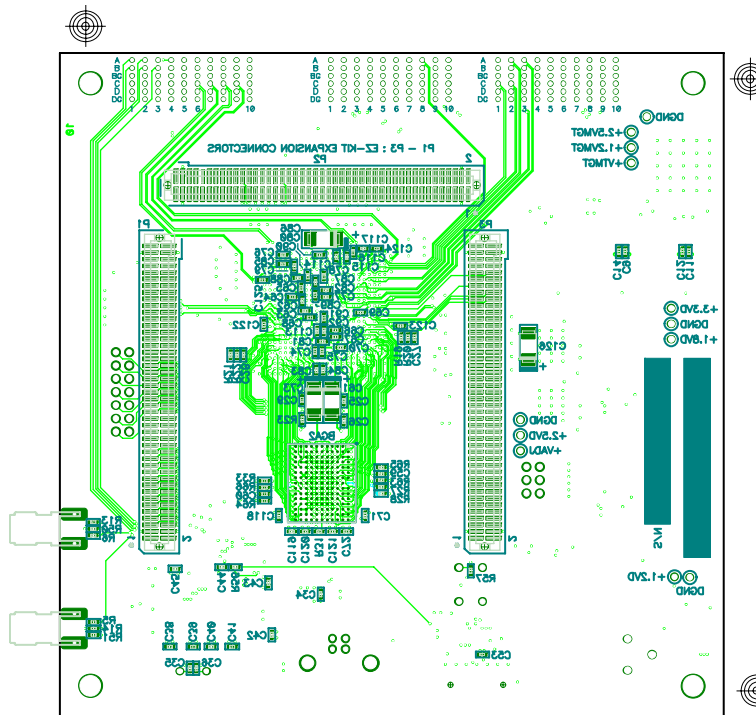


## PCB LAYOUT



06676-019

Figure 19. Top Silkscreen



06676-020

Figure 20. Bottom Silkscreen

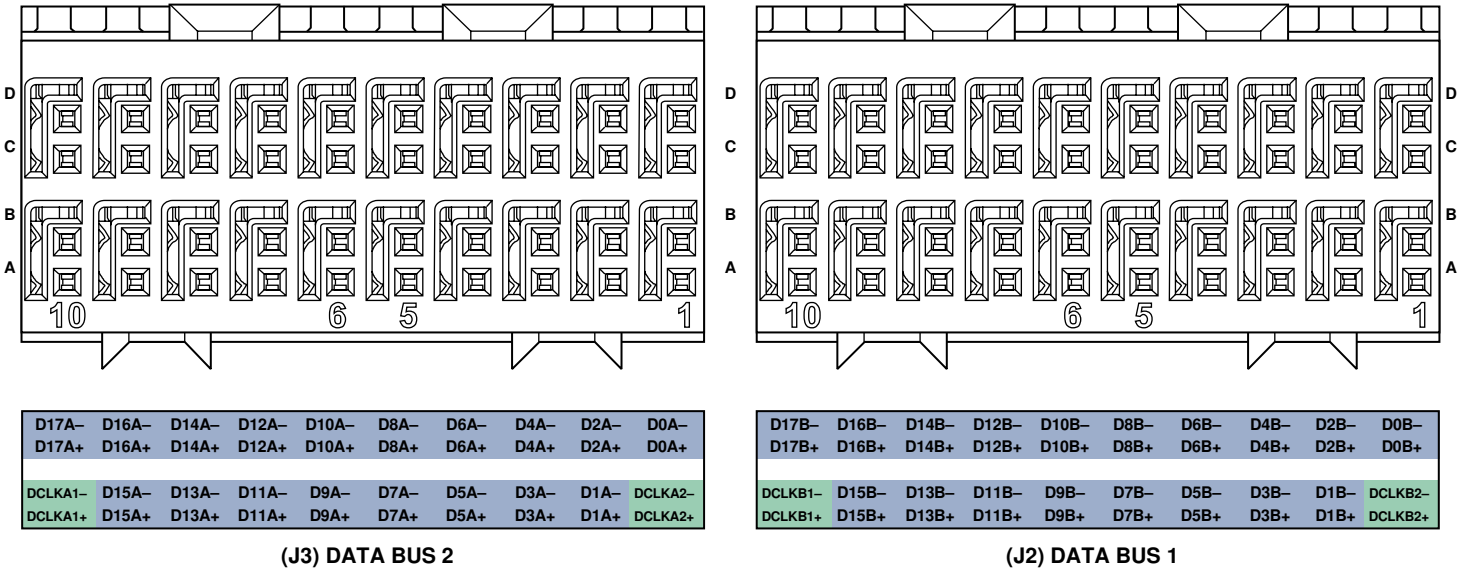


Figure 21. J2 and J3 Pin Mapping  
Rev. 0 | Page 24 of 32

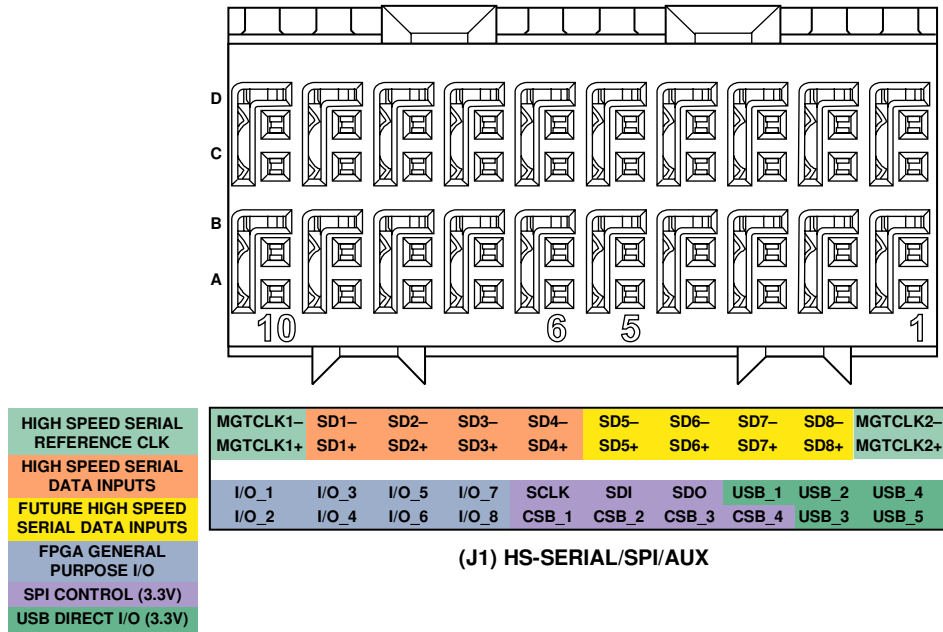


Figure 22. J1 Pin Mapping

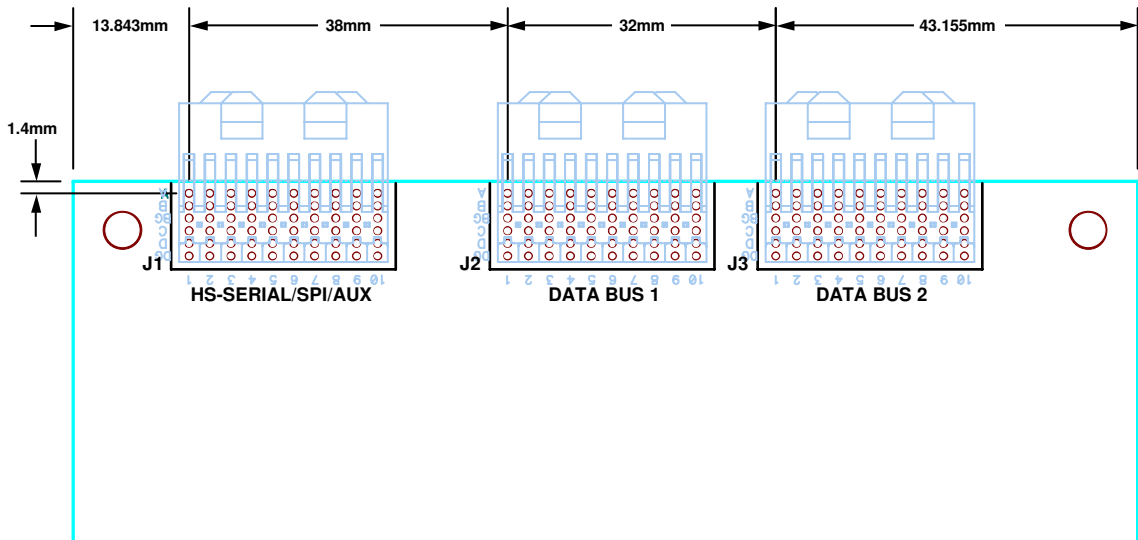


Figure 23. Data Converter I/O Connector Placement (Top View)