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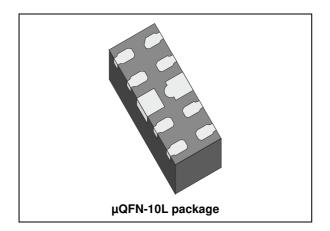




HSP061-4M10

Datasheet - production data

4-line ESD protection for high speed lines



Features

- Flow-through routing to keep signal integrity
- Ultralarge bandwidth: 8.7 GHz
- Ultralow capacitance: 0.3 pF
- Low leakage current: 70 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- Thin package: 0.5 mm max.
- RoHS compliant

Benefits

- High ESD robustness of the equipment
- Suitable for high density boards

Complies with following standards

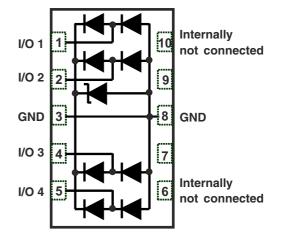
- MIL-STD 883G Method 3015-7 Class 3B:
 8 kV
- IEC 61000-4-2 level 4:
 - 8 kV (contact discharge)
 - 15 kV (air discharge)

Applications

The HSP061-4M10 is designed to protect against electrostatic discharge on sub micron technology circuits driving:

- HDMI 1.3 and 1.4
- Digital Video Interface
- Display Port
- USB 3.0
- Serial ATA
- Thunderbolt





Description

The HSP061-4M10 is a 4-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The ultralow variation of the capacitance ensures very low influence on signal-skew. The large bandwidth makes the device compatible with 3.4 Gbps.

The device is packaged in $\mu QFN\text{-}10L$ 2.5 x 1 mm with a 500 μm pitch, which minimizes the PCB area.

June 2014

This is information on a product in full production.

www.st.com

Characteristics 1

Symbol		Value	Unit
V _{PP}	Peak pulse voltage	8 20	kV
Тj	Operating junction tempe	-40 to +150	°C
T _{stg}	Storage temperature rang	-65 to +150	°C
TL	Maximum lead temperatu	260	°C

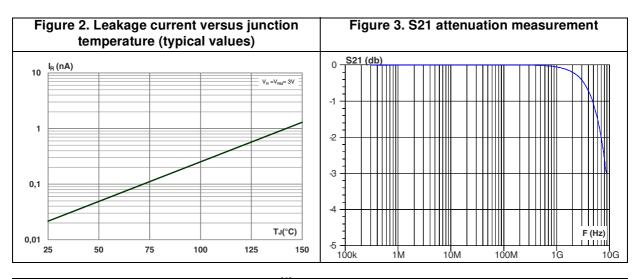
Table 1. Absolute maximum ratings T_{amb} = 25 °C

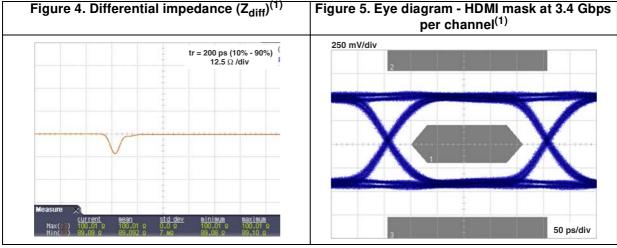
Table 2. E	lectrical characteristics T _{amb} = 25 °	°C	
Parameter	Test conditions	Min.	Тур.

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{BR}	Breakdown voltage	I _R = 1 mA	6			V
I _{RM}	Leakage current	V _{RM} = 3 V			70	nA
V _{CL}	Clamping voltage	IPP = 1 A, 8/20 μs			15	V
C _{I/O - I/O}	Capacitance (I/O to I/O)	$V_{I/O} = 0 V, F = 1 MHz, V_{OSC} = 30 mV$		0.3	0.4	pF
C _{I/O - GND}	Capacitance (I/O to GND)	$V_{I/O} = 0 V F = 1 MHz, V_{OSC} = 30 mV$		0.6	0.8	pF
f _C	Cut-off frequency	-3dB		8.7		GHz
Z _{Diff}	Differential impedance	t_r = 200 ps (10 - 90%) ⁽¹⁾ , Z _{0 Diff} = 100 Ω	85	100	115	Ω

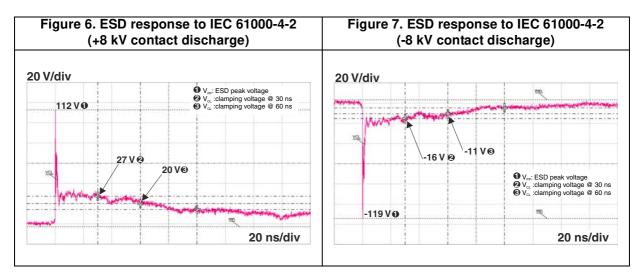
1. HDMI specification conditions. This information can be provided for other applications. Please contact your local ST office.







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2 Ordering information scheme

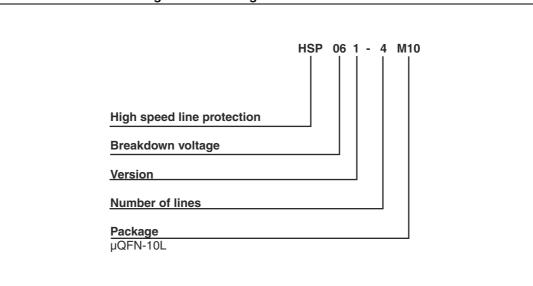


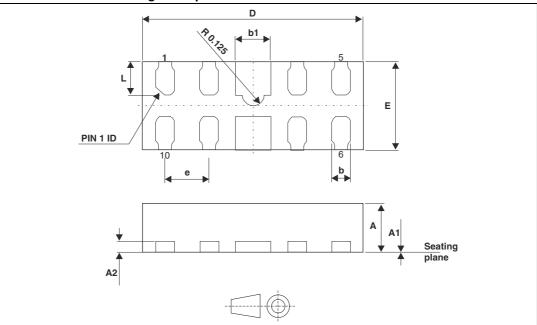
Figure 8. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK[®] is an ST trademark.



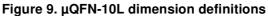


Table 3. µQFN-10L dimension values

	Dimensions					
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	0.40	0.48	0.50	0.018	0.019	0.020
A1	0.00	0.03	0.05	0.00	0.001	0.002
A2		0.13			0.005	
b	0.15	0.20	0.30	0.006	0.008	0.012
b1	0.35	0.40	0.45	0.014	0.016	0.041
D	2.40	2.50	2.60	0.094	0.098	0.102
Е	0.9	1.00	1.10	0.035	0.039	0.043
е		0.50			0.206	
L	0.30	0.38	0.425	0.012	0.015	0.017



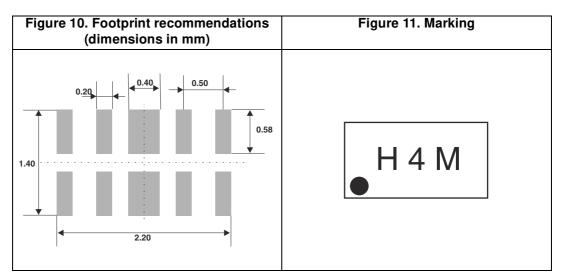
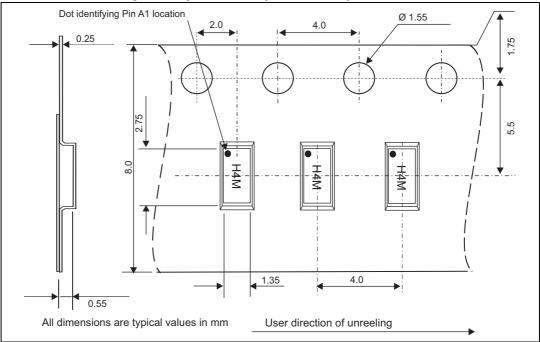


Figure 12. µQFN-10L tape and reel specification





4 Recommendation on PCB assembly

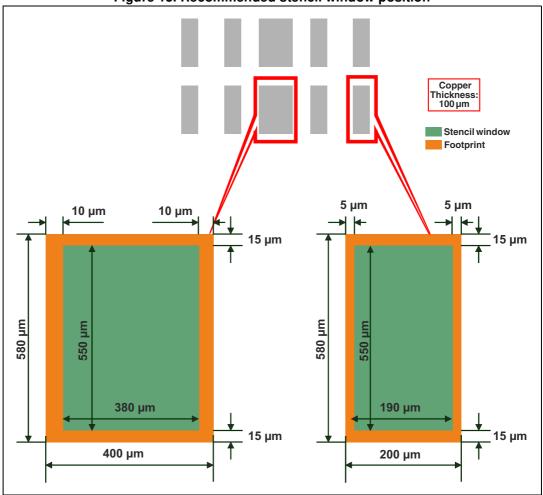


Figure 13. Recommended stencil window position

4.1 Solder paste

- 1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste recommended.
- 3. Offers a high tack force to resist component displacement during PCB movement.
- 4. Use solder paste with fine particles: powder particle size 20-45 $\mu m.$

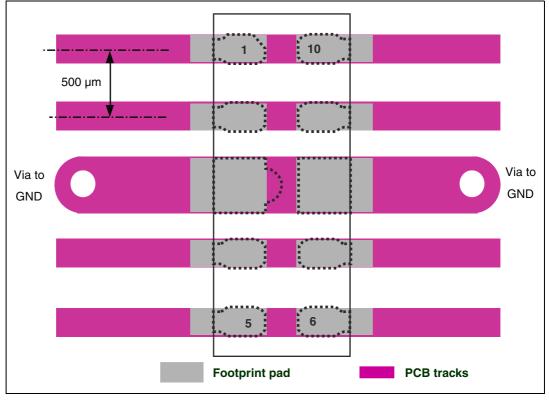


4.2 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
- 3. Standard tolerance of ± 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.3 PCB design

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.





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4.4 Reflow profile

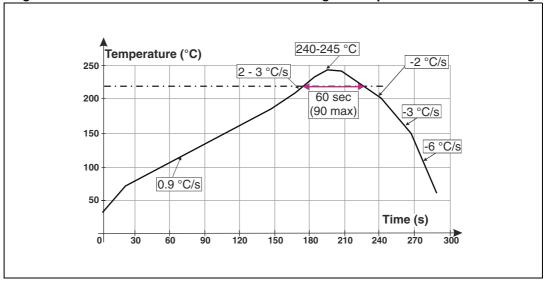


Figure 15. ST ECOPACK[®] recommended soldering reflow profile for PCB mounting

Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.



5 Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HSP061-4M10	H4M	µQFN-10L	3.27 mg	3000	Tape and reel

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
05-Sep-2012	1	Initial release.
18-Oct-2012	2	Updated V _{PP} in <i>Table 1</i> .
17-Jun-2014	3	Updated Figure 12 and reformatted to current standard.



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