Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
www.intersil.com/tsc

HSP50210

Digital Costas Loop

FN3652
Rev.5.00
Jul 2, 2008

Digital Costas Loop

The Digital Costas Loop (DCL) performs many of the baseband processing tasks required for the demodulation of BPSK, QPSK, 8-PSK, OQPSK, FSK, AM and FM waveforms. These tasks include matched filtering, carrier tracking, symbol synchronization, AGC, and soft decision slicing. The DCL is designed for use with the HSP50110 Digital Quadrature Tuner to provide a two chip solution for digital down conversion and demodulation.

The DCL processes the In-phase (I) and Quadrature (Q) components of a baseband signal which have been digitized to 10 bits. As shown in the block diagram, the main signal path consists of a complex multiplier, selectable matched filters, gain multipliers, cartesian-to-polar converter, and soft decision slicer. The complex multiplier mixes the I and Q inputs with the output of a quadrature NCO. Following the mix function, selectable matched filters are provided, which perform integrate and dump or root raised cosine filtering ($\alpha \sim 0.40$). The matched filter output is routed to the slicer, which generates 3-bit soft decisions, and to the cartesian-to-polar converter, which generates the magnitude and phase terms required by the AGC and Carrier Tracking Loops.

The PLL system solution is completed by the HSP50210 error detectors and second order Loop Filters that provide carrier tracking and symbol synchronization signals. In applications where the DCL is used with the HSP50110, these control loops are closed through a serial interface between the two parts. To maintain the demodulator performance with varying signal power and SNR, an internal AGC loop is provided to establish an optimal signal level at the input to the slicer and to the cartesian-to-polar converter.

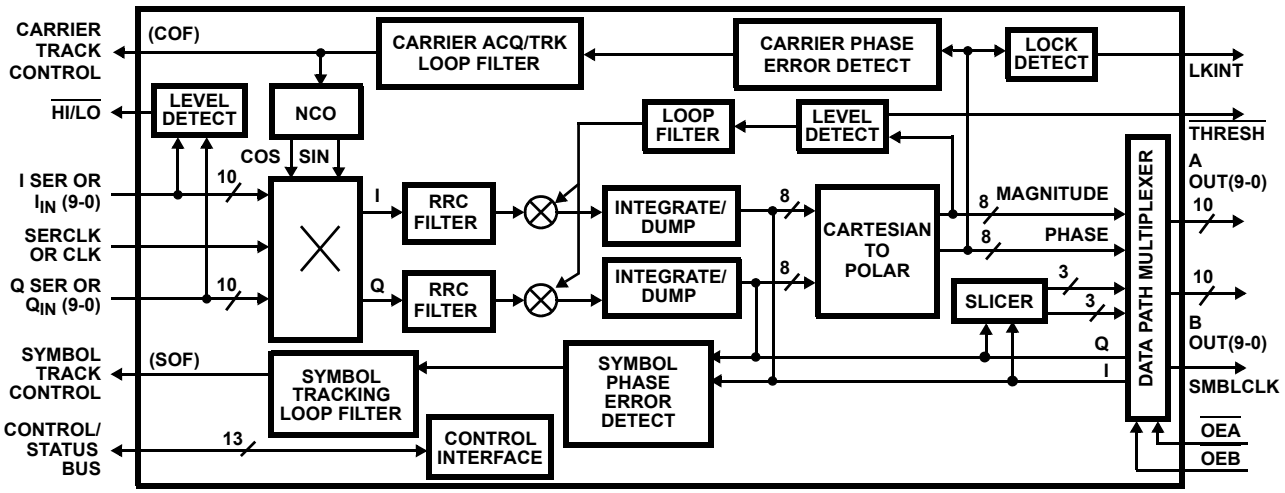
Features

- Clock Rates Up to 52MHz
- Selectable Matched Filtering with Root Raised Cosine or Integrate and Dump Filter
- Second Order Carrier and Symbol Tracking Loop Filters
- Automatic Gain Control (AGC)
- Discriminator for FM/FSK Detection and Discriminator Aided Acquisition
- Swept Acquisition with Programmable Limits
- Lock Detector
- Data Quality and Signal Level Measurements
- Cartesian-to-Polar Converter
- 8-Bit Microprocessor Control - Status Interface
- Designed to Work With the HSP50110 Digital Quadrature Tuner
- 84 Lead PLCC
- Pb-Free Available (RoHS compliant)

Applications

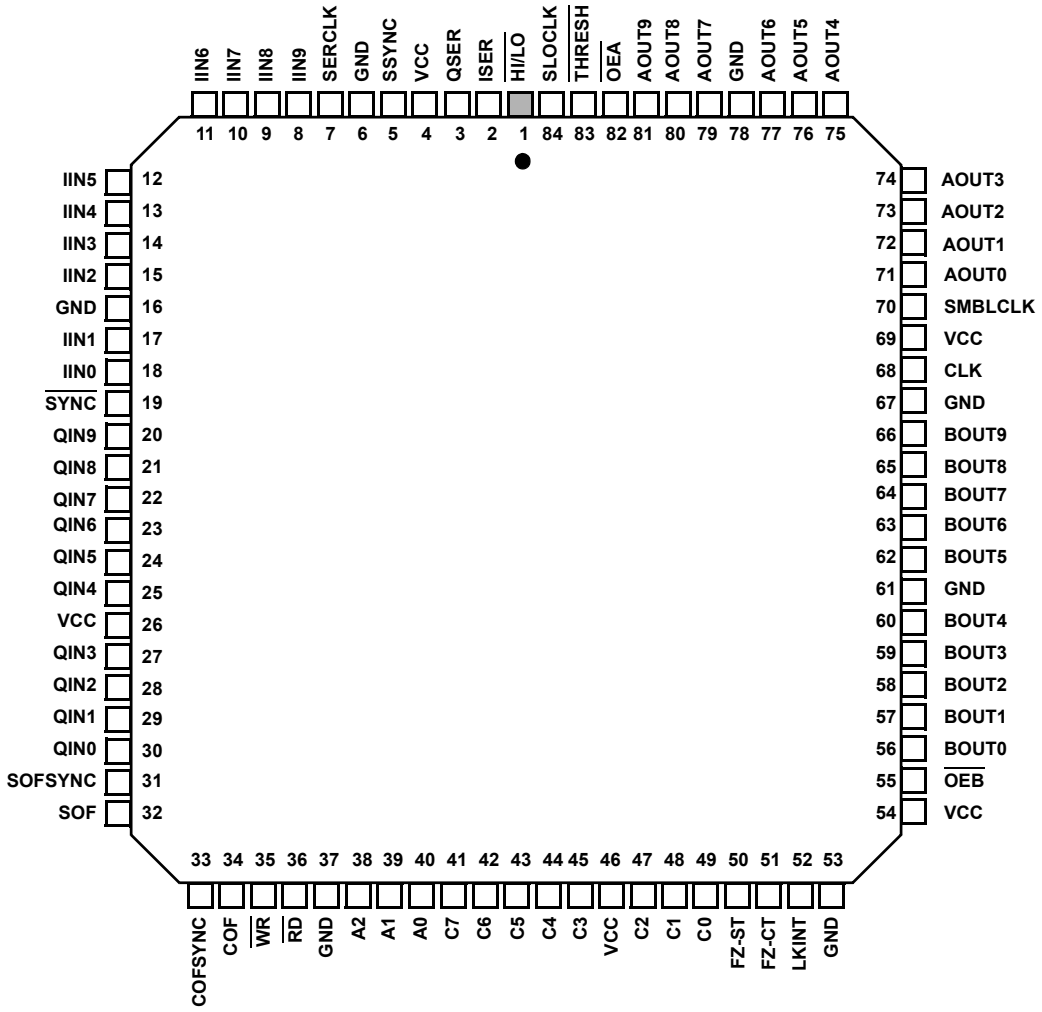
- Satellite Receivers and Modems
- BPSK, QPSK, 8-PSK, OQPSK, FSK, AM and FM Demodulators
- Digital Carrier Tracking
- Related Products: HSP50110 Digital Quadrature Tuner, D/A Converters HI5721, HI5731, HI5741
- HSP50110/210EVAL Digital Demod Evaluation Board

Block Diagram



Pinout

HSP50210
(84 LD PLCC)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HSP50210JC-52	HSP50210JC-52	0 to +70	84 Ld PLCC	N84.1.15
HSP50210JC-52Z (Note)	HSP50210JC-52Z	0 to +70	84 Ld PLCC (Pb-free)	N84.1.15
HSP50210JI-52	HSP50210JI-52	-40 to +85	84 Ld PLCC	N84.1.15
HSP50210JI-52Z (Note)	HSP50210JI-52Z	-40 to +85	84 Ld PLCC (Pb-free)	N84.1.15

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Description

NAME	TYPE	DESCRIPTION
VCC	-	+5V Power Supply.
GND	-	Ground.
IIN9-0	I	In-Phase Parallel Input. Data may be two's complement or offset binary format (see Table 15). These inputs are sampled by CLK when the $\overline{SYNC}$ signal is active Low. IIN9 is the MSB. See "Input Controller" on page 6.
QIN9-0	I	Quadrature Parallel Input. Data may be two's complement or offset binary format (see Table 15). These inputs are sampled by CLK when the $\overline{SYNC}$ signal is active Low. QIN9 is the MSB. "Input Controller" on page 6.
$\overline{SYNC}$	I	Data Sync. When $\overline{SYNC}$ is asserted "Low", data on IIN9-0 and QIN9-0 is clocked into the processing pipeline by the rising edge of CLK.
COF	O	Carrier Offset Frequency. The frequency term generated by the Carrier Tracking Loop Filter is output serially via this pin. The new offset frequency is shifted out MSB first by CLK or SLOCLK starting with the clock cycle after the assertion of COFSYNC.
COFSYNC	O	Carrier Offset Frequency Sync. This signal is asserted one CLK or SLOCLK cycle before the MSB of the serial data word. (Programmable Polarity, see Table 42 on page 42, Bit 11).
SOF	O	Sampler Offset Frequency. Sample frequency correction term generated by the Symbol Tracking Loop Filter is output serially via this pin. The frequency word is shifted out MSB first by CLK or SLOCLK starting with the clock cycle after assertion of SOFSYNC.
SOFSYNC	O	Sampler Offset Frequency Sync. This signal is asserted one CLK or SLOCLK cycle before the MSB of the serial data word. (Programmable Polarity, see Table 42 on page 42, Bit 12).
A2-0	I	Address Bus. The address on these pins specify a target register for reading or writing (see "Microprocessor Interface" on page 27). A0 is the LSB.
C7-0	I/O	Microprocessor Interface Data Bus. This bi-directional bus is used for reading and writing to the processor interface. These are the data I/O pins for the processor interface. C0 is the LSB.
$\overline{WR}$	I	Write. This is the write strobe for the processor interface (see "Microprocessor Interface" on page 27).
$\overline{RD}$	I	Read. This is the read enable for the processor interface (see "Microprocessor Interface" on page 27).
FZ_ST	I	Freeze Symbol Tracking Loop. Asserting this pin "high" zeroes the sampling error into the Symbol Tracking Loop Filter (see "Symbol Tracking Loop Filter" on page 17).
FZ_CT	I	Freeze Carrier Tracking Loop. Asserting this pin "high" zeroes the carrier Phase Error input to the Carrier Tracking Loop Filter.
LKINT	O	Lock Detect Interrupt. This pin is asserted "high" for at least 4 CLK cycles when the Lock Detector Integration cycle is finished (see "Lock Detector" on page 23). Used as an interrupt for a processor. The Lock Detect Interrupt may be asserted "high" longer than 4 CLK cycles, depending on the Lock Detector mode.
$\overline{THRESH}$	O	Threshold Exceeded. This output is asserted "low" when the magnitude out of the Cartesian to Polar converter exceeds the programmable Power Detect Threshold (see Table 16 on page 33 and "AGC" on page 10).
SLOCLK	O	Slow Clock. Optional serial clock used for outputting data from the Carrier and Symbol Tracking Loop Filters. The clock is programmable and has a 50% duty cycle. Note: Not used when the HSP50110 is used with the HSP50210 (see Table 42 page 42).
ISER	I	In-Phase Serial Input. Serial data input for In-Phase Data. Data on this pin is shifted in MSB first and is synchronous to SERCLK (see "Input Controller" on page 6).
QSER	I	Quadrature Serial Input. Serial data input for Quadrature Data. Data on this pin is shifted in MSB first and is synchronous to SERCLK (see "Input Controller" on page 6).
SSYNC	I	Serial Word Sync. This input is asserted "high" one CLK before the first data bit of the serial word (see Figure 2).
SERCLK	I	Serial Clock. May be asynchronous to other clocks. Used to clock in serial data (see "Input Controller" on page 6).
AOUT9-0	O	A Output. Data on this output depend on the configuration of Output Selector. AOUT9 is the MSB (see Table 43 on page 44).
BOUT9-0	O	B Output. Data on this output depend on the configuration of Output Selector. BOUT9 is the MSB (see Table 43 page 44).
SMBLCLK	O	Symbol Clock. 50% duty cycle clock aligned with soft bit decisions (see Figure 19).

Pin Description (Continued)

NAME	TYPE	DESCRIPTION
$\overline{OEA}$	I	A Output Enable. This pin is the three-state control pin for the AOUT9-0. When $\overline{OEA}$ is high, the AOUT9-0 is high impedance.
$\overline{OEB}$	I	B Output Enable. This pin is the three-state control pin for the BOUT9-BOUT0. When $\overline{OEB}$ is high, the AOUT9-0 is high impedance.
$\overline{HI/LO}$	0	HI/LO. The output of the Input Level Detector is provided on this pin (see “Input Level Detector” on page 6). This signal can be externally averaged and used to control the gain of an amplifier to close an AGC loop around the A/D converter. This type of AGC sets the level based on the median value on the input.
CLK	I	System Clock. Asynchronous to the processor interface and serial inputs.

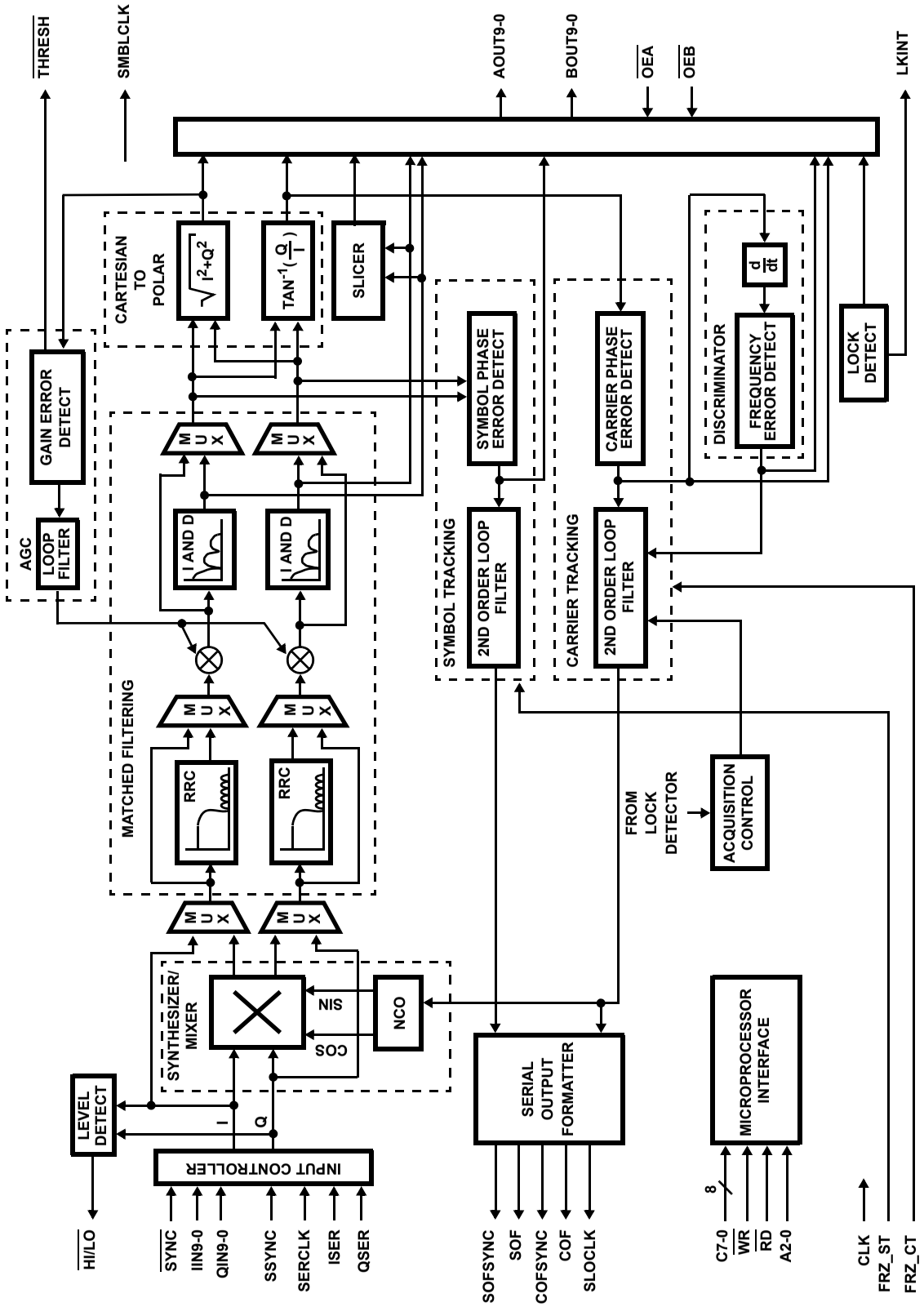


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE HSP50210

Functional Description

The HSP50210 Digital Costas Loop (DCL) contains most of the baseband processing functions needed to implement a digital Costas Loop Demodulator. These functions include LO generation/mixing, matched filtering, AGC, carrier phase and frequency error detection, timing error detection, carrier loop filtering, bit sync loop filtering, lock detection, acquisition/tracking control, and soft decision slicing for forward error correction algorithms. While the DCL is designed to work with the HSP50110 Digital Quadrature Tuner (DQT) as a variable rate PSK demodulator for satellite demodulation, functions on the chip are common to many communications receivers.

The DCL provides the processing blocks for the three tracking loops commonly found in a data demodulator: the Automatic Gain Control (AGC) loop, the Carrier Tracking Loop, and a Symbol Tracking Loop. The AGC loop adjusts for input signal power variations caused by path loss or signal-to-noise variations. The carrier tracking loop removes the frequency and phase uncertainties in the carrier due to oscillator inaccuracies and doppler. The symbol tracking loop removes the frequency and phase uncertainties in the data and generates a recovered clock synchronous with the received data. Each loop consists of an error detector, a loop filter, and a frequency or gain adjustment/control. The AGC loop is internal to the DCL, while the symbol and carrier tracking loops are closed external to the DCL. When the DCL is used together with the HSP50110, the tracking loops are closed around the baseband filtering to center the signal in the filter bandwidth. In addition, the AGC function is divided between the two chips with the HSP50110 providing the coarse AGC, and the HSP50210 providing the fine or final AGC.

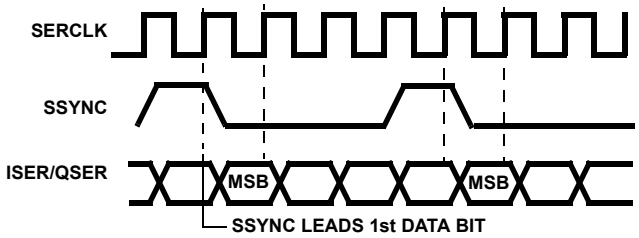
A top level block diagram of the HSP50210 is shown in Figure 1. This diagram shows the major blocks and the multiplexers used to reconfigure the data path for various architectures.

Input Controller

In-Phase (I) and Quadrature (Q) data enters the part through the Input Controller. The 10-bit data enters in either serial or parallel fashion using either two's complement or offset binary format. The input mode and binary format is set in the Data Path Configuration Control Register, bits 14 and 15 (see Table 15 on page 32).

If Parallel Input mode is selected, I and Q data are clocked into the part through IIN0-9 and QIN0-9 respectively. Data enters the processing pipeline when the input enable ($\overline{SYNC}$) is sampled "low" by the processing clock (CLK). The enable signal is pipelined with the data to the various processing elements to minimize pipeline delay where possible. As a result, the pipeline delay through the AGC, Carrier Tracking, and Symbol Tracking Loop Filters is measured in CLKs; not input data samples.

If serial input mode is selected, the I and Q data enters via the ISER and QSER pins using SERCLK and SSYNC. The beginning of a serial word is designated by asserting SSYNC 'high' one SERCLK prior to the first data bit, as shown in Figure 2. On the following SERCLKs, data is shifted into the register until all 10 bits have been input. Data shifting is then disabled and the contents of the register are held until the next assertion of SSYNC. The assertion of a SSYNC transfers data into the processing pipeline, and the Shift Register is enabled to accept new data on the following SERCLK. When data is transferred to the processing pipeline by SSYNC, a processing enable is generated which follows the data through the pipeline. This enable allows the delay through processing elements (like the loop filters) to be minimized since their pipeline delay is expressed in CLKs not SSYNC periods. ***Note: SSYNC should not be asserted for more than one SERCLK cycle***.



NOTE: Data must be loaded MSB first.

FIGURE 2. SERIAL INPUT TIMING FOR ISER AND QSER INPUTS

Input Level Detector

The Input Level Detector generates a one-bit error signal for an external IF AGC filter and amplifier. The error signal is generated by comparing the magnitude of the input samples to a user programmable threshold. The HI/LO pin is then driven "high" or "low" depending on the relationship of its magnitude to the threshold. The sense of the HI/LO pin is programmable so that a magnitude exceeding the threshold can either be represented as a "high" or "low" logic state. The Input Level Detector (HI/LO output) threshold and the sense are set by the Data Path Configuration Control Register bits 16 to 23 and 13 (see Table 15 page 32). ***Note: The Input Level Detector is typically not used in applications which use the HSP50210 with the HSP50110.***

The high/low outputs can be integrated by an external loop filter to close an AGC loop. Using this method, the gain of the loop forces the median magnitude of the input samples to the threshold. When the magnitude of half of the samples is above the threshold (and half is below), the error signal is integrated to zero by the loop filter. The magnitude of the complex input is estimated using Equation 1:

$$\text{Mag (I, Q)} = |I| + 0.375 \times |Q| \text{ if } I > Q \text{ and} \quad \text{(EQ. 1)}$$

$$\text{Mag (I, Q)} = |Q| + 0.375 \times |I| \text{ if } Q > I$$

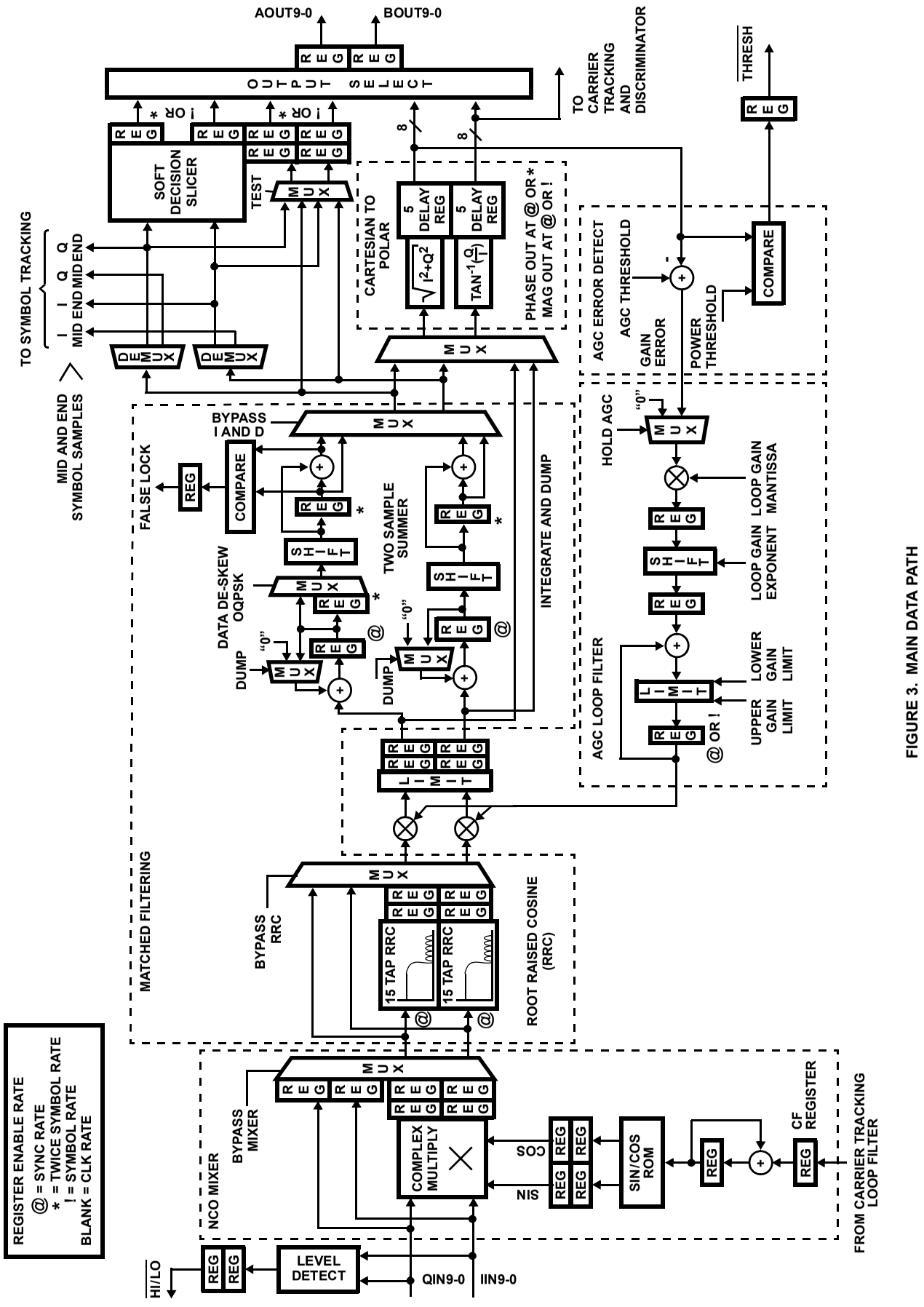


FIGURE 3. MAIN DATA PATH

NCO/Mixer

The NCO/Mixer performs a complex multiply between the baseband input and the output of a quadrature NCO (Numerically Controlled Oscillator). When the HSP50210 (DQT) is used with the HSP50110 (DCL), the NCO/Mixer shortens the Carrier Tracking Loop (i.e., minimizes pipeline delay around the loop) while providing wide loop bandwidths. This becomes important when operating at symbol rates near the maximum range of the part.

There are three configurations possible for closing the Carrier Tracking Loop when the DQT and the DCL are used together. The first configuration utilizes the NCO on the DQT and bypasses the NCO in the DCL. The Data Path Configuration Control Register (see Table 15 on page 32), Bit 10, and Carrier Loop Filter Control Register #1 (see Table 21 on page 34), Bit 6, are used to bypass the DCL NCO/Mixer and route the Loop filter outputs, respectively. The DQT provides maximum flexibility in NCO control with respect to frequency and phase offsets.

The second configuration feeds the lead Carrier Loop filter term to the DCL NCO/Mixer, and the lag Loop filter Term to the DQT NCO. This reduces the loop transport delay while maintaining wide loop bandwidths and reasonable loop damping factors. This configuration is especially useful in SATCOM applications with medium to high symbol rates. The Carrier Loop Filter Control Register #1, Bit 5 is where the lead/lag destination is set.

The final configuration feeds both the lead and lag Carrier Loop Filter terms back to the DCL NCO/Mixer. This provides the shortest transport delay. The DCL NCO/Mixer provides only for frequency/phase control from the Carrier Loop filter. The center frequency of this NCO/Mixer is set to the average of the Upper and Lower Carrier Loop Limits programmable parameters. These parameters are set in the two control registers bearing their names (see Tables 23 and 24 on page 35).

The NCO/Mixer uses a complex multiplier to multiply the baseband input by the output of a quadrature NCO. This operation is represented by Equations 2 and 3:

$$I_{OUT} = I_{IN}\cos(\omega_C) - Q_{IN}\sin(\omega_C) \quad \text{(EQ. 2)}$$

$$Q_{OUT} = I_{IN}\sin(\omega_C) + Q_{IN}\cos(\omega_C) \quad \text{(EQ. 3)}$$

Equation 3 illustrates how the complex multiplier implicitly performs the summing function when the DCL is configured as a modulator. The quadrature outputs of the NCO are generated by driving a sine/cosine look-up table with the output of a phase accumulator, as shown in Figure 3 on page 7. Each time the phase accumulator is clocked, its sum is incremented by the contents of the Carrier Frequency (CF) Register. As the accumulator sum increments from 0 to 2^{32}, the SIN/COS ROM produces quadrature outputs whose phase advances from 0 to 360°. The CF Register contains a 32-bit phase increment, which is updated with the output of Carrier Tracking Loop. Large phase increments take fewer clocks to step through the sine wave cycle, which results in a higher frequency NCO output.

The CF Register sets the NCO frequency using Equation 4:

$$F_C = f_{CLK} \times (CF)/2^{32} \quad \text{(EQ. 4)}$$

$$CF = INT[(F_C/f_{CLK})2^{32}]H$$

where f_{CLK} is the CLK frequency, and CF is the 32-bit two's complement hexadecimal value loaded into the Carrier Frequency Register. As an example, if the CF Register is loaded with a value of 4000 0000 (Hex), and the CLK frequency is 40MHz, the NCO would produce quadrature terms with a frequency of 10MHz. When CF is a negative value, a clockwise cos/sin vector rotation is produced. When CF is positive, a counterclockwise vector rotation is produced.

Note: The NCO is set to a fixed frequency by programming the upper and lower limits of the Carrier Tracking Loop Filter to the same value and zeroing the lead gain.

Matched Filtering

The HSP50210 provides two selectable matched filters: a Root Raised Cosine Filter (RRC) and an Integrate and Dump (I and D) filter. These are shown in Figure 3. The RRC filter is provided for shaped data pulses and the I and D filter is provided for square wave data. The filters may be cascaded for better adjacent channel rejection for square wave data. If these two filters do not meet baseband filtering requirements, then they can be bypassed and an external digital filter (such as the HSP43168 Dual FIR Filter or the HSP43124 Serial I/O Filter) used to implement the desired matched filter. The desired filter configuration is set in the Data Path Configuration Control Register, bits 1 through 7 (see Table 15 on page 32).

The sample rate of the baseband input depends on the symbol rate and filtering configuration chosen. In configurations which bypass both filters or use only the RRC Filter, the input sample rate must be twice the symbol rate. In configurations which use the I and D Filter, the input sample rate is decimated by the I and D Filter, down to two samples per symbol. I and D configurations support input sample rates up to 32x the input symbol rate.

The RRC filter is a fixed coefficient 15 Tap FIR filter. It has ~40% excess bandwidth beyond Nyquist, which equates to α = ~0.4 shape factor. The filter frequency response is shown in Figures 4 and 5. In addition, the 9-bit filter coefficients are listed as integer values in Table 1. The noise equivalent bandwidth of the RRC filter and other filter configurations possible with the HSP50110/210 chipset are given in Appendix A.

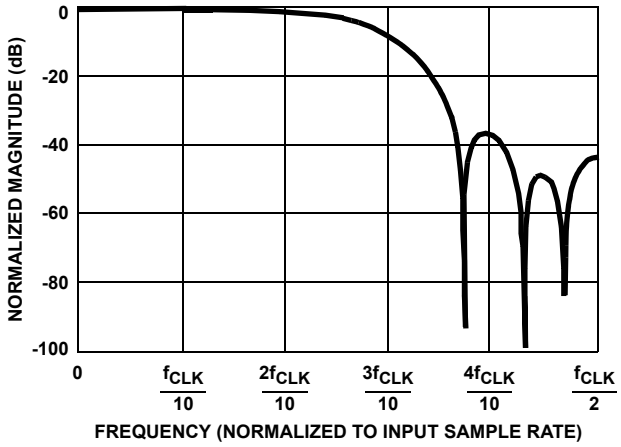


FIGURE 4. RRC FILTER IN HSP50210

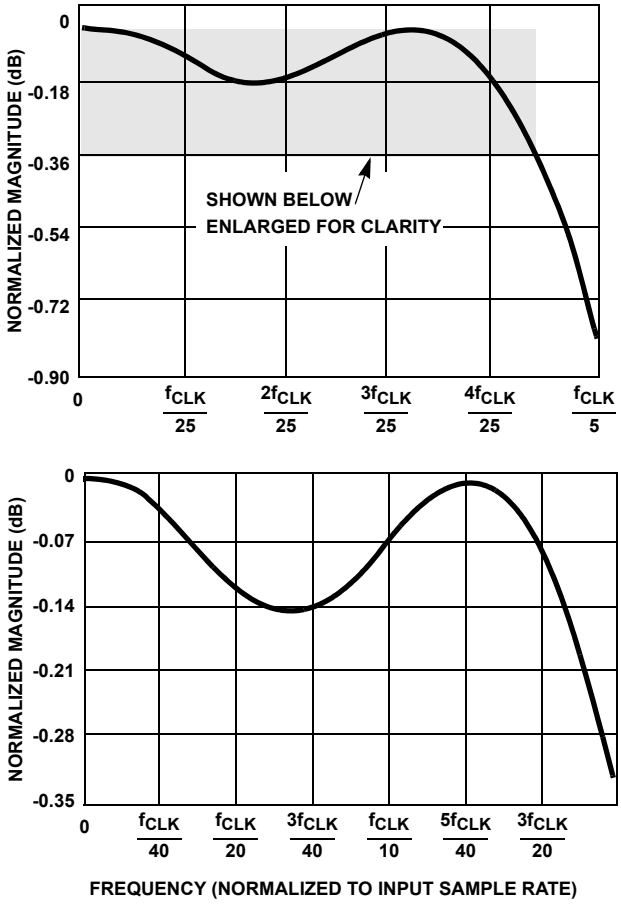


FIGURE 5. PASSBAND RIPPLE OF RRC FILTER IN HSP50210

TABLE 1. ROOT RAISED COSINE COEFFICIENTS

COEFFICIENT INDEX	COEFFICIENT
0	2
1	-2
2	1
3	8
4	-16
5	-14
6	86
7	160
8	86
9	-14
10	-16
11	8
12	1
13	-2
14	2

The I and D filter consists of an accumulator, a programmable shifter and a two sample summer, as shown in Figure 3. The programmable shifter is provided to compensate for the gain introduced by the accumulator (see Table 15). The accumulator provides Integrate and Dump Filtering for decimation factors up to 16. The two sample summer provides the moving average required for an additional decimation factor of 2. A decimation factor of 1 (bypass), 2, 4, 8, 16, or 32 may be selected. At the maximum decimation rate, a baseband signal sampled at 32x the symbol rate can be filtered.

The output of the two sample summer is demultiplexed into two sample streams at the symbol rate. The demultiplexed data streams from the I and Q processing paths are fed to the Symbol Tracking Block and Soft decision slicer. The multiplexed data streams on I and Q are provided as one of the selectable inputs for the Cartesian-to-Polar Converter.

Cartesian/Polar Converter

The Cartesian/Polar Converter maps samples on the I and Q processing paths to their equivalent phase/magnitude representation. The magnitude conversion is equivalent to Equation 5:

$$\text{Mag}(I, Q) = (0.81)*\sqrt{(I^2 + Q^2)} \quad \text{(EQ. 5)}$$

where 0.81 is the gain of the conversion process. The magnitude output is an 8-bit unsigned value ranging from 0.0 to 1.9922.

The phase conversion is equivalent to Equation 6:

$$\text{Phase (I, Q)} = \tan^{-1}(Q/I), \quad \text{(EQ. 6)}$$

where $\tan^{-1}( )$ is the arctangent function. The phase conversion output is an 8-bit two's complement output, which ranges from -1.0 to 0.9922 (80 to 7f HEX, respectively). The -1 to almost 1 range of the phase output represents phase values from -π to π, respectively. An example of the I/Q to phase mapping is shown in Figures 6A through 6C. The phase and magnitude values may be output via the Output Selector bits 0 through 3 (see Table 43).

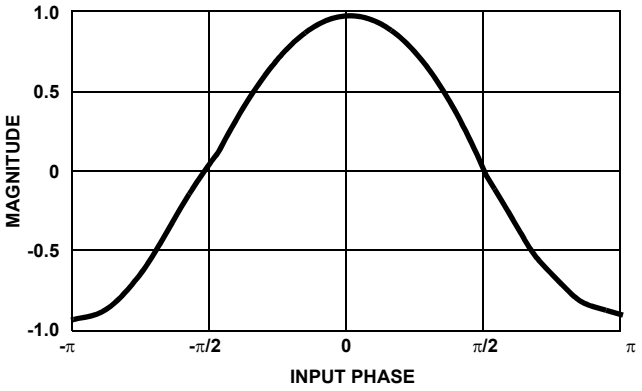


FIGURE 6A. I INPUT TO CARTESIAN/POLAR CONVERTER

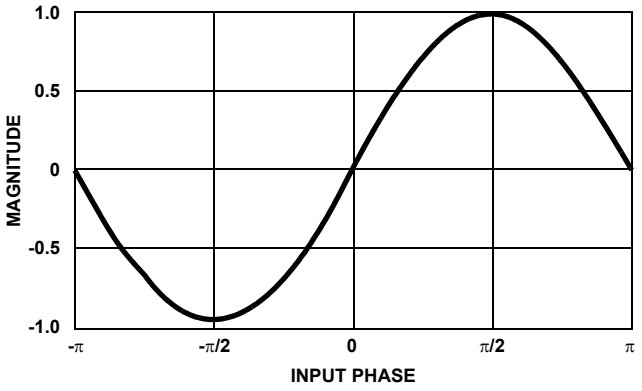


FIGURE 6B. Q INPUT TO CARTESIAN/POLAR CONVERTER

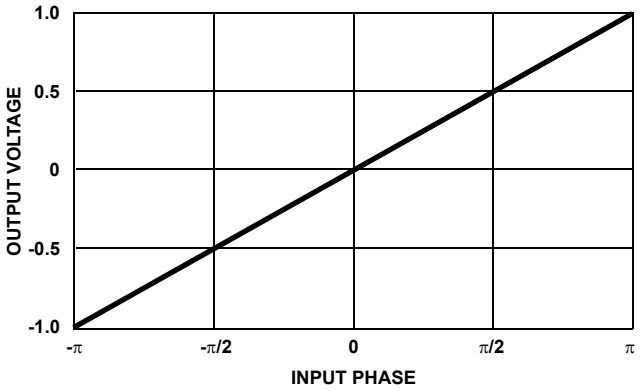


FIGURE 6C. CARTESIAN/POLAR CONVERTER PHASE OUTPUT

The I/Q data path selected for input to the Cartesian-to-Polar converter determines the input data rate of the AGC and carrier tracking loops. If the I/Q data path out of the Integrate and Dump Filter is selected, the AGC is fed with magnitude values produced by the end-symbol samples. Magnitude values produced by midsymbol samples are not used because these samples occur on symbol transitions, resulting in poor signal magnitude estimates. The Carrier Tracking block is fed with phase values generated from both the end and mid-symbol samples. The carrier tracking loop filter, however, is only fed with Phase Error terms generated by the end symbol samples. If the input of the I and D is selected for input to the coordinate converter, the control loops are fed with data at the I/Q data rate. The desired data path input to the Cartesian to Polar converter is specified in the Data Path Configuration Control Register, Bit 8 (see Table 15 on page 32).

AGC

The AGC loop operates on the main data path (I and Q) and performs three signal level adjusting functions:

1. Maximizing dynamic range
2. Compensating for SNR variations
3. Maintaining an optimal level into the Soft Decision Slicer.

The AGC Loop Block Diagram, shown in Figure 7, consists of an Error Detector, a Loop Filter, and Signal Gain Adjusters (multipliers). The AGC Error Detector generates an error signal by subtracting the programmable AGC threshold from the magnitude output of the Cartesian to Polar Converter. This difference signal is scaled (gain adjusted via multiplier and shifter), then filtered (integrated) by the AGC Loop Filter to generate the gain correction to the I and Q signals at the multipliers. If a fixed gain is desired, set the upper and lower limits equal.

The AGC responds to the magnitude of the sum of all the signals in the bandpass of the narrowest filter preceding the Cartesian to Polar Coordinate Converter. This filter may be the Integrate and Dump filter shown in Figure 7 on page 12, the RRC filter upstream in the HSP50210 data path, or some other filter outside the DCL chip. The magnitude signal usually contains several components:

1. The signal of interest component,
2. The noise component, and
3. Interfering signals component.

At high SNR's the signal of interest is significantly greater than the other components. At lower SNR's, components 2 or 3 may become greater than the signal of interest. Narrowing the filter bandwidth is the primary technique used to mitigate magnitude contributions of component 3. This will also improve the SNR by reducing the magnitude contributions of element 2. Consideration of the range of signal amplitudes expected into the HSP50210, in conjunction with a gain distribution analysis, will provide the

necessary insight to set the signal level into the Soft Decision Slicer to yield optimum performance.

Note: Failure to consider the variations due to noise or interfering signals, can result in signal limiting in the HSP50210 processing algorithms, which will degrade the system Bit Error Rate performance.

The AGC Loop is configured by the Power Detect Threshold and AGC Loop Parameters Control Registers (see Tables 16 and 17 on page 33). Seven programmable parameters must be set to configure the AGC Loop and its status outputs. Two parameters, the Power Threshold and the AGC Threshold are associated with the Error Detector and are represented in 8-bit fractional unsigned binary format: $2^0 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} 2^{-6} 2^{-7}$. While the format provides a range from 0 to 1.9961 for the thresholds, the Cartesian-to-Polar Converter scales the I and Q input magnitudes by 0.81. Thus, if a full scale (±1) complex (I and Q) input signal is presented to the converter, the output will be $\sqrt{(0.81)^2 + (0.81)^2} = 1.1455$. The AGC Threshold parameter value is the desired magnitude of the signal as it enters the Soft Decision Slicer. It is the parameter that will determine the error signal in the AGC loop. The Power Threshold, on the other hand, determines only the power threshold at which the $\overline{\text{THRESH}}$ signal is asserted. If the signal magnitude exceeds the threshold, then the $\overline{\text{THRESH}}$ is asserted. This may be used for signal detection, power detection or external AGC around the A/D converter. The AGC Threshold parameter is set in the AGC Loop Parameters Control Register, Bits 16 through 23 (see Table 17 on page 33). The Power Threshold parameter is set in the Power Detect Threshold Control Register, Bits 0 through 7 (see Table 16 on page 33). Note that these two threshold parameters are not required to be set to identical or even related values, since they perform independent functions.

The Enable AGC parameter sets the AGC Error Detector output to zero if asserted and to normal error detection output when not asserted. This control bit is set in the AGC Loop Parameter Control Register, Bit 31 (see Tables 17 on page 33). This bit is used to disable the AGC loop.

The remaining AGC parameters determine the AGC loop characteristics: gain tracking, tracking rate and tracking limits. The AGC Loop gain is set via two parameters: AGC Loop Gain Exponent and AGC Loop Gain Mantissa. In general, the higher the loop gain, the faster signal level acquisition and tracking, but this must be tempered by the specific signal characteristics of the application and the remaining programmable loop parameters. For the HSP50210, the AGC Loop Gain provides for a variable attenuation of the input to the loop filter. The AGC gain mantissa is a 4-bit value which provides error signal scaling from 0.000 to 0.9375, with a resolution of 0.0625. Table 2 on page 11 details the discrete set of decimal values possible for the AGC Loop Gain mantissa. The exponent provides a shift factor scaling from 2^{-7} to 2^{-14}. Table 3 on page 11 details the discrete set of decimal values possible for the AGC Loop Gain Exponent. When combined, the exponent and mantissa provide a loop gain defined as Equation 7:

$$\text{AGC Loop Gain: } G_{AGC} = [(M)(2^{-4})][(2^{-(7+E)})] \quad \text{(EQ. 7)}$$

where M is a binary number with a range from 0 to 15 and E is a 3-bit binary value from 0 to 7. M and E are the parameters set in the AGC Loop Parameters Control Register, Bits 24 through 30 (see Table 17 on page 33). The composite range of the AGC loop Gain is 0.0000 to [0.9375][2 to 7]. This will scale the AGC error signal to a range of 0.000 to (1.1455)(0.9375)(2 to 7) = 1.07297(2 to 7).

TABLE 2. AGC LOOP GAIN BINARY MANTISSA TO DECIMAL SCALED MANTISSA MAPPING

BINARY CODE (MMMM)	DECIMAL SCALED MANTISSA	BINARY CODE (MMMM)	DECIMAL SCALED MANTISSA
0000	0.0000	1000	0.5000
0001	0.0625	1001	0.5625
0010	0.1250	1010	0.6250
0011	0.1875	1011	0.6875
0100	0.2500	1100	0.7500
0101	0.3125	1101	0.8125
0110	0.3750	1110	0.8750
0111	0.4375	1111	0.9375

TABLE 3. AGC LOOP BINARY EXPONENT TO SCALED DECIMAL EXPONENT MAPPING

BINARY CODE (EEE)	DECIMAL/HEX EXPONENT	DECIMAL SCALED EXPONENT
000	0	2^{-7}
001	1	2^{-8}
010	2	2^{-9}
011	3	2^{-10}
100	4	2^{-11}
101	5	2^{-12}
110	6	2^{-13}
111	7	2^{-14}

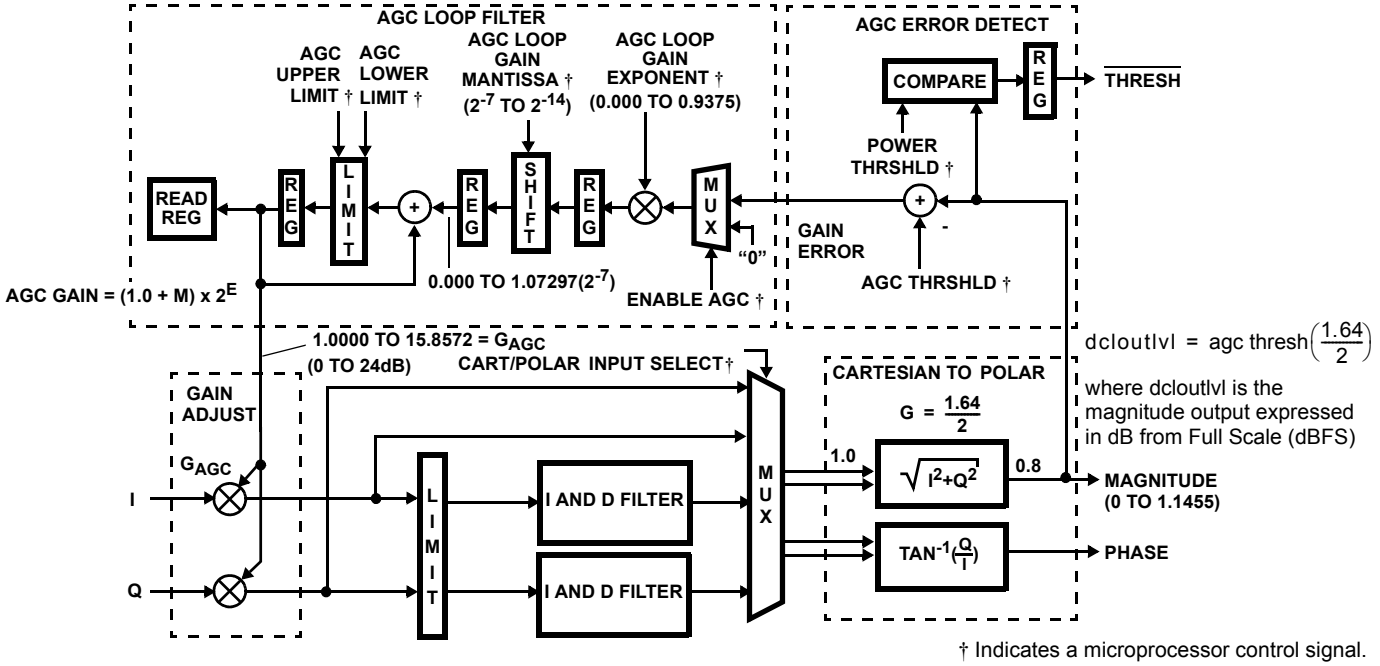


FIGURE 7. AGC LOOP BLOCK DIAGRAM

The AGC Loop Filter integrates the scaled error signal to provide a correction control term to the multipliers in the I and Q path. The loop filter accumulator has internal upper and lower limiters. The upper eight bits of the accumulator output map to an exponent and mantissa format that is used to set these upper and lower limits. The format, illustrated in Figure 8, is used for the AGC Upper Limit, AGC Lower Limit and the Correction Control Term (AGC output). This format should not be confused with the similar format used for the AGC Loop Gain. The input to the AGC Loop Filter is included in Figure 8 to show the relative weighting of the input to output of the loop filter. The loop filter input is represented as the eleven letter "G"s. Lower case "e" and "m" detail the format for the AGC Upper and Lower Limits. This change in type case should help keep the AGC Limits and AGC Gain formats from being confused. The AGC Upper and Lower Limits are set in the AGC Loop Parameters Control Register, Bits 0 through15, (see Table 17). This 6-bit unsigned mantissa format provides for an AGC output control range from 0.0000 to 0.9844, with a resolution of 0.015625. The 2-bit exponent format provides an AGC output control range from 1 to 8. The decimal values for each of the 64 binary mantissa values is detailed in Table 4, while Table 5 details the decimal value for the 4 exponent values.

The AGC Output is implemented in the multiplier according to Equations 8 and 9.

$$Out_{AGC-linear} = (1.0 + m_{AGC})(2^{e}) \quad \text{(EQ. 8)}$$

$$Out_{AGC-dB} = 20 \log [(1.0 + m_{AGC})(2^{e})] \quad \text{(EQ. 9)}$$

where m and e are the binary values for mantissa and exponent found in Tables 4 and 5.

Note: This format is identical to the format used to program the AGC Upper and Lower Limits, but in this usage it is not a programmed value. It is a representation of the digital AGC output number, which is presented to the Gain Adjuster (multipliers) to correct the gain of the I and Q data signals in the main data path.

These equations yield a composite (mantissa and exponent) AGC output range of 0.0000 to 1.9844(2^3) which is a logarithmic range from 0dB to 24dB. Figure 9 has graphed the results of Equations 8 and 9 for both the linear and logarithmic equations. Figure 9 also has a linear estimate of the logarithmic equation. This linear approximation will be used in calculating the AGC response time.

2^1	2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}
e	e	.m	m	m	m	m	m		G	G	G	G	G	G	G	G	G	G	G

FIGURE 8. AGC OUTPUT AND AGC LIMITS BIT WEIGHTING

TABLE 4. AGC GAIN MANTISSA TO DECIMAL MAPPING

BINARY CODE ($MMMMMM_{AGC}$)	DECIMAL VALUE OF AGC MANTISSA	BINARY CODE ($MMMMMM_{AGC}$)	DECIMAL VALUE OF AGC MANTISSA
000000	0.000000	100000	0.500000
000001	0.015625	100001	0.515625
000010	0.031250	100010	0.531250
000011	0.046875	100011	0.546875
000100	0.062500	100100	0.562500
000101	0.078125	100101	0.578125
000110	0.093750	100110	0.593750
000111	0.109375	100111	0.609375
001000	0.125000	101000	0.625000
001001	0.140625	101001	0.640625
001010	0.156250	101010	0.656250
001011	0.171875	101011	0.671875
001100	0.187500	101100	0.687500
001101	0.203125	101101	0.703125
001110	0.218750	101110	0.718750
001111	0.234375	101111	0.734375
010000	0.250000	110000	0.750000
010001	0.265625	110001	0.765625
010010	0.281250	110010	0.781250
010011	0.296875	110011	0.796875
010100	0.312500	110100	0.812500
010101	0.328125	110101	0.828125
010110	0.343750	110110	0.843750
010111	0.359375	110111	0.859375
011000	0.375000	111000	0.875000
011001	0.390625	111001	0.890625
011010	0.406250	111010	0.906250
011011	0.421875	111011	0.921875
011100	0.437500	111100	0.937500
011101	0.453125	111101	0.953125
011110	0.468750	111110	0.968750
011111	0.484375	111111	0.984375

TABLE 5. AGC GAIN EXPONENT TO DECIMAL MAPPING

BINARY CODE	DECIMAL/HEX EXPONENT	DECIMAL SCALED EXPONENT
00	0	2^0
01	1	2^1
10	2	2^2
11	3	2^3

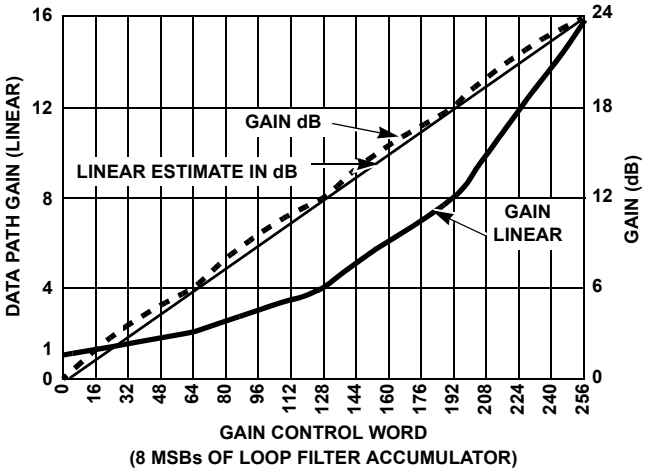


FIGURE 9. GAIN CONTROL TRANSFER FUNCTION

There are two techniques for setting a fixed gain for the AGC. The first is to set Control Word 2 Bit 31 = 1. This precludes any error update of present AGC gain value. The second is to set the upper and lower AGC limits to the desired gain using Figure 9. The upper and lower limits have the same value for this case.

The HSP50210 provides two mechanisms for monitoring signal strength. The first, which involved the THRESH signal, has already been described. The second mechanism is via the Microprocessor Interface. The 8 most significant bits of the AGC loop filter output can be read by a microprocessor. Refer to the “Microprocessor Interface” on page 27 for details of how to read this value. This AGC value has the format described in Figure 8.

AGC Bit Weighting and Loop Response

The AGC loop response is a function of the programmable gain, the bit weightings inherent in the connection of each element of the loop, the AGC Loop filter limits and the magnitude of the input gain error step. Table 6 on page 14 details the bit weighting between each element of the AGC Loop from the error detector through the weighting at the gain adjuster in the signal path. The AGC Loop Gain sets the growth rate of the sum in the loop filter accumulator. The Loop filter output growth rate determines how quickly the AGC loop traces the transfer function shown previously in Figure 9. To calculate the rate at which the AGC can adjust over a given period of time, a gain step is introduced to the gain error detector and the amount of change that is observed between clocks at the AGC Level Adjusters (multipliers) is the AGC response time in dB per symbol. This AGC loop will respond immediately with the greatest correction term, then asymptotically approach zero correction.

We begin calculation of the loop response with a full scale error detector input of ±1. This error input is scaled by the Cartesian to Polar converter, the error detector and the AGC

Loop Gain, accumulated in the loop filter, limited and output to the gain adjusters. The AGC loop tries to make the error correction as quickly as possible, but is limited by the AGC Loop Gain and potentially, the AGC limits. The maximum AGC response is the maximum gain adjustment made in any given clock cycle. This involves applying maximum Loop gain and setting the AGC limits as wide as possible. A calculation using only exponent terms of the various gains will be sufficient to yield a rough order of magnitude of the range of the AGC Loop response. The results are shaded in the last column of Table 6 on page 14 and provided in detail in Equations 10 and 11.

TABLE 6. AGC BIT WEIGHTING

AGC ACCUM BIT POSITION	GAIN ERROR INPUT	GAIN ERROR BIT WEIGHT	AGC LOOP FILTER GAIN (MANTISSA)	AGC LOOP FILTER GAIN MULTIPLIER (OUTPUT)	AGC LOOP FILTER GAIN BITS KEPT (rnd)	SHIFT = 0		SHIFT = 7	AGC OUTPUT AND AGC LIMITS BIT WEIGHT	AGC GAIN RESOLUTION (dB)
22								Shifter →	E 1	12
21								Shifter →	E 0	6
20						Multiplier →			M -1	3
19									M -2	1.5
18									M -3	0.75
17									M -4	0.375
16									M -5	0.1875
15						Multiplier →		1	M -6	0.09375
14								0•	• 0-7	0.04688
13								1	G -8	0.02344
12								2	G -9	0.01172
11								3	G -10	0.00586
10								4	G -11	0.00293
9								5	G -12	0.00146
8	8(S)	= 1(S)	0.	12(S)	12(S)	= 1	1	6	G -13	0.000732
7	7	= 0•	x	11	11	= 0•	0•		G -14	0.000366
6	6	= 1	x	10	10	= 1	1		G -15	0.000183
5	5	= 2	x	9	9	= 2	2		G -16	0.0000916
4	4	= 3	x	8	8	= 3	3		G -17	0.0000458
3	3	= 4		7	7	= 4	4		G -18	0.0000229
2	2	= 5		6	6	= 5	5		-19	0.0000114
1	1	= 6		5	5	= 6	6		-20	0.00000572
0	0	= 7		4					-21	0.00000286
				3						
				2						
				1						
				0						

$AGC\ Response_{MAX}$ = Input (Cartesian to Polar Converter Gain)(Error Detector Gain)(AGC Loop Gain)(AGC Output Weighting)

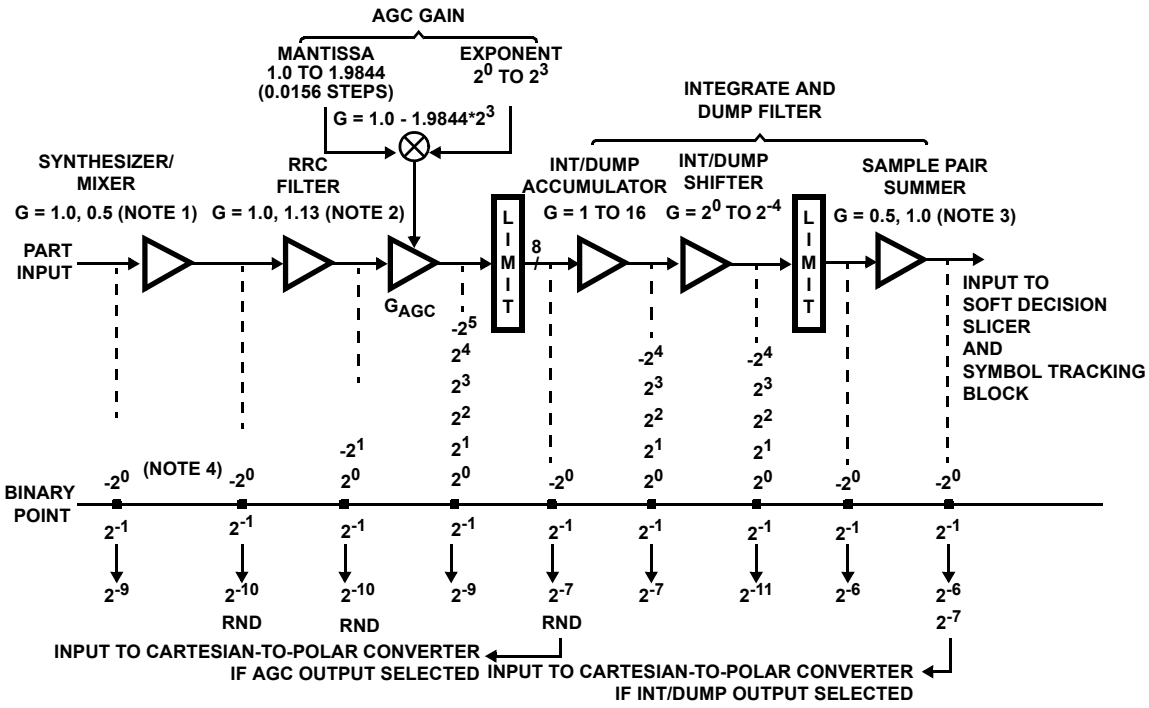
$$AGC\,Response_{MAX} = \pm 1(0.5)(0.5)(2^{-7})(24) = \pm 1(2^{-9})(24) = 0.04688dB/symbol\ time \quad \text{(EQ. 10)}$$

where (0.5) is the MSB of the 0.81 scaling in the Cartesian-to-Polar Coordinate Converter, (0.5) is the MSB of the mantissa of the Loop Gain, (2^{-7}) is the maximum shift gain, and 24 is the maximum loop filter gain.

A similar procedure is used to calculate the minimum AGC response rate.

$$AGC\,Response_{MIN} = \pm 1(0.5)(0.5)(2^{-14})(24) = \pm 1(2^{-16})(24) = 0.000366dB/symbol\ time \quad \text{(EQ. 11)}$$

Thus, the expected range for the AGC rate is approximately 0.0004 to 0.0469dB/symbol time.



NOTES:

1. If the Mixer is enabled, the result of the complex multiply is scaled by two (G = 0.5). If the mixer is bypassed, the data passes unmodified (G = 1.0).
2. If the Root Raised Cosine Filter is enabled, a gain of G = 1.13 is introduced. If the RRC filters bypassed, the gain is unity.
3. If the integrate and Dump Filter is bypassed the Sample Pair summer has a gain of G = 1.0 and the 2^{-7}-bit position is set to 1. If the integrate and dump is enabled, the sample pair sum is scaled by one half (G = 0.5).
4. The negative sign on the MSBs indicates use of 2's complement data format.

FIGURE 10. GAIN DISTRIBUTION AND INTERMEDIATE BIT WEIGHTINGS

Gain Distribution

The gain distribution in the DCL is shown in Figure 10. These gains consist of a combination of fixed, programmable, and adaptive gains. The fixed gains are introduced by processing elements such as the Mixer and Square Root of Root Raised Cosine Filter. The adaptive gains are set to compensate for variations in input signal strength.

The main signal path, with processing block gains and path bit weightings, is shown in Figure 10. The quadrature inputs to the HSP50210 are 10-bit fractional two's complement numbers with relative bit weightings, as shown in Figure 10. The first element in the processing chain is the Mixer, which scales the quadrature outputs of the complex multiplier by 1/2 providing a gain of G = 0.5. If the Mixer is bypassed, the signal is passed unmodified with a gain of 1.0. Following the mixer, the quadrature signal is passed to the fixed coefficient RRC filtering block, which has a gain of 1.13 if enabled and 1.0 if bypassed. Next, the AGC supplies gain to maintain an optimal signal level at the input to the Soft Decision Slicer, Cartesian-to-Polar Converter, and the Symbol Tracking Loop. The gain supplied by the AGC ranges from 1.0 to 1.9844*2^3.

Following the AGC, the signal path is limited to 8 bits and passed through the Integrate and Dump Filter en route to the Soft Decision Slicer and Symbol Tracking Block. The I and D Filter uses an accumulator together with a sample pair summer to achieve the desired decimation rate. The I and D shifter is provided to compensate for the gain introduced by the I and D Accumulator. The accumulator introduces gain equal to the decimation factor R, and the shifter gain can be set to 1/R. For example, if the I and D Filter decimation of 16 is chosen, the I and D Accumulator will accumulate 8 samples before dumping, which produces a gain of 8. Thus, for unity gain, the I and D Shifter would be set for a gain of 2^{-3}. The Sample Pair Summer is unity gain since its output is scaled by one-half.

Symbol Tracking

The symbol tracking loop adjusts the baseband sampling frequency to force sampling of the baseband waveform at optimal points for data decisions. The key elements of this loop are the Sampling Error Detector and Symbol Tracking Loop Filter shown in Figure 11. The output of these two blocks is a frequency correction term which is used to adjust the baseband sample frequency external to the HSP50210. In typical applications, the frequency correction term is fed back to the HSP50110 to adjust baseband sampling via the Resampling NCO (see HSP50110 Datasheet).

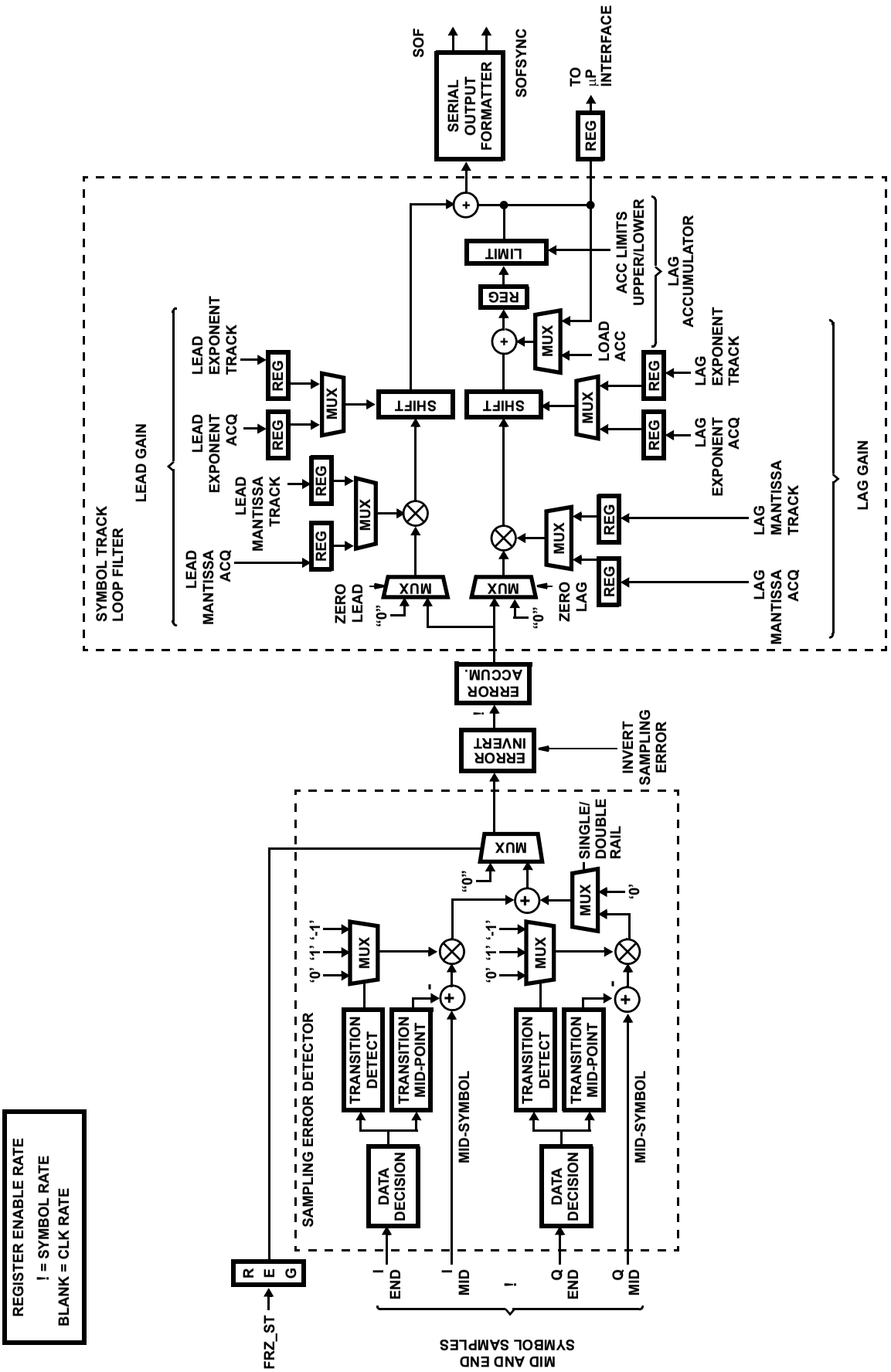


FIGURE 11. SYMBOL TRACKING

Sampling Error Detector

The Sampling Error Detector is a decision based error detector which determines sampling errors on both the I and Q processing paths. The detector assumes that it is fed with samples of the baseband waveform taken in the middle of the symbol period (mid-symbol sample) and between symbols (end-symbol sample) as shown in Figure 12. The sampling error is a measure of how far the mid-symbol sample is from the symbol transition mid-point. The transition mid-point is half way between two symbol decisions. The detector makes symbol decisions by comparing the end-symbol samples against a selectable threshold set (see Modulation Order Select bits 9 through 10 in Table 29 on page 37). The error term is generated by subtracting the mid-symbol sample from the transition mid-point. The sign of the error term is negated for negatively sloped symbol transitions. If no symbol transitions are detected the error detector output is zeroed. Errors on both the I and Q processing paths are summed and divided by two if Double Rail error detection is selected (see Symbol Tracking Configuration Control Register, Bit 8: Table 29 on page 37).

The sampling Error Detector provides an error accumulator to compensate for the processing rate of the loop filter. The error detector generates outputs at the symbol rate, but the loop filter can only accept inputs every eight f_{CLK} clocks. Thus, if the symbol rate is faster than 1/8 CLK, the error accumulator should be used to accumulate the error until the loop filter is ready for a new input. If the error accumulator is not used when the symbol rate exceeds 1/8 CLK, some error outputs will be missed. For example, if f_{CLK} = 40MHz, then error accumulation is required for symbol rates greater than 5 MSPS (f_{CLK}/8). Note: The loop filter lead gain term must be scaled accordingly if the accumulator is used.

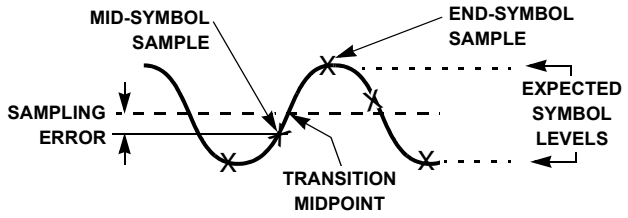


FIGURE 12. TRACKING ERROR ASSOCIATED WITH BASEBAND SAMPLING ON EITHER I OR Q RAIL (BPSK/QPSK)

Symbol Tracking Loop Filter

The Symbol Tracking Loop Filter is a second order lead/lag filter. The sampling error is weighted by the lag gain and accumulated to give the integral response (see Figure 11). The Lag Accumulator output is summed with the sampling error weighted by the Lead Gain. The result is a frequency term which is output serially, via the SOF output, to the NCO/VCO controlling the baseband sample rate (see “Serial Output Interfaces” on page 23). In basic configurations, the SOF output of the HSP50210 is connected to the SOF input of the HSP50110.

Two sets of registers are provided to store the loop gain parameters associated with acquisition and tracking. The appropriate loop gain parameters are selected manually via the Microprocessor Interface or automatically via the Carrier Lock Detector. The loop filter’s lead and lag gain terms are represented as a mantissa and exponent. The mantissa is a 4-bit value which weights the loop filter input from 1.0 to 1.9375. The exponent defines a shift factor that provides additional weighting from 2^{-1} to 2^{-32}. Together the loop gain mantissa and exponent provide a gain range between 2^{-32} and ~1.0 as given by Equation 10.

$$\text{Lead/Lag Gain} = (1.0+M*2^{-4})*2^{-(32-E)} \quad \text{(EQ. 10)}$$

where M = a 4-bit binary number from 0 to 15, and E is a 5-bit binary value ranging from 0 to 31. For example, if M = 0101 and E = 00110, the Gain = $1.3125*2^{-26}$. They are stored in the Control Registers described in Tables 32 and 33 beginning on page 38.

A limiter is provided on the lag accumulator output to keep the baseband sample rate within a user defined range (see Tables 30 and 31 on page 38). If the lag accumulator exceeds either the upper or lower limit, the accumulator is loaded with the limit. For additional loop filter control, the loop filter output can be frozen by asserting the FZ_ST pin which null the sampling error term into the loop filter. The lag accumulator can be initialized to a particular value and can be read via the microprocessor interface as described in “Reading from the Microprocessor Interface” on page 27, and Table 34 on page 39. The symbol tracking loop filter bit weighting is identical to the carrier tracking loop bit weighting, shown in Figures 9 and 10.

Soft Decision Slicer

The Soft Decision Slicer encodes the I/Q end-symbol samples into 3-bit soft decisions. The input to the slicer is assumed to be a bipolar (2ary) baseband signal representing encoded values of either ‘1’ or ‘0’. The most significant bit of the 3-bit soft decision represents a hard decision with respect to the mid-point between the expected symbol values. The 2 LSBs represent a level of confidence in the decision. They are determined by comparing the magnitude of the slicer input to multiples (1x, 2x, and 3x) of a programmable soft decision threshold (see Figure 13).

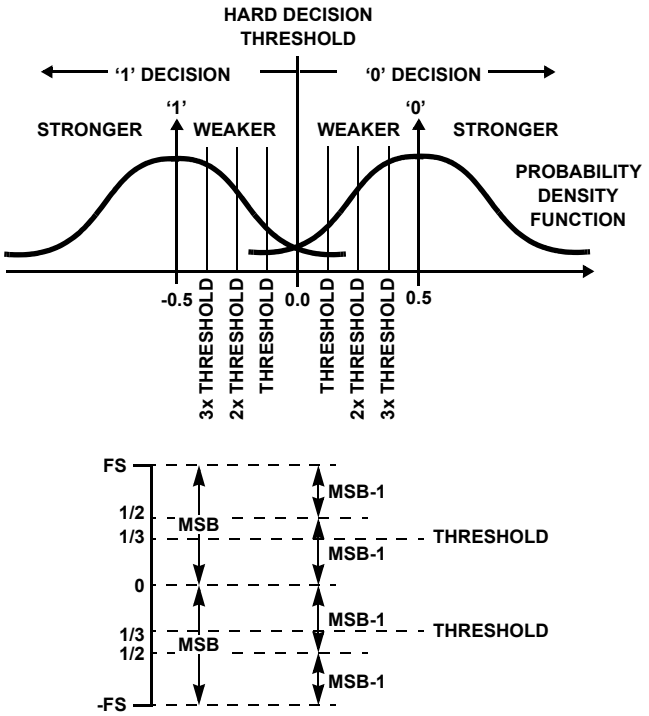


FIGURE 13. OVERLAY OF THE HARD/SOFT DECISION THRESHOLDS ON THE SYMBOL PROBABILITY DENSITY FUNCTIONS (PDFs) FOR BPSK/QPSK SIGNALS)

The soft decision threshold represents a range of magnitude values from 0.0 to ~0.5. Note: Since the input to the slicer has a range of 0.0 to ~1.0, the threshold setting should be set to less than 1.0/3 = 0.33. This avoids saturation. The slicer decisions are output in either a two's complement or sign/magnitude format (see Soft Decision Slicer Configuration Control Register, Bit 7: Table 41 on page 42). The slicer input to output mapping for a range of input magnitudes is given in Table 7. For example, a negative input to the slicer whose magnitude is greater than twice the programmable threshold but less than 3x the threshold would produce a sign/magnitude output of 110 (BINARY). The I and Q inputs to the slicer are encoded into 3-bit soft decisions ISOFT(2-0) and QSOFT(3-0). These signals are routed to the OUTA(9-4) outputs by the Output Configuration Control Register Selector bits 0-3 (see Table 43 on page 44).

TABLE 7. SLICER INPUT TO OUTPUT MAPPING

SIGNAL INPUT POLARITY	SLICER INPUT MAGNITUDE RELATIVE TO			SIGN/MAGNITUDE OUTPUT	TWO'S COMPLEMENT OUTPUT
	1x THRESHOLD	2x THRESHOLD	3x THRESHOLD		
+	>	>	>	011	011
+	>	>	≤	010	010
+	>	≤	<	001	001
+	≤	<	<	000	000
-	≤	<	<	100	111
-	>	≤	<	101	110
-	>	>	≤	110	101
-	>	>	>	111	100

Carrier Phase Error Detector

The Carrier Phase Error is computed by removing the phase modulation from the phase output of the Cartesian-to-Polar Converter. To remove the modulation, the phase term is rotated and multiplied (modulo 2π) to fold the Phase Error into an arc centered about 0° but encompasses the whole plane, as shown in Figure 14. The phase rotation is performed by adding a 4-bit two's complement phase offset (resolution 22.5°) to the 4 MSBs of the 8-bit phase term. The multiplication is performed by left shifting the result from 0 to 3 positions with the MSBs discarded and zeros inserted into the LSBs. For example, Carrier Phase Error produces I/Q constellation points which are rotated from the expected constellation points as shown in Figure 14. By adding an offset of 45° (0010 0000 binary) and multiplying by 4 (left shift by two positions) the phase modulation is removed, and the error is folded into a 90° arc centered at 0°. The left axis represents a decision boundary of ±45°C, implying the vertical axis is ±22.5° as shown in Figure 15. The phase offset and shift factors required for different PSK orders is given in Table 9 on page 21. Configuration of the Carrier Phase Error Detector is done via the Carrier Phase Error Detector Control Register, bits 0 to 5, (see Table 18 on page 33). The Phase Error term may be selected for output via the Output Selector Configuration Control Register, bits 0 to 3 (see Table 43 on page 44).

In applications where Phase Error terms are generated faster than the processing rate of the Carrier Loop Filter, an error accumulator is provided to accumulate errors until the loop filter is ready for a new input. Phase Error terms are generated at the rate I/Q samples are input to the Cartesian to Polar Converter. However, the Carrier Loop Filter cannot accept new input faster than CLK/6 since six CLK(f_{CLK}) clock edges are required to complete its processing cycle. If the error accumulator is not used and the I/Q sample rate exceeds CLK/6, error terms will be missed.

Note: The carrier Phase Error terms input to the loop filter are only generated from the end-symbol samples when the output of the I and D filter is selected for input to the Cartesian-to-Polar converter.

Note: The loop filter lead gain term must be scaled accordingly if the accumulator is used.

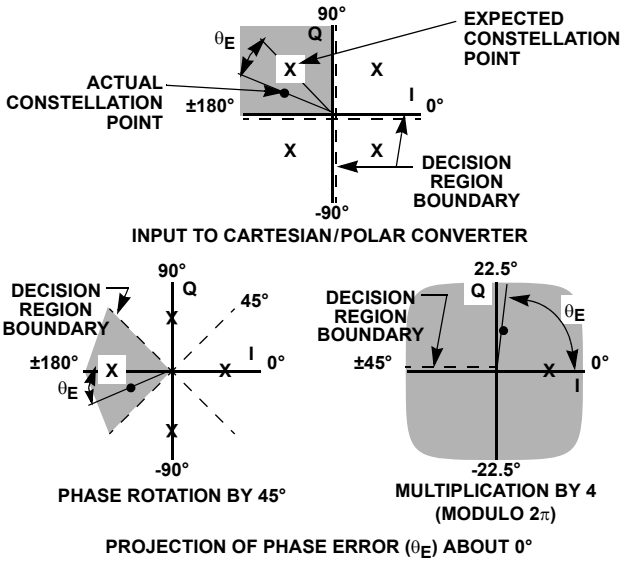


FIGURE 14. PHASE ERROR DETECTOR OPERATION (QPSK)

TABLE 8. BASIC PHASE ERROR DETECTOR SETTINGS

MODULATION TYPE	PHASE OFFSET	SHIFT FACTOR	PHASE ERROR RANGE
CW	0° (00 HEX)	0 (no shift)	±180
BPSK	0° (00 HEX)	1 (left shift 1)	±90
QPSK	45° (20 HEX)	2 (left shift 2)	±45
8-PSK	22.5° (10 HEX)	3 (left shift 3)	±22

Carrier Loop Filter

The Carrier Loop Filter is second order lead/lag filter as shown in Figure 14. The loop filter is similar to the Symbol Tracking Loop Filter except for the additional terms from the AFC Loop Filter and the Frequency Sweep Block. The output of the Lag Accumulator is summed with the weighted Phase Error term on the lead path to produce a frequency control term. The Carrier Loop Filter is configured for operation by the Control Registers described in Tables 21 through 28 beginning on page 34.

The Carrier Tracking Loop is closed by using the loop filter output to control the NCO or VCO used to down convert the channel of interest. In basic configurations, the frequency correction term controls the Synthesizer NCO in the HSP50110 Digital Quadrature Tuner via the COF and COFSYNC pins of the HSP50210's serial interface (see "Serial Output Interfaces" on page 23). In applications where the carrier tracking is performed using the NCO on board the HSP50210, the loop filter output is fed to the on-board NCO as a frequency control.

The gain for the lead and lag paths of the Carrier Loop Filter are set through a programmable mantissa and exponent. The mantissa is a 4-bit value which weights the loop filter input from 1.0 to 1.9375. The exponent defines a shift factor that provides additional weighting from 2^{-1} to 2^{-32}. Together the loop gain mantissa and exponent provide a gain range between 2^{-32} and ~1.0 as given by Equation 11.

$$\text{Lead/Lag Gain} = (1.0+M*2^{-4})*2^{-(32-E)} \quad \text{(EQ. 11)}$$

where M = a 4-bit binary number from 0 to 15, and E is a 5-bit binary value ranging from 0 to 31. For example, if M = 0101 and E = 00110, the Gain = $1.3125*2^{-26}$. The loop gain mantissa and exponent are set in the Carrier Loop Gain Control Registers (see Tables 25 through 26 on page 36).

The Phase Error input to the Carrier Loop Filter is an 8-bit fractional two's complement number between ~1.0 to -1.0 (Format $-2^0.\ 2^{-1}2^{-2}2^{-3}2^{-4}2^{-5}2^{-6}2^{-7}$). Some LSBs are zero for BPSK, QPSK and 8-PSK. If minimum loop gain is used, the Phase Error is shifted in significance by 2^{-32}. With maximum loop gain, the Phase Error is passed almost unattenuated. The output of the Carrier Loop filter is a 40-bit fractional two's complement number between ~1.0 and -1.0 (Format $-2^0.\ 2^{-1}2^{-2}2^{-3}\ldots..\ 2^{-39}2^{-40}$). In typical applications, the 32 MSBs of the loop filter output represent the frequency control word needed to adjust the down converting NCO for phase lock. Tables 9 and 10 beginning on page 21 illustrate the bit weighting of the Carrier Loop Filter into the NCO for both tracking and acquisition sweep modes.

A limiter is provided on the Carrier lag accumulator output to keep frequency tracking within a user defined range (see Tables 23 and 24 on page 35). If the lag accumulator exceeds either the upper or lower limit the accumulator is loaded with the limit. For additional loop filter control, the Carrier Loop Filter output can be frozen by asserting the FZ_CT pin which nulls the Phase Error term into the loop filter. Also, the lag accumulator can be initialized to a particular value via the Microprocessor Interface as described in Table 28 on page 37 and can be read via the microprocessor interface as described in "Reading from the Microprocessor Interface" on page 27.

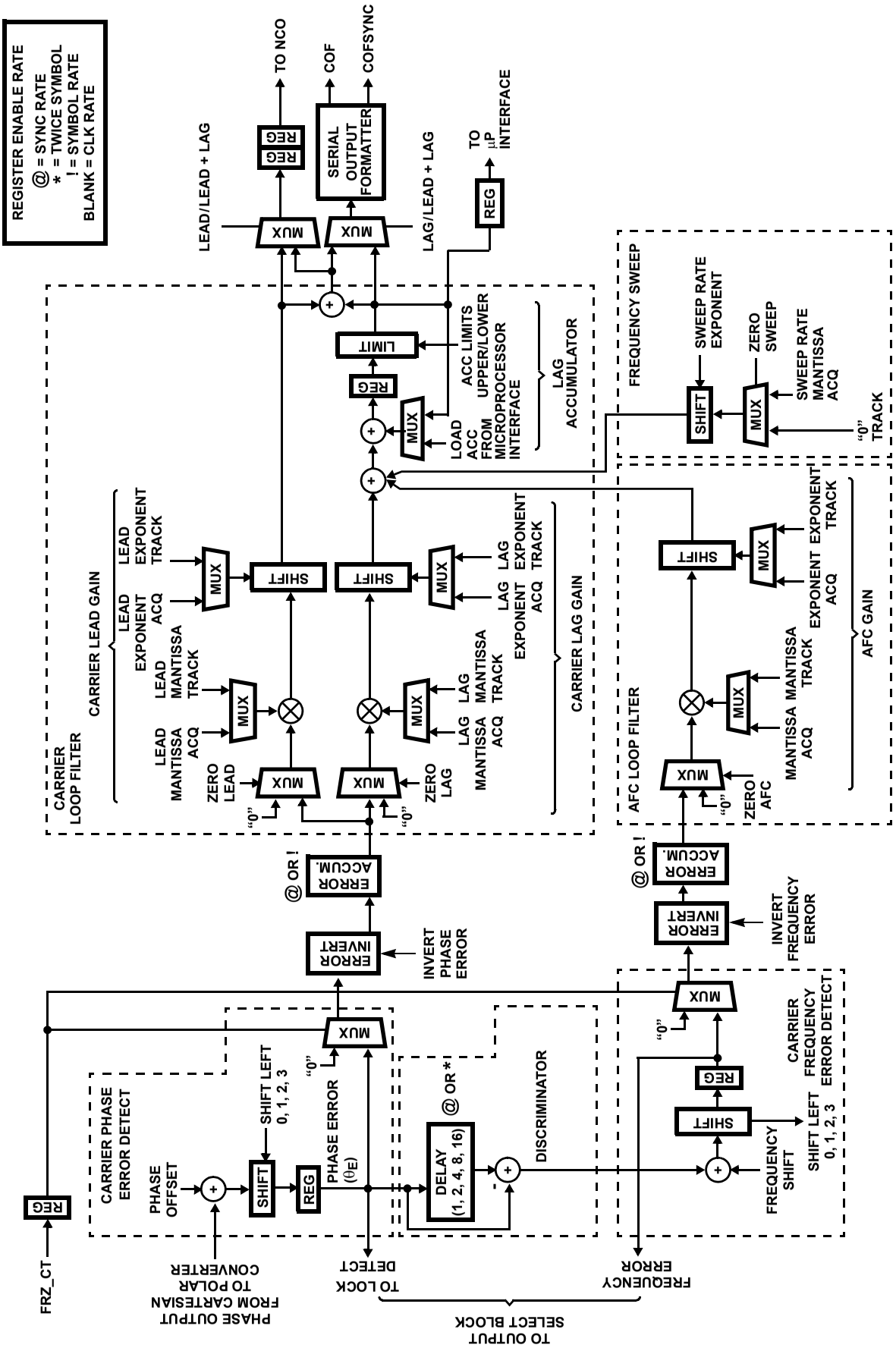


FIGURE 15. CARRIER ACQUISITION/TRACKING LOOP BLOCK DIAGRAM

TABLE 9. BIT WEIGHTING IN THE CARRIER LOOP FILTER TO THE NCO - TRACKING

BIT WEIGHT	ϕe (AND ACCOM.)	MANTISSA GAIN	MULT OUT	BITS KEPT (RND)		SHIFT = 0	SHIFT ≅ 32	SHIFT COUNTS	NCO BIT WEIGHT	OUTPUT FREQUENCY RESOLUTION
40									0	f_{CLK}
39	Obtained with a shift of 31 and a Gain of 01.1111 (~2) →						(8)	- shift31	1	$f_{CLK}/2$
38							7.	- shift31	2	$f_{CLK}/4$
37							6	- shift30	3	$f_{CLK}/8$
36							5	- shift29	4	$f_{CLK}/16$
35							4	- shift28	5	$f_{CLK}/32$
34							3	- shift27	6	$f_{CLK}/64$
33							2	- shift26	7	$f_{CLK}/128$
32							1	- shift25	8	$f_{CLK}/256$
31							0	- shift24	9	$f_{CLK}/512$
30								- shift23	10	$f_{CLK}/1024$
29								- shift22	11	$f_{CLK}/2048$
28								- shift21	12	$f_{CLK}/4096$
27								- shift20	13	$f_{CLK}/8192$
26								- shift19	14	$f_{CLK}/2^{14}$
25								- shift18	15	$f_{CLK}/2^{15}$
24								- shift17	16	$f_{CLK}/2^{16}$
23								- shift16	17	$f_{CLK}/2^{17}$
22								- shift15	18	$f_{CLK}/2^{18}$
21								- shift14	19	$f_{CLK}/2^{19}$
20								- shift13	20	$f_{CLK}/2^{10}$
19								- shift12	21	$f_{CLK}/2^{21}$
18								- shift11	22	$f_{CLK}/2^{22}$
17								- shift10	23	$f_{CLK}/2^{23}$
16								- shift9	24	$f_{CLK}/2^{24}$
15								- shift8	25	$f_{CLK}/2^{25}$
14								- shift7	26	$f_{CLK}/2^{26}$
13			17					- shift6	27	$f_{CLK}/2^{27}$
12	(12)		16	17	= (12)	(12)		- shift5	28	$f_{CLK}/2^{28}$
11	(11)		15	16	= (11)	(11)		- shift4	29	$f_{CLK}/2^{29}$
10	(10)		14	15	= (10)	(10)		- shift3	30	$f_{CLK}/2^{30}$
9	(9)		13	14	= (9)	(9)		- shift2	31	$f_{CLK}/2^{31}$
8	(8)	0	12	13	= (8)	(8)		- shift1	32	$f_{CLK}/2^{32}$
7	7.	1.	11.	12.	= 7.	7.		- shift0	33	$f_{CLK}/2^{34}$
6	6	x	10	11	= 6	6			34	$f_{CLK}/2^{34}$
5	5	x	9	10	= 5	5			35	$f_{CLK}/2^{35}$
4	4	x	8	9	= 4	4			36	$f_{CLK}/2^{36}$
3	3	x	7	8	= 3	3			37	$f_{CLK}/2^{37}$
2	2		6	7	= 2	2			38	$f_{CLK}/2^{38}$
1	1		5	6	= 1	1			39	$f_{CLK}/2^{39}$
0	0		4	5	= 0	0			40	$f_{CLK}/2^{40}$
			3	(RND)						
			2							
			1							
			0							

TABLE 10. BIT WEIGHTING IN THE CARRIER LOOP FILTER TO THE NCO - SWEEP

BIT WEIGHT	ϕe	SWEEP MANTISSA GAIN	SHIFT = 0	SHIFT = 32	SHIFT COUNTS	NCO BIT WEIGHT	OUTPUT FREQUENCY RESOLUTION
40						0	f_{CLK}
39	Shift 27 and Gain = 01.1111 →			(8)	- shift28	1	$f_{CLK}/2$
38				7.	- shift27	2	$f_{CLK}/4$
37				6	- shift26	3	$f_{CLK}/8$
36				5	- shift25	4	$f_{CLK}/16$
35				4	- shift24	5	$f_{CLK}/32$
34				3	- shift23	6	$f_{CLK}/64$
33				2	- shift22	7	$f_{CLK}/128$
32				1	- shift21	8	$f_{CLK}/256$
31				0	- shift20	9	$f_{CLK}/512$
30					- shift19	10	$f_{CLK}/1024$
29					- shift18	11	$f_{CLK}/2048$
28					- shift17	12	$f_{CLK}/4096$
27					- shift16	13	$f_{CLK}/8192$
26					- shift15	14	$f_{CLK}/2^{14}$
25					- shift14	15	$f_{CLK}/2^{15}$
24					- shift13	16	$f_{CLK}/2^{16}$
23					- shift12	17	$f_{CLK}/2^{17}$
22					- shift11	18	$f_{CLK}/2^{18}$
21					- shift10	19	$f_{CLK}/2^{19}$
20					- shift9	20	$f_{CLK}/2^{10}$
19					- shift8	21	$f_{CLK}/2^{21}$
18					- shift7	22	$f_{CLK}/2^{22}$
17					- shift6	23	$f_{CLK}/2^{23}$
16					- shift5	24	$f_{CLK}/2^{24}$
15					- shift4	25	$f_{CLK}/2^{25}$
14					- shift3	26	$f_{CLK}/2^{26}$
13					- shift2	27	$f_{CLK}/2^{27}$
12	(12)	0	5		- shift1	28	$f_{CLK}/2^{28}$
11	(11)	1.	4.		- shift0	29	$f_{CLK}/2^{29}$
10	(10)	x	3			30	$f_{CLK}/2^{30}$
9	(9)	x	2			31	$f_{CLK}/2^{31}$
8	(8)	x	1			32	$f_{CLK}/2^{32}$
7	7.	x	0			33	$f_{CLK}/2^{34}$
6	6	z				34	$f_{CLK}/2^{34}$
5	5	z				35	$f_{CLK}/2^{35}$
4	4	z				36	$f_{CLK}/2^{36}$
3	3	z				37	$f_{CLK}/2^{37}$
2	2	z				38	$f_{CLK}/2^{38}$
1	1	z				39	$f_{CLK}/2^{39}$
0	0	z				40	$f_{CLK}/2^{40}$

NOTE:

5. $SW_{min} = 2^{-29}$ at 1% FLB, $4M_{clk}$, 0.075Hz/Baud = 12Kbps.

Frequency Sweep Block

The Frequency Sweep Block is used during carrier acquisition to sweep the range of carrier uncertainty. The Sweep Block is loaded with a programmable value which is input to the lag path of the Carrier Tracking Loop Filter when frequency sweep is enabled. The sweep value is accumulated by the loop filter's lag accumulator which causes a frequency sweep between the accumulator's upper and lower limits. When one of the limits is reached, the sweep value is inverted to sweep the frequency back toward the other limit. The Frequency Sweep Block is controlled by the Lock Detector and is only enabled during carrier acquisition (see "Lock Detector Control" on page 24).

A stepped acquisition mode is provided for microprocessor controlled acquisition. In the stepped acquisition mode, the lag accumulator is incremented or decremented by the programmed sweep value each time the lock detector is restarted during acquisition. This technique prevents the loop from sweeping past the lock point before the microprocessor can respond. Typically in stepped acquisition mode, the step value is set to a percentage of the loop bandwidth. A dwell counter is also provided for stepped acquisition. This counter holds off the lock detector integration from 1 to 129 symbols to allow the loop to settle before starting the integration.

The sweep value is set via a programmable mantissa and exponent. The format is 01.MMMM * $2^{-(28 - EEEEE)}$ where MMMM is the 4-bit mantissa and EEEEE is the 5-bit exponent and the weighting is relative to the MSB of the NCO control word. In swept acquisition mode, the sweep value is the amount that the carrier lag accumulator is incremented or decremented each time a new filter output is calculated (sweep rate/N). In stepped acquisition mode, it is the amount the lag accumulator is incremented or decremented each time that the lock detector is restarted. (See Frequency Sweep/AFC Control Loop Control Register, Table 27.)

Carrier Frequency Detector

The Frequency Detector generates a frequency term for use in Automatic Frequency Control (AFC) configurations. The Frequency Detector (discriminator) subtracts a previous Phase Error sample from the current one (d/dt) to produce a term proportional to the carrier frequency. The discriminator gain is adjusted by programming a variable delay (1-16) between the samples subtracted (see Frequency Detector Control Register; Table 19).

Note: The input to the discriminator corresponds to phase terms taken from baseband samples at either the SYNC rate or twice symbol rate depending on the input source chosen for the Cartesian-to-Polar converter.

Carrier Frequency Error Detector

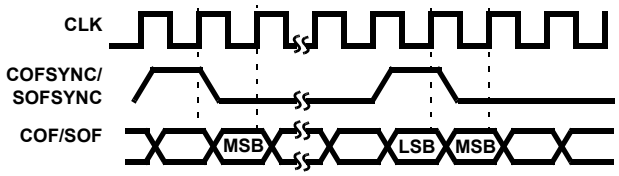
The Frequency Error Detector is used to generate a frequency error term for FSK modulated waveforms. The error is computed by adding an offset and shifting the frequency detector output in a manner similar to that used by the Phase Error Detector. For PSK demodulation, this block is bypassed by setting the offset and shift terms to zero (see Frequency Error Detector Control Register; Table 20 on page 34). The frequency error term may be selected for output via the Output Select Block. (See Serial Output Configuration Control Register, Table 42 on page 42).

Automatic Frequency Control (AFC) Loop Filter

The AFC Loop Filter supplies a frequency correction term to the lag path of the Carrier Loop filter. The frequency correction term is generated by weighting the output of the Frequency Error Detector by a user programmable weight (see Sweep/AFC Control Register; Table 27). Note: If AFC is not desired, the frequency error term to the loop filter is nulled via the Carrier Tracking Configuration Control Register #2 (see Table 22 on page 35).

Serial Output Interfaces

Frequency control data for Carrier and Symbol Tracking is output from the DCL through two separate serial interfaces. The Carrier Offset frequency control is output via the COF and COFSYNC pins. The Symbol Tracking Offset frequency control is output via the SOF and SOFSYNC pins. A SLOCLK is provided to allow for reduced serial rate data exchanges. The timing relationship of these signals is shown in Figure 16.



Note: Data must be loaded MSB first.

FIGURE 16. SERIAL OUTPUT TIMING FOR COF AND SOF OUTPUTS

Each serial word has a programmable word width of either 8, 12, 16, 20, 24, 28, 32, or 40 bits (see Table 42, CW27, bits 4 through 6 for COF and bits 0 through 2 for SOF). The polarity of the sync signals is programmable and is set in CW27 Bit 12 for SOF and Bit 11 for COF. The polarity of the serial clock to the serial data is programmed via CW27 Bit 10. If reduced rate frequency updates is required, the SLOCLK rate is selected via CW27 Bit 7 and the rate is set via CW27 bits 8 through 9, to be either CLK/2, CLK/4, CLK/8 or CLK/16. Note that if the DCL is used with the HSP50110 DQT, then the SLOCLK cannot be used, i.e., the serial clock must be set to be CLK.

Lock Detector

The Lock Detector consists of the Dwell Counter, Integration Counter, Phase Error Accumulator, False Lock/Frequency Accumulator, Gain Error Accumulator and the Lock Detect

State Machine (see Figure 16). The function of the Lock Detector is to monitor the baseband symbols and to decide whether the Carrier Tracking Loop is locked to the input signal. Note: The Symbol Tracking Loop locks independently; under most circumstances, it will lock before the Carrier Tracking Loop locks up. Based on the in-lock/out-of-lock decision, either the Acquisition or Tracking parameters are selected in the Carrier Tracking Loop, the Symbol Tracking Loop and in the Lock Detector itself. The Lock Detector can be configured either to make the “lock” decision automatically using the State Machine Control Mode, or to collect the necessary data so that an external microprocessor can control the acquisition/tracking process via the Microprocessor Control Mode (see Figure 22).

In State Machine Control Mode, the Lock Detector State Machine monitors the outputs of the Phase Error Accumulator and the False Lock Accumulator to determine the Lock Detector state. Accumulation effectively averages the Phase Error and false lock count, reducing their variance. Lock is detected by accumulating the magnitude of the Phase Error over a predetermined interval up to 1025 symbols (the Integration Time). When the Carrier Loop is locked, the Integration Period will end before an overflow occurs in the Phase Error Accumulator. At the beginning of a lock detection cycle, the Phase Error Accumulator and the Integration Counter are loaded with their respective pre-load values. With each end bit sample, the Phase Error Accumulator adds the magnitude of the current Phase Error to its accumulated sum, while the Integration Counter decrements one count. The Lock Detector State Machine monitors the overflow bit of the Phase Error Accumulator and the output of the Integration Counter. If the Phase Error Accumulator overflows before the Integration Counter reaches zero, then the accumulated Phase Error is too large for the Carrier Tracking Loop to be in lock and the Lock Detector State Machine goes into the Search state (see Lock Detector State Machine in Figure 17). In the search state, the loop parameters are reloaded with “Acquisition” rather than “Tracking” values. When the Phase Accumulator overflows or when the Integration Counter reaches zero, the Integration Counter and the accumulators are re-initialized and the process begins again. The Integration Counter Pre-load corresponds to the number of symbols over which to integrate. The Phase Error Preload corresponds to the distance the Phase Error Accumulator starts away from overflow. This distance divided by the Integration Period equals the average Phase Error. The pre-load value is calculated using Equation 12:

$$\text{Preload} = \text{Full Scale} - \left(\frac{\text{Lock Threshold}}{\text{Full Scale Phase}} \times 128 \times \text{Integration Count}\right) \quad \text{(EQ. 12)}$$

where

Full scale = 2^{18}-1

Full scale phase = 180° for CW, 90° for BPSK, 45° for QPSK, etc;

Lock Threshold <45° for BPSK, <22.5° for QPSK, etc. (typical after shift); and Integration Count = Integration Period measured in symbol times.

The False Lock Detector is used to indicate false lock on square wave data in a high SNR environment. A false lock condition is detected by monitoring the final integration stage in the Q branch of the Integrate and Dump Filter (see Figure 3 on page 7). If the magnitude of the integration over the symbol period is less than the integration over half a symbol period, a possible false lock condition is detected; (integration over a symbol period has gone from end-bit to end-bit, while integration over half the symbol period has gone from the previous end-bit to mid-bit). By accumulating the number of these occurrences over the Integration Period, the Lock Detector State Machine determines whether a false lock condition exists. The False Lock Accumulator is used to accumulate the number of possible false lock occurrences over the Integration Period. The False Lock Accumulator can also be configured to accumulate the output of the Frequency Error Detector (see Lock Detection Configuration Control Register Bit 27: Table 35 on page 40).

The Gain Error Accumulator provides a mechanism to estimate data quality (E_S/N_O). The accumulator integrates the magnitude of the gain error of the end-bit samples, over the Integration Period. Note: The Gain Error end-bit data is valid only after lock has been declared, and the demod is the tracking mode. The accumulated value gives an indication of the variance about the ideal constellation points. The accumulator output is read via the Microprocessor Interface. The Gain Error Accumulator is always pre-loaded with zero.

For applications where stepped acquisition is used, a Dwell Counter is provided. In this mode, the lag accumulator in the Carrier Loop Filter is stepped to a new frequency after each Lock Detector integration. The Dwell Counter is used to hold off Lock Accumulator integration until the loop has a chance to settle.

Lock Detector Control

The selection of acquisition and tracking modes is controlled by either the internal state machine or an external microprocessor. The internal state machine monitors the rollover of the Phase Error Accumulator and the False Lock Accumulator relative to the Integration Counter. Depending on whether the accumulators or counter roll over first, the acquisition or tracking parameters are selected for the Loop Filters and the Lock Detector Accumulators. In addition, the state machine controls the frequency sweep input to the Carrier Tracking Loop.

The flow of the acquisition control is shown in the State Diagram in Figure 18 on page 26. The state machine controls the acquisition process described as follows:

Search. The frequency uncertainty is swept by enabling the Frequency Sweep Block to the lag path of the Carrier Tracking Loop Filter. The acquisition parameters are enabled to the Loop Filters and the Lock Detector Accumulators. Phase lock is obtained when the Lock Counter rolls over before the Phase Error Accumulator (average Phase Error is less than the lock threshold).

Verify. Once phase lock is obtained, the frequency sweep is disabled and the tracking parameters are enabled. Lock is verified if the accumulated Phase Error is below the threshold for a programmable number of Integration Periods. False lock conditions are also monitored by comparing the roll over of the False Lock Accumulator to that of the Integration Counter. If the False Lock Accumulator rolls over before the Integration Counter, a false lock condition exists.

False Lock. Once a false lock has been determined, the Frequency Sweep block is enabled to move the carrier tracking beyond the false lock region. The Frequency Sweep is performed for a programmable number of Integration Periods before returning to the search state.

Lock. When phase lock has been verified, the Lock status output is asserted and the False Lock Detector is disabled. The lock state is maintained as long as the Integration Counter rolls over before the Phase Error Accumulator.

If the acquisition and tracking process is controlled externally, the Phase Error Accumulator and False Lock Accumulators are monitored by an external processor to determine when lock has been achieved. In this mode the accumulator pre-loads are typically set to zero and the accumulator output is compared in the processor against a threshold equal to the maximum Phase Error per sample times the number of samples per Integration Period. The accumulators stop after each Integration Period to hold their outputs for reading via the Microprocessor Interface (see Read Enable Address Map; Table 13 on page 28). The accumulators are restarted by writing the Initialize Lock Detector Control address (see Initialize Lock Detector Control Register: Table 45 on page 46). To simplify the processor interface, the LKINT output is provided to interrupt the processor when the accumulator integration period is complete. The processor controls the use of the acquisition/tracking parameters and lock status line by setting the appropriate bits in the Acquisition/Tracking Configuration Control Register (see Table 38 on page 41). In addition, the frequency sweep function is enabled via the Microprocessor Interface.

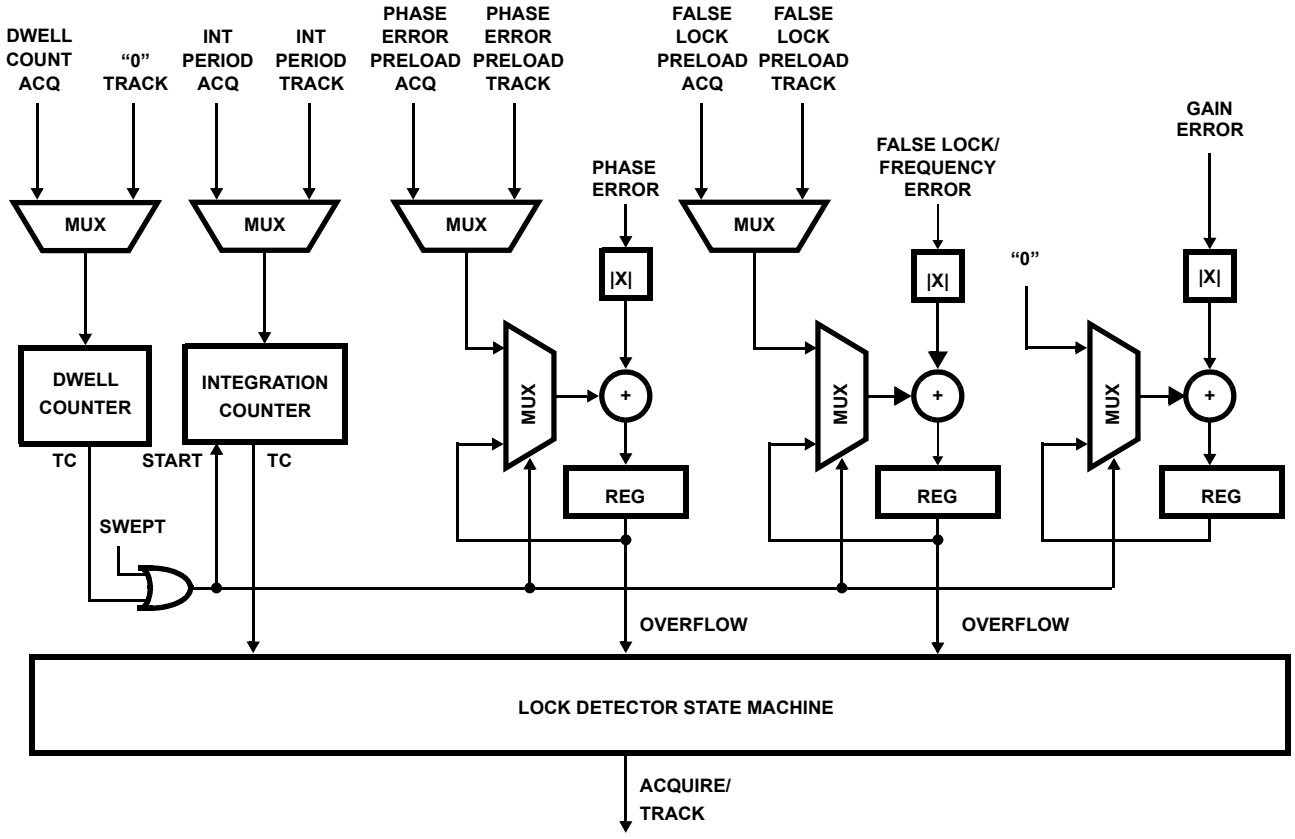


FIGURE 17. LOCK DETECTOR BLOCK DIAGRAM