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Data Sheet May 1, 2007 FN4450.4

Programmable Downconverter

The HSP50214B Programmable Downconverter converts digitized IF data into filtered baseband data which can be processed by a standard DSP microprocessor. The Programmable Downconverter (PDC) performs down conversion, decimation, narrowband low pass filtering, gain scaling, resampling, and Cartesian to Polar coordinate conversion.

The 14-bit sampled IF input is down converted to baseband by digital mixers and a quadrature NCO, as shown in the Block Diagram. A decimating (4 to 32) fifth order Cascaded Integrator-Comb (CIC) filter can be applied to the data before it is processed by up to 5 decimate-by-2 halfband filters. The halfband filters are followed by a 255-tap programmable FIR filter. The output data from the programmable FIR filter is scaled by a digital AGC before being re-sampled in a polyphase FIR filter. The output section can provide seven types of data: Cartesian (I, Q), polar (R, θ), filtered frequency ($d\theta/dt$), Timing Error (TE), and AGC level in either parallel or serial format.

Features

- Up to 65MSPS Front-End Processing Rates (CLKIN) and 55MHz Back-End Processing Rates (PROCCLK) Clocks May Be Asynchronous
- Processing Capable of >100dB SFDR
- Up to 255-Tap Programmable FIR
- Overall Decimation Factor Ranging from 4 to 16384
- Output Samples Rates to $\cong$12.94MSPS with Output Bandwidths to $\cong$ 982kHz Lowpass
- 32-Bit Programmable NCO for Channel Selection and Carrier Tracking
- Digital Resampling Filter for Symbol Tracking Loops and Incommensurate Sample-to-Output Clock Ratios
- Digital AGC with Programmable Limits and Slew Rate to Optimize Output Signal Resolution; Fixed or Auto Gain Adjust
- Serial, Parallel, and FIFO 16-Bit Output Modes
- Cartesian to Polar Converter and Frequency Discriminator for AFC Loops and Demodulation of AM, FM, FSK, and DPSK
- Input Level Detector for External I.F. AGC Support
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

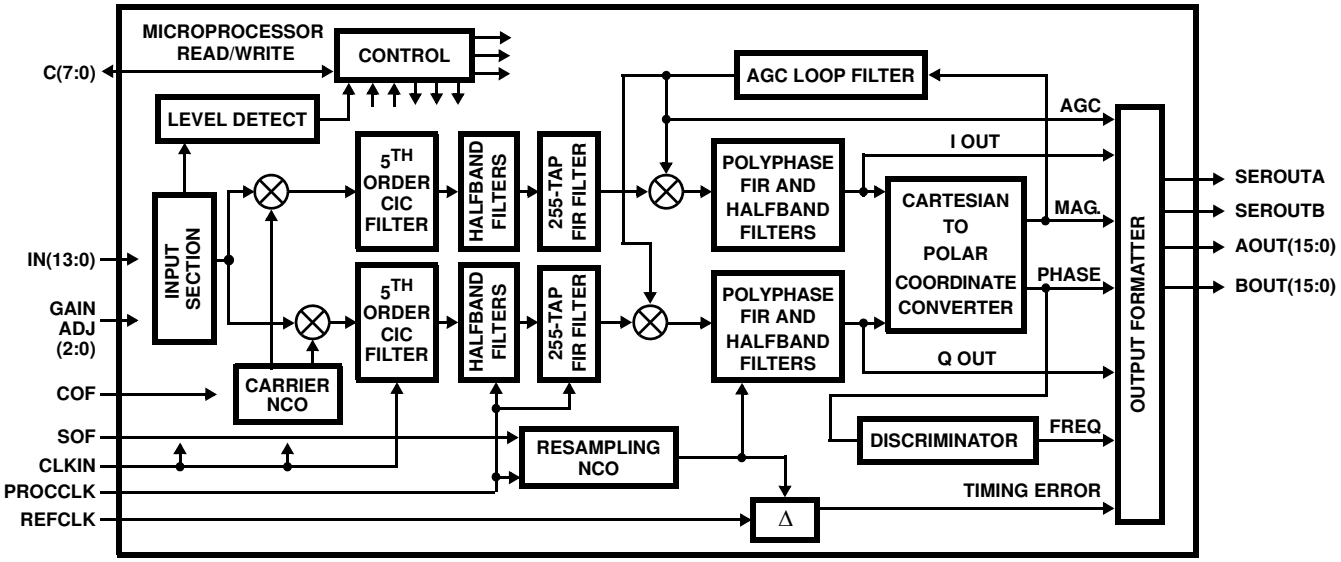
- Single Channel Digital Software Radio Receivers
- Base Station Rx's: AMPS, NA TDMA, GSM, and CDMA
- Compatible with HSP50210 Digital Costas Loop for PSK Reception
- Evaluation Platform Available

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. NO.
HSP50214BVC	HSP50214BVC	0 to +70	120 Ld MQFP	Q120.28x28
HSP50214BVCZ (Note)	HSP50214BVCZ	0 to +70	120 Ld MQFP (Pb-free)	Q120.28x28
HSP50214BVI	HSP50214BVI	-40 to +85	120 Ld MQFP	Q120.28x28
HSP50214BVIZ (Note)	HSP50214BVIZ	-40 to +85	120 Ld MQFP (Pb-free)	Q120.28x28

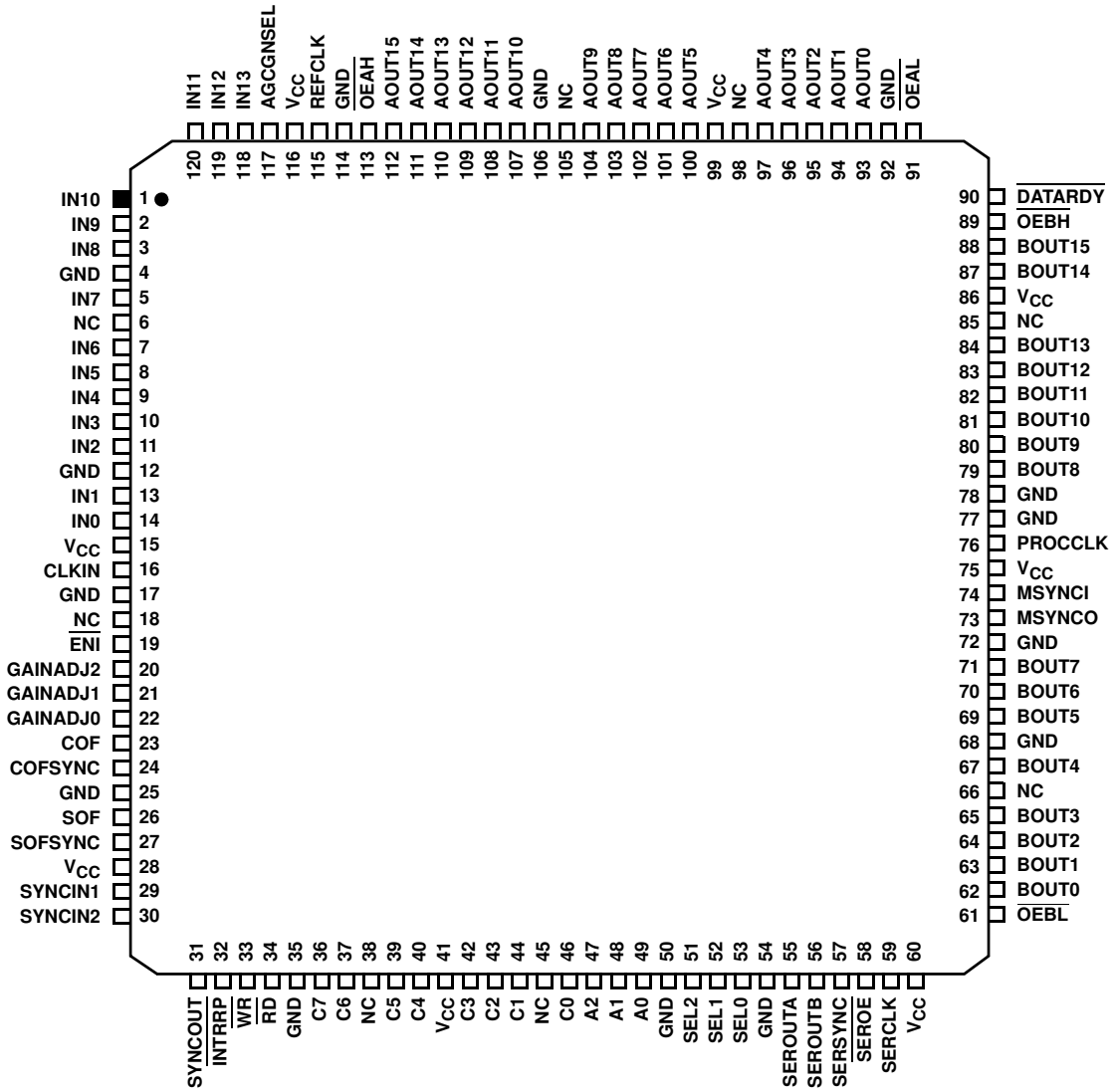
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pinout

HSP50214B
(120 LD MQFP)
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}	-	Positive Power Supply Voltage.
GND	-	Ground.
CLKIN	I	Input Clock. This clock should be a multiple of the input sample rate. All input section processing occurs on the rising edge of CLKIN. The frequency of CLKIN is designated f_{CLKIN}.
IN(13:0)	I	Input Data. The format of the input data may be set to offset binary or 2's complement. IN13 is the MSB (see Control Word 0).
$\overline{ENI}$	I	Input Enable. Active Low. This pin enables the input to the part in one of two modes, gated or interpolated (see Control Word 0). In gated mode, one sample is taken per CLKIN when $\overline{ENI}$ is asserted. The input sample rate is designated f_S, which can be different from f_{CLKIN} when $\overline{ENI}$ is used.
GAINADJ(2:0)	I	GAINADJ Input. Adds an offset to the gain via the shifter following the mixer. GAINADJ value is added to the shift code from the microprocessor (µP) interface. The shift code is saturated to a maximum code of F. The gain is offset by (6dB)(GAINADJ); (000 = 0dB gain adjust; 111 = 42dB gain adjust) GAINADJ2 is the MSB. See "Using the Input Gain Adjust Control Signals" Section.
PROCCLK	I	Processing Clock. PROCCLK is the clock for all processing functions following the CIC Section. Processing is performed on PROCCLK's rising edge. All output timing is derived from this clock. This clock may be asynchronous to CLKIN.
AGCGNSEL	I	AGC Gain Select. This pin selects between two AGC loop gains. This input is setup and held relative to PROCCLK. Gain setting 1 is selected when AGCGNSEL = 1.
COF	I	Carrier Offset Frequency Input. This serial input pin is used to load the carrier offset frequency into the Carrier NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32-bits. The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
COFSYNC	I	Carrier Offset Frequency Sync. This signal is asserted one CLK before the most significant bit (MSB) of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
SOF	I	Re-Sampler Offset Frequency Input. This serial input pin is used to load the offset frequency into the Re-Sampler NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32-bits. The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
SOFSYNC	I	Re-Sampler Offset Frequency Sync. This signal is asserted one CLK before the MSB of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
AOUT(15:0)	O	Parallel Output Bus A. Two parallel output modes are available on the HSP50214B. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of AOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. AOUT15 is the MSB. In this mode, the AOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. For this mode, the output choices are: I, |r|, or f. The format is 2's complement, except for magnitude, which is unsigned binary with a zero as the MSB. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a data type is selected using SEL(2:0). Up to 7 data sets are stored in the Buffer RAM Output Port. The LSBytes of the AOUT and BOUT busses form the 16-bits for the buffered output mode and can be used for buffered mode while the MSBytes are outputting data in the direct output mode. For this mode, the output formats are the same as the Direct Output Port mode.
BOUT(15:0)	O	Parallel Output Bus B. Two parallel output modes are available on the HSP50214B. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of BOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. BOUT15 is the MSB. In this mode, the BOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. For this mode, the output choices are: Q, ϕ, or |r|. The format is 2's complement, except for magnitude which is unsigned binary with a zero as the MSB. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a particular information is selected using SEL(2:0). Up to 7 data sets is stored in the Buffer RAM Output Port. The least significant byte of BOUT can be used to either output the least significant byte of the B Parallel Direct Output Port or the least significant byte of the Buffer RAM Output Port. See Output Section. For this mode the output formats are the same as the Direct Output Port mode.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{DATARDY}}$	O	Output Strobe Signal. Active Low. Indicates when new data from the Direct Output Port Section is available. DATARDY is asserted for one PROCCLK cycle during the first clock cycle that data is available on the parallel out busses. See Output Section.
$\overline{\text{OEAH}}$	I	Output enable for the MSByte of the AOUT bus. Active Low. The AOUT MSByte outputs are three-stated when $\overline{\text{OEAH}}$ is high.
$\overline{\text{OEAL}}$	I	Output enable for the LSByte of the AOUT bus. Active Low. The AOUT LSByte outputs are three-stated when $\overline{\text{OEAL}}$ is high.
$\overline{\text{OEBH}}$	I	Output enable for the MSByte of the BOUT bus. Active Low. The BOUT MSByte outputs are three-stated when $\overline{\text{OEBH}}$ is high.
$\overline{\text{OEBL}}$	I	Output enable for the LSByte of the BOUT bus. Active Low. The BOUT LSByte outputs are three-stated when $\overline{\text{OEBL}}$ is high.
SEL(2:0)	I	Select Address is used to choose which information in a data set from the Buffer RAM Output Port is sent to the least significant bytes of AOUT and BOUT. SEL2 is the MSB.
$\overline{\text{INTRRP}}$	O	Interrupt Output. Active Low. This output is asserted for 8 PROCCLK cycles when the Buffer RAM Output Port is ready for reading.
SEROUTA	O	Serial Output Bus A Data. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SEROUTB	O	Serial Output Bus B Data. Contents may be related to SEROUTA. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SERCLK	O	Output Clock for Serial Data Out. Derived from PROCCLK as given by Control Word 20 in the Microprocessor Write Section.
SERSYNC	O	Serial Output Sync Signal. Serves as serial data strobes. See Output Section and Microprocessor Write Section.
$\overline{\text{SEROE}}$	I	Serial Output Enable. When high, the SEROUTA, SEROUTB, SERCLK, and SERSYNC signals are set to a high impedance.
C(7:0)	I/O	Processor Interface Data Bus. See Microprocessor Write Section. C7 is the MSB.
A(2:0)	I	Processor Interface Address Bus. See Microprocessor Write Section. A2 is the MSB.
$\overline{\text{WR}}$	I	Processor Interface Write Strobe. C(7:0) is written to Control Words selected by A(2:0) in the Programmable Down Converter on the rising edge of this signal. See Microprocessor Write Section.
$\overline{\text{RD}}$	I	Processor Interface Read Strobe. C(7:0) is read from output or status locations selected by A(2:0) in the Programmable Down Converter on the falling edge of this signal. See Microprocessor Read Section.
REFCLK	I	Reference Clock. Used as an input clock for the timing error detector. The timing error is computed relative to REFCLK. REFCLK frequency must be less than or equal to PROCCLK/2.
MSYNCO	O	Multiple Chip Sync Output. Provided for synchronizing multiple parts when CLKIN and PROCCLK are asynchronous. MSYNCO is the synchronization signal between the input section operating under CLKIN and the back end processing operating under PROCCLK. This output sync signal from one part is connected to the MSYNCI signal of all the HSP50214Bs.
MSYNCI	I	Multiple Chip Sync Input. The MSYNCI pin of all the parts should be tied to the MSYNCO of one part. NOTE: MSYNCI must be connected to an MSYNCO signal for operation.
SYNCIN1	I	CIC Decimation/Carrier NCO Update Sync. Can be used to synchronize the CIC Section, carrier NCO update, or both. See the Multiple Chip Synchronization Section and Control Word 0 in the Microprocessor Write Section. Active High.
SYNCIN2	I	FIR/Timing NCO Update/AGC Gain Update Sync. Can be used to synchronize the FIR, Timing NCO update, AGC gain update, or any combination of the above. See the Multiple Chip Synchronization Section and Control Words 7, 8, and 10 in the Microprocessor Write Section. Active High.
SYNCOUT	O	Strobe Output. This synchronization signal is generated by the µP interface for synchronizing multiple parts. Can be generated by PROCLK or CLKIN (see Control Word 0 and Control Word 24 in the Microprocessor Write Section). Active High.

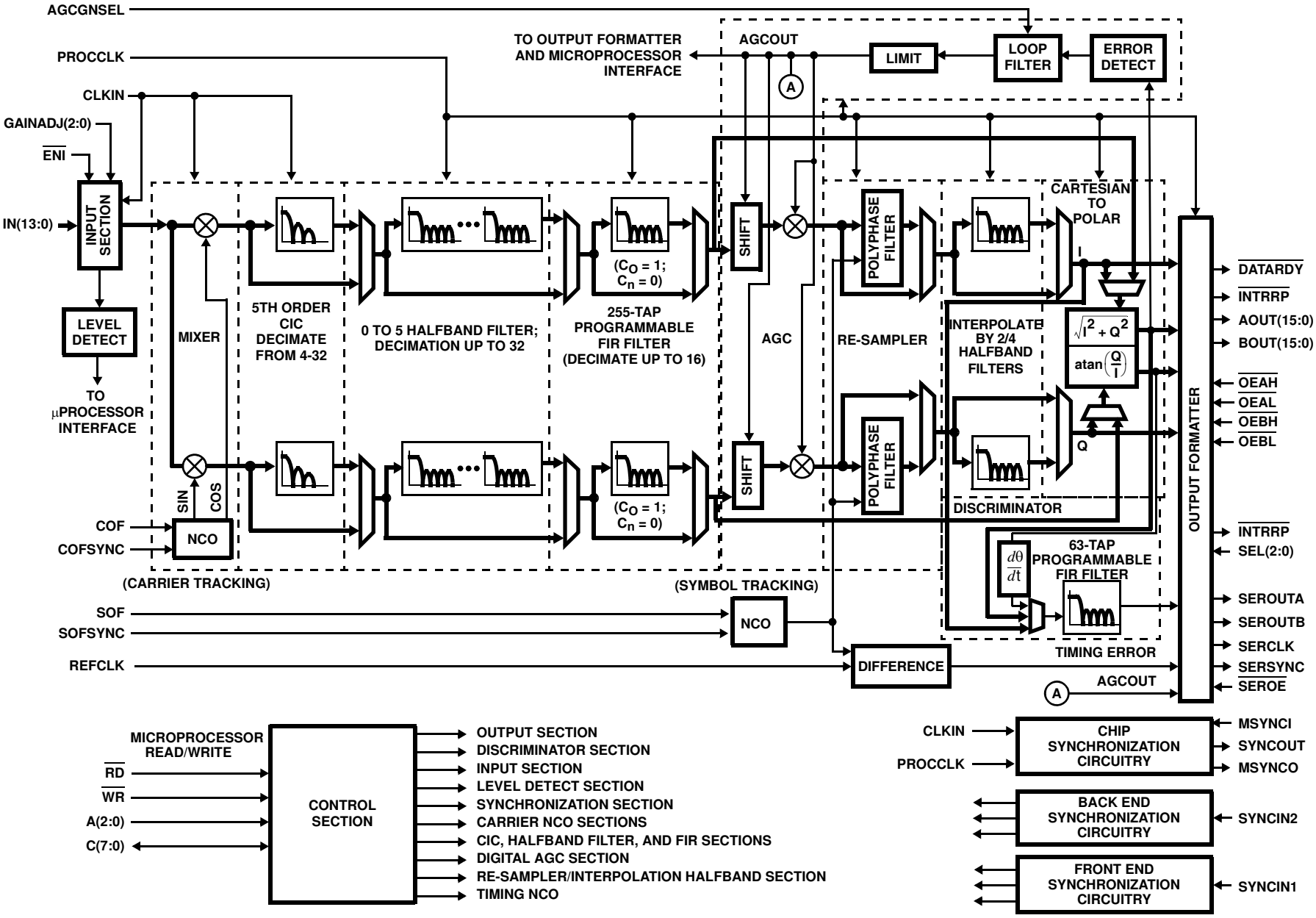


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE HSP50214B PROGRAMMABLE DOWNCONVERTER

Functional Description

The HSP50214B Programmable Downconverter (PDC) is an agile digital tuner designed to meet the requirements of a wide variety of communications industry standards. The PDC contains the processing functions needed to convert sampled IF signals to baseband digital samples. These functions include LO generation/mixing, decimation filtering, programmable FIR shaping/bandlimiting filtering, resampling, Automatic Gain Control (AGC), frequency discrimination and detection as well as multi-chip synchronization. The HSP50214B interfaces directly with a DSP microprocessor to pass baseband and status data.

A top level functional block diagram of the HSP50214B is shown in Figure 1. The diagram shows the major blocks and multiplexers used to reconfigure the data path for various architectures. The HSP50214B can be broken into 13 sections: Synchronization, Input, Input Level Detector, Carrier Mixer/Numerically Control Oscillator (NCO), CIC Decimating Filter, Halfband Decimating Filter, 255-Tap Programmable FIR Filter, Automatic Gain Control (AGC), Re-sampler/Halfband Filter, Timing NCO, Cartesian to Polar Converter, Discriminator, and Output Sections. All of these sections are configured through a microprocessor interface.

The HSP50214B has three clock inputs; two are required and one is optional. The input level detector, carrier NCO, and CIC decimating filter sections operate on the rising edge of the input clock, CLKIN. The halfband filter, programmable FIR filter, AGC, Re-Sampler/Halfband filters, timing NCO, discriminator, and output sections operate on the rising edge of PROCCLK. The third clock, REFCLK, is used to generate timing error information.

NOTE: All of the clocks may be asynchronous.

PDC Applications Overview

This section highlights the motivation behind the key programmable features from a communications system level perspective. These motivations will be defined in terms of ability to provide DSP processing capability for specific modulation formats and communication applications. The versatility of the Programmable Downconverter can be intimidating because of the many Control Words required for chip configuration. This section provides system level insight to help allay reservations about this versatile DSP product. It should help the designer capitalize on the greatest feature of the PDC - ***VERSATILITY THROUGH PROGRAMMABILITY***. It is this feature, when fully understood, that brings the greatest return on design investment by offering a single receiver design that can process the many waveforms required in the communications marketplace.

FDM Based Standards and Applications

Table 1 provides an overview of some common frequency division multiplex (FDM) base station applications to which the PDC can be applied. The PDC provides excellent selectivity for frequency division multiple access (FDMA) signals. This high selectivity is achieved with 0.012Hz resolution frequency control of the NCO and the sharp filter responses capable with a 255-tap, 22-bit coefficient FIR filter. The 16-bit resolution out of the Cartesian to Polar Coordinate Converter are routed to the frequency detector, which is followed by a 63-tap, 22-bit coefficient FIR filter structure for facilitating FM and FSK detection. The 14-bit input resolution is the smallest bit resolution found throughout the conversion and filtering sections, providing excellent dynamic range in the DSP processing. A unique input gain scaler adds an additional 42dB of range to the input level variation, to compensate for changes in the analog RF front end receive equipment. Synchronization circuitry allows precise timing control of the base station reconfiguration for all receive channels simultaneously. Portions of this table were corroborated with reference [2].

TABLE 1. CELLULAR PHONE BASE STATION APPLICATIONS USING FDMA

STANDARD	AMPS (IS-91)	MCS-L1 MCS-L2	NMT-400 NMT-900	C450	ETACS NTACS
RX BAND (MHz)	824-849	925-940	453-458 890-915	451-456	871-904 915-925
CHANNEL BW (kHz)	30	25.0 12.5	25 12.5	20.0 10.0	25.0 12.5
# TRAFFIC CHANNELS	832	600 1200	200 1999	222 444	1240 800
VOICE MODULA-TION	FM	FM	FM	FM	FM
PEAK DEVIATION (kHz)	12	5	5	4	9.5
CONTROL MODULA-TION	FSK	FSK	FSK	FSK	FSK
PEAK DEVIATION (kHz)	8	4.5	3.5	2.5	6.4
CONTROL CHANNEL RATE (Kbps)	10	0.3	1.2	5.3	8

TDM Based Standards and Applications

Table 2 provides an overview of some common Time Division Multiplexed (TDM) base station applications to which the PDC can be applied. For time division multiple access (TDMA) applications, such as North American TDMA (IS136), where 30kHz is the received band of interest for the PCS basestation, the PDC offers 0.012Hz frequency resolution in downconversion in addition to $\alpha = 0.35$ matched (programmable) filtering capability. The $\pi/4$ DPSK modulation can be processed using the PDC Cartesian to Polar coordinate converter and $d\phi/dt$ detector circuitry or by processing the I/Q samples in the DSP μP. The PDC provides

the ability to change the received signal gain and frequency, synchronous with burst timing. The synchronous gain adjustment allows the user to measure the power of the signal at the A/D at the end of a burst, and synchronously reload that same gain value at the arrival of the next user burst.

For applications other than cellular phones (where the preambles are not changed), the PDC frequency discriminator output can be used to obtain correlation on the preamble pattern to aid in burst acquisition.

TABLE 2. CELLULAR BASESTATION APPLICATIONS USING TDMA

STANDARD	GSM	PCN	IS-54
TYPE	Cellular	Cellular	Cellular
BASESTATION RX BAND (MHz)	935-960	1805-1880	824-849
CHANNEL BW (kHz)	200	200	30
# TRAFFIC CHANNELS	8	16	3
VOICE MODULATION	GMSK	GMSK	$\pi/4$ DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6
CONTROL MODULATION	GMSK	GMSK	$\pi/4$ DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6

Several applications are combinations of frequency and time domain multiple access schemes. For example, GSM is a TDMA signal that is frequency hopped. The individual channels contain Gaussian MSK modulated signals. The PDC again offers the 0.012Hz tuning resolution for de-hopping the received signal. The combination of halfband and 256-tap programmable, 22-bit coefficient FIR filters readily performs the necessary matched filtering for demodulation and optimum detection of the GMSK signals.

CDMA Based Standards and Applications

For Code Division Multiple Access (CDMA) type signals, the PDC offers the ability to have a single wideband RF front end, from which it can select a single spread channel of interest. The synchronization circuitry provides for easy control of multiple PDC for applications where multiple received signals are required, such as base-stations.

In IS-95 CDMA, the receive signal bandwidth is approximately 1.2288MHz wide with many spread spectrum channel in the band. The PDC supplies the downconversion and filtering required to receive a single RF channel in the presence of strong adjacent interference. Multiple PDC's would be sourced from a single receive RF chain, each processing a different receive frequency channel. The despreader would usually follow the PDC. In some very specific applications, with short, fixed codes, the filtering and despreading may be possible with innovative use of the programmable, 22-bit coefficient FIR filter. The PDC offers 0.012Hz resolution on tuning to the desired receive channel and excellent rejection of the portions of the band not being processed, via the halfband and 255-tap programmable, 22-bit coefficient FIR filter.

Traditional Modulation Formats

AM, ASK, FM AND FSK

The PDC has the capability to fully demodulate AM and FM modulated waveforms. The PDC outputs 15-bits of amplitude or 16-bits of frequency for these modulation formats. The FM discriminator has a 63-tap programmable, 22-bit coefficient FIR filter for additional signal conditioning of the FM signal. Digital versions of these formats, ASK and FSK are also readily processed using the PDC. Just as in the AM modulated case, ASK signals will use 15-bit magnitude output of the Cartesian to Polar Coordinate converter. Multi-tone FSK can be processed several ways. The frequency information out of the discriminator can be used to identify the received tone, or the filter can be used to identify and power detect a specific tone of the received signal. AMPS is an example of an FM application.

PM AND PSK

The PDC provides the downconversion, demodulation, matched filtering and coordinate conversion required for demodulation of PM and PSK modulated waveforms. These modulation formats will require external carrier and symbol timing recovery loop filters to complete the receiver design. The PDC was designed to interface with the HSP50210 Digital Costas Loop to implement the carrier phase and symbol timing recovery loop filters (for continuous PSK signals-not burst).

Digital modulation formats that combine amplitude and phase for symbol mapping, such as m-ary QAM, can also be downconverted, demodulated, and matched filtered. The received symbol information is provided with 16-bits of resolution in either Cartesian or Polar coordinates to facilitate remapping into bits and to recover the carrier phase. External Symbol mapping and Carrier Recovery Loop Filtering is required for this waveform.

Resampling and Interpolation Filters

Two key features of the resampling FIR filter are that the re-sampler filter allows the output sample rate to be programmed with millihertz resolution and that the output sample rate can be phase locked to an independent separate clock. The re-sampler frees the front end sampling clocks from having to be synchronous or integrally related in rate to the baseband output. The asynchronous relationship between front end and back end clocks is critical in applications where ISDN interfaces drive the baseband interfaces, but the channel sample rates are not related in any way. The interpolation halfband filters can increase the rate of the output when narrow frequency bands are being processed. The increase in output rate allows maximum use of the programmable FIR while preserving time resolution in the baseband data.

14-Bit Input and Processing Resolution

The PDC maintains a minimum of 14-bits of processing resolution through to the output, providing over 84dB of dynamic range. The 18-bits of resolution on the internal references provide a spurious floor that is better than 98dBc. Furthermore, the PDC provides up to 42dB of gain scaling to compensate for any change in gain in the RF front end as well as up to 96dB of gain in the internal PDC AGC. This gain maximizes the output resolution for small signals and compensates for changes in the RF front end gain, to handle changes in the incoming signal.

Summary

The greatest feature of the PDC is its ability to be reconfigured to process many common standards in the communications industry. Thus, a single hardware element can receive and process a wide variety of signals from PCS to traditional cellular, from wireless local loop to SATCOM. The high resolution frequency tuning and narrowband filtering are instrumental in almost all of the applications.

Multiple Chip Synchronization

Multiple PDCs are synchronized using a MASTER/SLAVE configuration. One part is responsible for synchronizing the front end internal circuitry using CLKIN while another part is responsible for synchronizing the backend internal circuitry using PROCCLK.

The PDC is synchronized with other PDCs using five control lines: SYNCOUT, SYNCIN1, SYNCIN2, MSYNCO, and MSYNCI. Figure 2 shows the interconnection of these five signals for multiple chip synchronization where different sources are used for CLKIN and PROCCLK.

PDC A is the Master sync through MSO.

PDC B configures the CLKIN sync through SYNCIN1.

PDC A configures the PROCCLK sync through SYNCIN2.

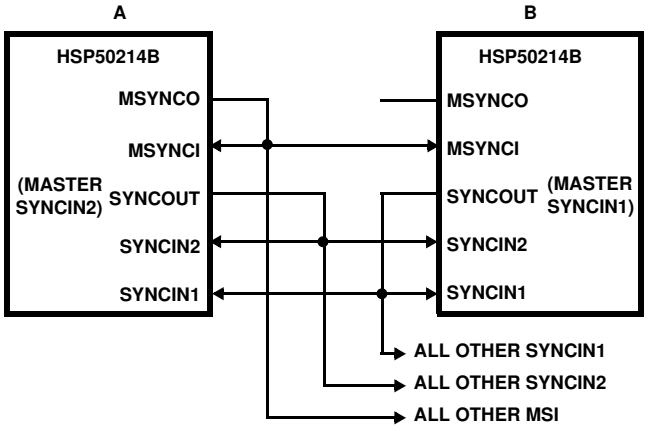


FIGURE 2. SYNCHRONIZATION CIRCUIT

SYNCOUT for PDC B should be set to be synchronous with CLKIN (Control Word 0, Bit 3 = 0. See the Microprocessor Write Section). SYNCOUT for PDC B is tied to the SYNCIN1 of all the PDCs. The SYNCIN1 can be programmed so that the carrier NCO and/or the 5th order CIC filter of all PDCs can be synchronously loaded/updated using SYNCIN1. See Control Word 0, Bits 19 and 20 in the Microprocessor Write Section for details.

SYNCOUT for one of the PDC's other than PDC B, should be set for PROCCLK (bit 3 = 1 in Control Word 0). This output signal is tied to the SYNCIN2 of all PDCs. The SYNCIN2 can be programmed so that the AGC updates its accumulator with the contents in the master registers (Control Word 8, Bit 29 in the Microprocessor Write Section). SYNCIN2 is also used to load or reset the timing NCO using bit 5, Control Word 11. The halfband and FIR filters can be reset on SYNCIN2 using Control Word 7, Bit 21. The MSYNCO of one of the PDCs is then used to drive the MSYNCI of all the PDCs (including its own).

For application configurations where CLKIN and PROCCLK have the same source, SYNCIN1 and SYNCIN2 can be tied together. However, if different enabling is desired for the front end and backend processing of the PDC's, these signals can still be controlled independently.

In the HSP50214B, the Control Word 25 reset signal has been extended so that the front end reset is 10 CLKIN periods wide and the back end reset is 10 PROCCLK periods wide. This guarantees that no enables will be caught in the pipelines. In addition, the SYNCIN1 internal reset signal, which is enabled by setting Control Word 7, Bit 21 = 1, has been extended to 10 cycles.

In summary, SYNCIN1 is used to update carrier phase offset, update carrier center frequency, reset CIC decimation counters and reset the carrier NCO (clear the feedback in the NCO). SYNCIN2 is used to reset the HB filter, FIR filter, re-sampler/HB state machines and the output FIFO, load a new gain into the AGC and load a new re-sampler NCO center frequency and phase offset.

Input Section

The block diagram of the input controller is provided in Figure 3. The input can support offset binary or two's complement data and can be operated in gated or interpolated mode (see Control Word 0 from the Microprocessor Write Section). The gated mode takes one sample per clock when the input enable (ENI) is asserted. The gated mode allows the user to synchronize a low speed sampling clock to a high speed CLKIN.

The interpolated mode allows the user to input data at a low sample rate and to zero-stuff the data prior to filtering. This zero stuffing effectively interpolates the input signal up to the rate of the input clock (CLKIN). This interpolated mode allows the part to be used at rates where the sampling frequency is above the maximum input rate range of the halfband filter section, and where the desired output bandwidth is too wide to use a Cascaded Integrator Comb (CIC) filter without significantly reducing the dynamic range.

See Figures 4 to 7 for an interpolated input example, detailing the associated spectral results.

Interpolation Example:

The specifications for the interpolated input example are:

CLKIN = 40MHz
Input Sample Rate = 5MSPS
PROCCLK = 28MHz
Interpolate by 8, Decimate by 10
Desired 85dB dynamic range output bandwidth = 500kHz

Input Level Detector

The Input Level Detector Section measures the average magnitude error at the PDC input for the microprocessor by comparing the input level against a programmable threshold and then integrating the result. It is intended to provide a gain error for use in an AGC loop with either the RF/IF or A/D converter stages (see Figure 8). The AGC loop includes Input Level Detector, the microprocessor and an external gain control amplifier (or attenuator). The input samples are rectified and added to a threshold programmed via the microprocessor interface, as shown in Figure 9. The bit weighting of the data path through the input threshold detector is shown in Figure 10. The threshold is a signed number, so it should be set to the inverse of the desired input level. The threshold can be set to zero if the average input level is desired instead of the error. The sum of the threshold and the absolute value of the input is accumulated in a 32-bit accumulator. The accumulator can handle up to 2^{18} samples without overflow. The integration time is controlled by an 18-bit counter. The integration counter preload (ICPrel) is programmed via the microprocessor interface through Control Word 1. Only the upper 16-bits are programmable. The 2 LSBs are always zero. Control Word 1, Bits 29-14 are programmed to:

$$ICPrel = (N)/4 + 1 \quad \text{(EQ. 1)}$$

where N is the desired integration period, defined as the number of input samples to be integrated. N must be a multiple of 4: [0, 4, 8, 12, 16 .... , 2^{18}].

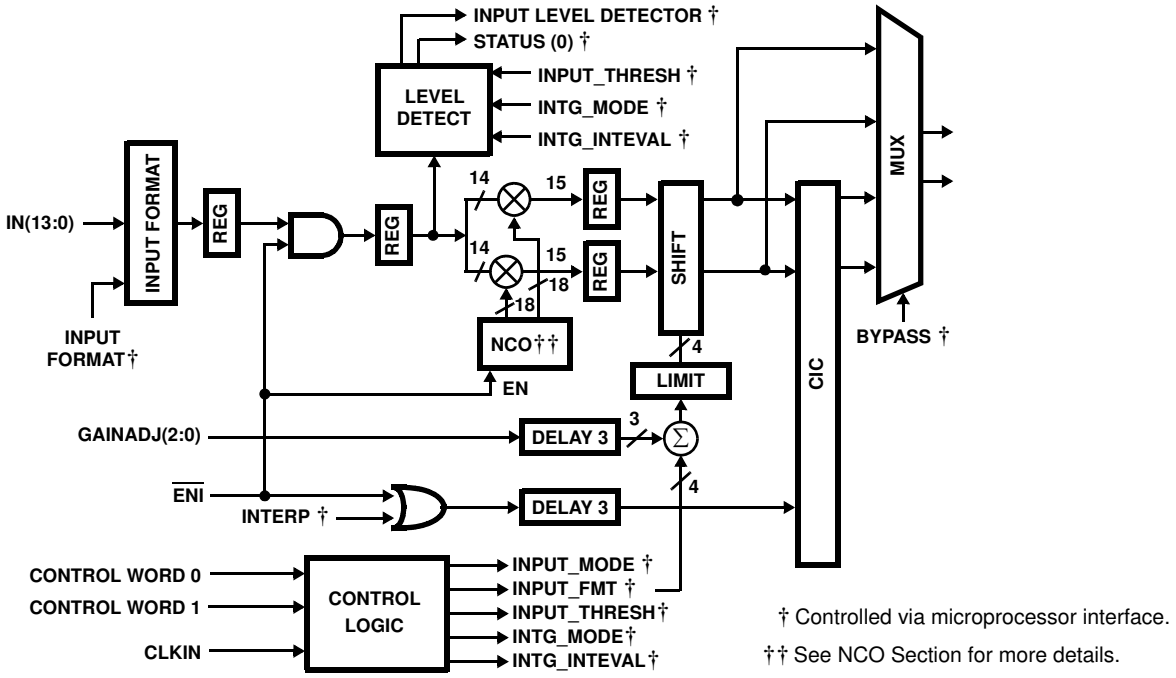
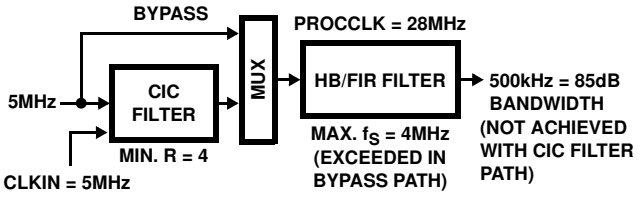


FIGURE 3. BLOCK DIAGRAM OF THE INPUT SECTION



Without Interpolation, the CIC bypass path exceeds the HB/FIR filter input sample rate and the CIC filter path will not yield the desired 85dB dynamic range band width of 500kHz.

FIGURE 4. STATEMENT OF THE PROBLEM

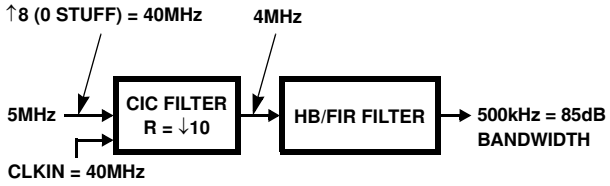


FIGURE 5. BLOCK DIAGRAM OF THE INTERPOLATION APPROACH

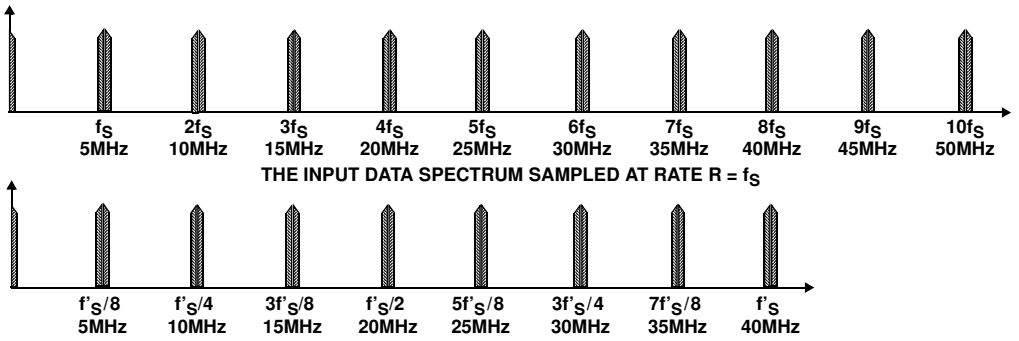


FIGURE 6. INTERPOLATION SPECTRUM: INTERPOLATE BY 8 THE INPUT DATA WITH ZERO STUFFING; SAMPLE AT RATE R = f's

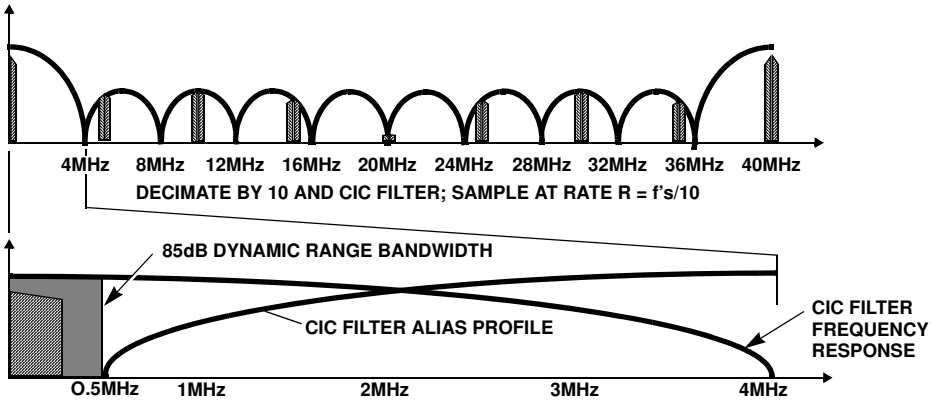


FIGURE 7. ALIAS PROFILE AND THE 85dB DYNAMIC RANGE BANDWIDTH

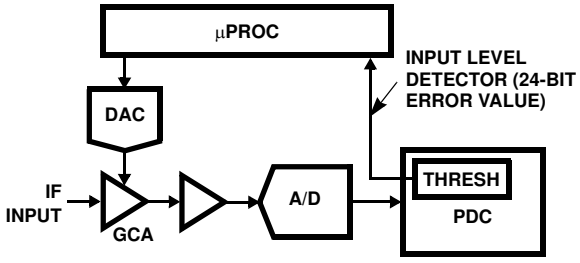


FIGURE 8. PROCESSOR BASED EXTERNAL IF AGC

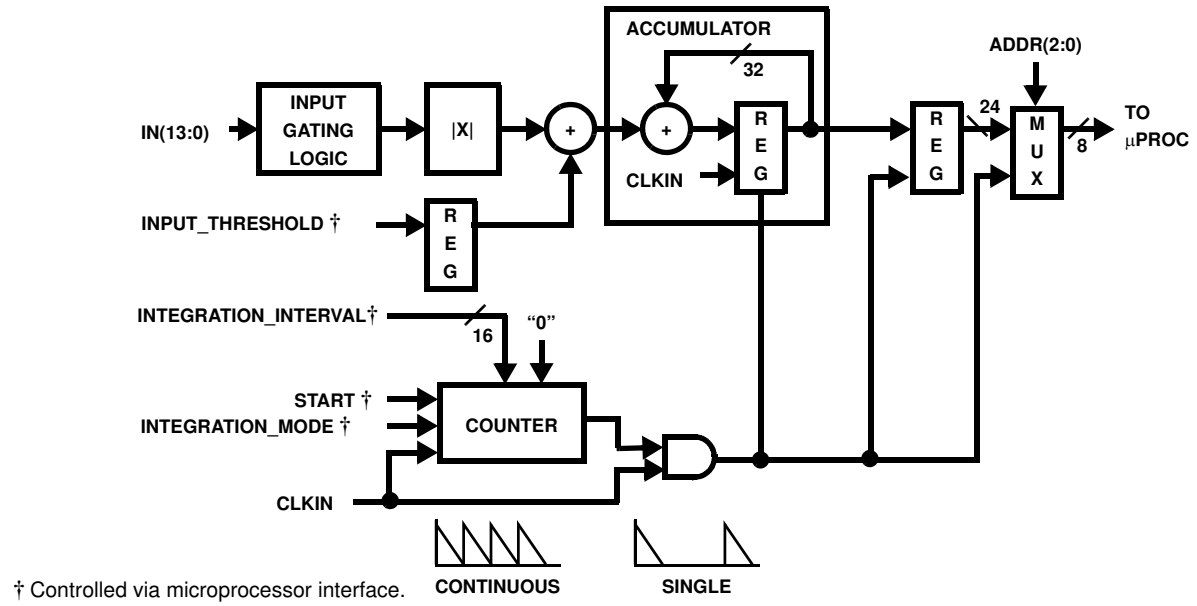


FIGURE 9.

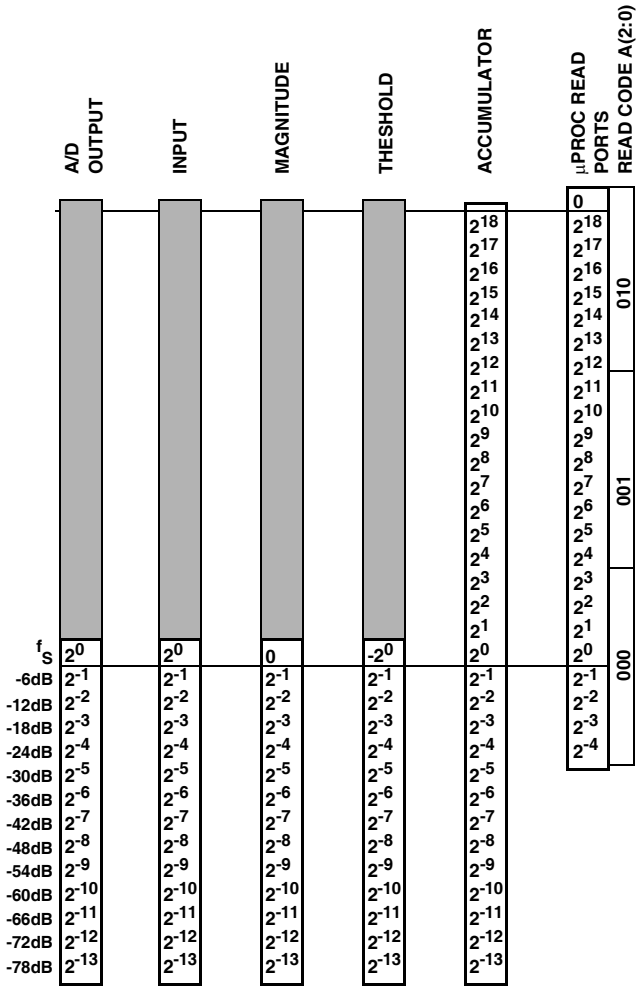


FIGURE 10. INPUT THRESHOLD DETECTOR BIT WEIGHTING

The integration period counter can be set up to run continuously or to count down and stop. Continuous integration counter operation lets the counter run, with sampling occurring every time the counter reaches zero. Because the processor samples the detector read port asynchronous to the CLKIN, data can be missed unless the status bit is monitored by the processor to ensure that a sample is taken for every integration count down sequence.

Additionally, in the HSP50214B, the ability to align the start/restart of the input level detector integration period with an external event is provided. This allows the sync signals, which are synchronized to external events, to be used to align all of the gain adjustments or measurements. If Control Word 27, Bit 17 is set to a logic one, the SYNCIN1 signal will cause the input level detector to start/restart its integration period. If Control Word 27, Bit 17 is set to a logic zero, control of the start/restart of the input level detector integration period does not respond to SYNCIN1.

In the count down and stop mode, the microprocessor read commands can be synchronized to system events, such as the start of a burst for a TDMA application. The integration counter can be started at any time by writing to Control Word 2. At the end of the integration period (counter = 0000), the upper 23-bits of the accumulator are transferred to a holding register for reading by the microprocessor. Note that it is not the restarting of the counter (by writing to Control Word 2) that latches the current value, but the end of the integration count. When the accumulator results are latched, a bit is set in the Status Register to notify the processor. Reading the most significant byte of the 23-bits clears the status bit. See the Microprocessor Read Section. Figure 11 illustrates a typical AGC detection process.

Typically, the average input error is read from the Input Level Detector port for use in AGC Applications. By setting the threshold to 0, however, the average value of the input signal can be read directly. The calculation is:

$$dBFS_{RMS} = (20)\log[(1.111)(level)/((N)(16))] \quad \text{(EQ. 2)}$$

where "level" is the 24-bit value read from the 3 level Detector Registers and "N" is the number of samples to be integrated. Note that to get the RMS value of a sinusoid, multiply the average value of the rectified sinusoid by 1.111. For a full scale input sinusoid, this yields an RMS value of approximately $3dBf_S$.

NOTE: 1.111 scales the rectified sinusoid average ($2/\pi$) to $1/\sqrt{2}$

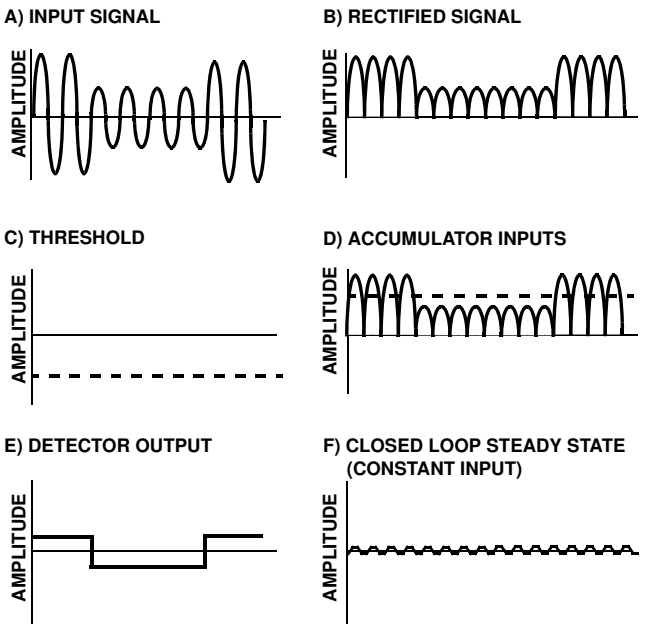


FIGURE 11. SIGNAL PROCESSING WITHIN LEVEL DETECTOR

In the HSP50214B, the polarity of the LSB's of the integration period pre-load is selectable. If Control Word 27, Bit 23 is set to a logic one, the two LSB's of the integration period preload are set to logic ones. This allows a power of two to be set for the integration period, for easy normalization in the processor. If Control Word 27, Bit 23 is set to a logic zero, then the two LSB's of the integration period preload are set to zeros as in the HSP50214.

Carrier Synthesizer/Mixer

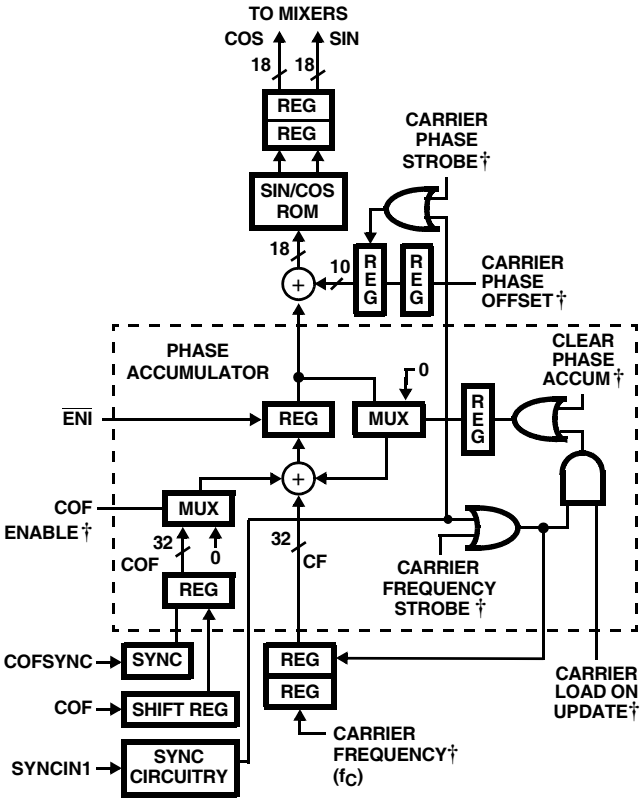
The Carrier Synthesizer/Mixer Section of the HSP50214B is shown in Figure 12. The NCO has a 32-bit phase accumulator, a 10-bit phase offset adder, and a sine/cosine ROM. The frequency of the NCO is the sum of a center frequency Control Word, loaded via the microprocessor interface (Control Word 3, Bits 0 to 31), and an offset frequency, loaded serially via the COF and COFSYNC pins. The offset frequency can be zeroed in Control Word 0, Bit 1. Both frequency control terms are 32-bits and the addition is modulo 2^{32}. The output frequency of the NCO is computed as:

$$f_C = f_S * N/(2^{32}), \quad \text{(EQ. 3)}$$

or in terms of the programmed value:

$$N = INT[f_C \times 2^{32}/f_S]_{HEX}, \quad \text{(EQ. 3A)}$$

where N is the 32-bit sum of the center and offset frequency terms, f_C is the frequency of the carrier NCO sinusoids, f_S is the input sampling frequency, and INT is the integer of the computation. See the Microprocessor Write Section on instructions for writing Control Word 3.



† Controlled via microprocessor interface.

FIGURE 12. BLOCK DIAGRAM OF NCO SECTION

For example, if N is 3267 (decimal), and f_S is 65MHz, then f_C is 49.44Hz. If received data is modulated at a carrier frequency of 10MHz, then the synthesizer/mixer should be programmed for N = 27627627 (hex) or D89D89D8 (hex).

Because the input enable, ENI, controls the operation of the phase accumulator, the NCO output frequency is computed relative to the input sample rate, f_S, not to f_{CLKIN}. The frequency control, N, is interpreted as two's complement because the output of the NCO is quadrature. Negative frequency L.O.s select the upper sideband; positive frequency L.O.s select the lower sideband. The range of the NCO is $-f_S/2$ to $+f_S/2$. The frequency resolution of the NCO is $f_S/(2^{32})$ or approximately 0.015Hz when CLKIN is 65MSPS and ENI is tied low.

The phase of the Carrier NCO can be shifted by adding a 10-bit phase offset to the MSB's (modulo 360^o) of the output of the phase accumulator. This phase offset control has a resolution of 0.35^o and can be interpreted as two's complement from -180^o to 180^o ($-\pi$ to π) or as binary from 0 to 360^o (0 to 2π). The phase offset is given by:

$$\phi_{OFF} = 2\pi \times (PO/2^{10}); (-(2^9) \le PO \le (2^9 - 1)) \quad (-512 \text{ to } 511) \quad \text{(EQ. 4)}$$

or, in terms of the parameter to be programmed:

$$PO = INT[(2^{10}\phi_{OFF})/2\pi]_{HEX}; (-\pi < \phi_{OFF} < \pi) \quad \text{(EQ. 4A)}$$

where PO is the 10-bit two's complement value loaded into the Phase Offset Register (Control Word 4, Bits 9-0). For example, a value of 32 (decimal) loaded into the Phase Offset Register would produce a phase offset of 11.25^o and a value of -512 would produce an offset of 180^o. The phase offset is loaded via the microprocessor interface. See the Microprocessor Write Section on instructions for writing Control Word 4.

The most significant 18-bits from the phase adder are used as the address a sin/cos lookup table. This lookup table maps phase into sinusoidal amplitude. The sine and cosine values have 18-bits of amplitude resolution. The spurious components in the sine/cosine generation are at least -102dBc. The sine and cosine samples are routed to the mixer section where they are multiplied with the input samples to translate the signal of interest to baseband.

The mixer multiplies the 14-bit input by the 18-bit quadrature sinusoids. The mixer equations are:

$$I_{OUT} = I_{IN} \times \cos(\omega_c) \quad \text{(EQ. 5)}$$

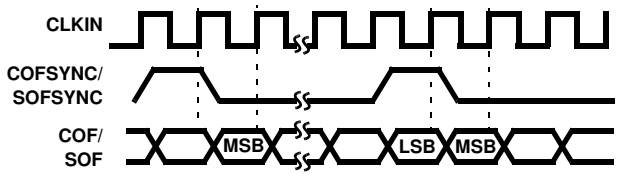
$$Q_{OUT} = I_{IN} \times \sin(\omega_c) \quad \text{(EQ. 5A)}$$

The mixer output is rounded symmetrically to 15-bits.

To allow the frequency and phase of multiple parts to be updated synchronously, two sets of registers are used for latching the center frequency and phase offset words. The offset phase and center frequency Control Words are first loaded into holding registers. The contents of the holding registers are transferred to active registers in one of two ways. The first technique involves writing to a specific Control Word Address. A processor write to Control Word 5, transfers the center frequency value to the active register while a processor write to Control Word 6 transfers the phase offset value to the active register.

The second technique, designed for synchronizing updates to multiple parts, uses the SYNCIN1 pin to update the active registers. When Control Word 1, Bit 20 is set to 1, the SYNCIN1 pin causes both the center frequency and Phase Offset Holding Registers to be transferred to active registers. Additionally, when Control Word 0, Bit 0 is set to 1, the feedback in the phase accumulator is zeroed when the transfer from the holding to active register occurs. This feature provides synchronization of the phase accumulator starting phase of multiple parts. It can also be used to reset the phase of the NCO synchronous with a specific event.

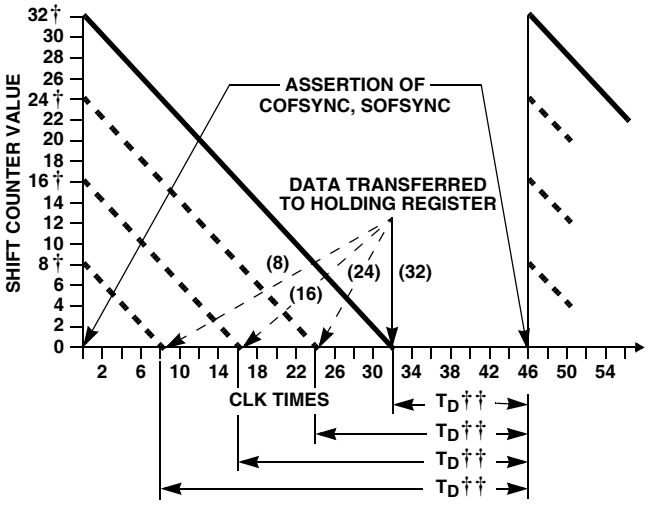
The carrier offset frequency is loaded using the COF and COFSYNC pins. Figure 13 details the timing relationship between COF, COFSYNC and CLKIN. The offset frequency word can be zeroed if it is not needed. Similarly, the Sample Offset Frequency Register controlling the Re-Sampler NCO is loaded via the SOF and SOFSYNC pins. The procedure for loading data through the two pin NCO interfaces is identical except that the timing of SOF and SOFSYNC is relative to PROCCLK.



NOTE: Data must be loaded MSB first.

FIGURE 13. SERIAL INPUT TIMING FOR COF AND SOF INPUTS

Each serial word has a programmable word width of either 8, 16, 24, or 32-bits (See Control Word 0, Bits 4 and 5, for the Carrier NCO programming and Control Word 11, Bits 3 and 4, for Timing NCO programming). On the rising edge of the clock, data on COF or SOF is clocked into an input shift register. The beginning of a serial word is designated by asserting either COFSYNC or SOFSYNC "high" one CLK period prior to the first data bit.



†Serial word width can be: 8, 16, 24, 32 bits wide.

††T_D is determined by the COFSYNC, COFSYNC rate.

FIGURE 14. HOLDING REGISTERS LOAD SEQUENCE FOR COF AND SOF SERIAL OFFSET FREQUENCY DATA

NOTE: Serial Data must be loaded MSB first, and COFSYNC or SOFSYNC should not be asserted for more than one CLK cycle.

NOTE: COF loading and timing is relative to CLKIN while SOF loading and timing is relative to PROCCLK.

NOTE: T_D can be 0, and the fastest rate is with 8-bit word width.

The assertion of the COFSYNC (or SOFSYNC) starts a count down from the programmed word width. On following CLKs, data is shifted into the register until the specified number of bits have been input. At this point the contents of the register are transferred from the Shift Register to the respective 32-bit Holding Register. The Shift Register can accept new data on the following CLK. If the serial input word is defined to be less than 32-bits, it will be transferred to the MSBs of the 32-bit Holding Register and the LSBs of the Holding Register will be zeroed. See Figure 14 for details.

CIC Decimation Filter

The mixer output may be filtered with the CIC filter or it may be routed directly to the halfband filters. The CIC filter is used to reduce the sample rate of a wideband signal to a rate that the halfbands and programmable filters can process, given the maximum computation speed of PROCCLK. (See Halfband and FIR Filter Sections for techniques to calculate this value).

Prior to the CIC filter, the output of the mixer goes through a barrel shifter. The shifter is used to adjust the gain in 6dB steps to compensate for the variation in CIC filter gain with decimation. (See Equation 6). Fine gain adjustments must be done in the AGC Section. The shifter is controlled by the sum of a 4-bit CIC Shift Gain word from the microprocessor and a 3-bit gain word from the GAINADJ(2:0) pins. The three bit value is pipelined to match the delay of the input samples. The sum of the 3 and 4-bit shift gain words saturates at a value of 15. Table 1 details the permissible values for the GAINADJ(2:0) barrel shifter control, while Figure 15 shows the permissible CIC Shift Gain values.

The CIC filter structure for the HSP50214B is fifth order; that is it has five integrator/comb pairs. A fifth order CIC has 84dB of alias attenuation for output frequencies below 1/8 the CIC output sample rate.

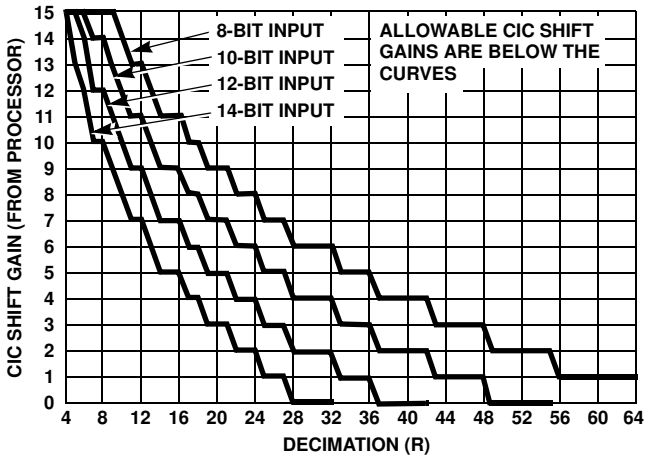


FIGURE 15. CIC SHIFT GAIN VALUES

The decimation factor of the CIC filter is programmed in Control Word 0, Bits 12 - 7. The CIC Shift Gain is programmed in Control Word 0, Bits 16-13. The CIC Bypass is set in Control Word 0, Bit 6. When bypassing the CIC filter, the $\overline{ENI}$ signal must be de-asserted between samples, i.e., the CLKIN rate must be $\geq 2 \bullet f_S$.

TABLE 3. GAIN ADJUST CONTROL AND CIC DECIMATION

ΔGAIN VALUE (dB)	GAIN ADJ(2:0)	MAX. CIC DECIMATION
0	000	32
6	001	27
12	010	24
18	011	21
24	100	18
30	101	16
36	110	12
42	111	10

CIC Gain Calculations

The gain through the CIC filter increases with increased decimation. The programmable barrel shifter that precedes the first integrator in the CIC is used to offset this variation. Gain variations due to decimation should be offset using the 4-bit CIC Shift Gain word. This allows the input signal level to be adjusted in 6dB steps to control the CIC output level.

The gain at each stage of the CIC is:

$$k = R^N, \quad \text{(EQ. 6)}$$

where R is the decimation factor and N is the number of stages. The input to the CIC from the mixer is 15-bits, and the bit widths of the accumulators for the five stages in the HSP50214B are 40, 36, 32, 32, and 32, as shown in Figure 16. This limits the maximum decimation in the CIC to 32 for a full scale input.

If R is 32, the gain through all five integrator stages is $32^5 = 2^{25}$. (The gain through the last four CIC stages is 2^{20}, through the

last 3 it is 2^{15}, etc.). The sum of the input bits and the growth bits cannot exceed the accumulator size. This means that for a decimation of 32 and 15 input bits, the first accumulator must be 15 + 25 = 40-bits.

Thus, the value of the CIC Shift Gain word can be calculated:

$$SG = FLOOR\ [39 - (IIN) - \log_2(R)^5 \text{ for } 4<R<32 \quad = 15 \text{ for } R = 4 \qquad \text{(EQ. 7)}$$

NOTE: The number of input bits is IIN. (If the number of bits into the CIC filter is used, the value 40 replaces 39).

For 14-bits, Equation 7 becomes:

$$SG = FLOOR[25 - \log_2(R)^5] \text{for } 4 < R < 32 \quad = 15 \text{ for } R = 4 \qquad \text{(EQ. 8A)}$$

For 12-bits, Equation 7 becomes:

$$SG = FLOOR[27 - \log_2(R)^5] \text{for } 5 < R < 40 \quad = 15 \text{ for } 4 \leq R \leq 5 \qquad \text{(EQ. 8B)}$$

For 10-bits, Equation 7 becomes:

$$SG = FLOOR[29 - \log_2(R)^5] \text{for } 6 < R < 52 \quad = 15 \text{ for } 4 \leq R \leq 6 \qquad \text{(EQ. 8C)}$$

For 8-bits, Equation 7 becomes:

$$SG = FLOOR[31 - \log_2(R)^5] \text{for } 9 < R < 64 \quad = 15 \text{ for } 4 \leq R \leq 9 \qquad \text{(EQ. 8D)}$$

Figure 15 is a plot of Equations 8A through 8D. The 4-bit CIC Shift Gain word has a range from 0 to 15. The 6-bit Decimation Factor counter preload field, (R-1), has a range from 0 to 63, limited by the input resolution as cited above.

Using the Input Gain Adjust Control Signals

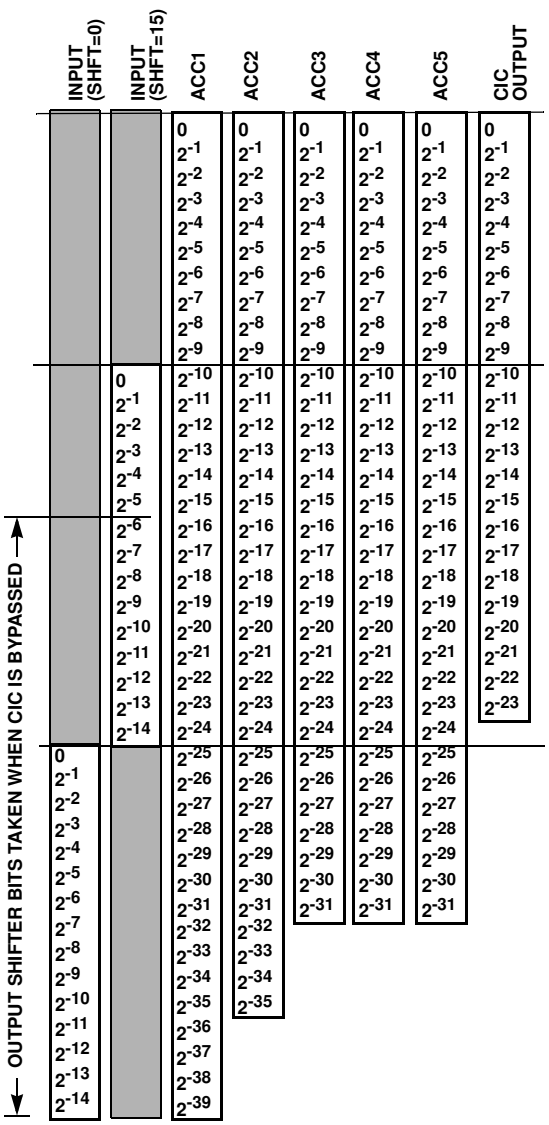
The input gain offset control GAINADJ(2:0)) is provided to offset the signal gain through the part, i.e., to keep the CIC filter output level constant as the analog front end attenuation is changed. The gain adjust offset is 6dB per code, so the gain adjust range is 0 to 42dB. For example, if 12dB of attenuation is switched in at the receiver RF front end, a code of 2 would increase the gain at the input to the CIC filter up 12dB so that the CIC filter output would not drop by 12dB. This fixed gain adjust eliminates the need for the software to continually normalize.

One must exercise care when using this function as it can cause overflow in the CIC filter. Each gain adjust in the shifter from the gain adjust control signals is the equivalent of an extra bit of input. The maximum decimation in the CIC is reduced accordingly. With a decimation of 32, all 40-bits of the CIC are needed, so no input offset gain is allowed. As the decimation is reduced, the allowable offset gain increases. Table 3 shows the decimation range versus desired offset gain range. Table 3 assumes that the CIC Shift Gain has been programmed per Equation 7 or 8A.

The CIC filter decimation counter can be loaded synchronous with other PDC chips, using the SYNCIN1 signal and the CIC External Sync Enable bit. The CIC external Sync Enable is set via Control Word 0, Bit 19.

Halfband Decimating Filters

The Programmable Down Converter has five halfband filter stages, as shown in Figure 17. Each stage decimates by 2 and filters out half of the available bandwidth. The first halfband, or HB1, has 7 taps. The remaining halfbands; HB2, HB3, HB4, and HB5; have 11, 15, 19, and 23 taps respectively. The coefficients for these halfbands are given in Table 4. Figure 18 shows the frequency response of each of the halfband filters with respect to normalized frequency, F_N. Frequency normalization is with respect to the input sampling frequency of each filter section. Each stage is activated by their respective bit location (15-20) in Control Word 7. Any combination of halfband filters may be used, or all may be bypassed.



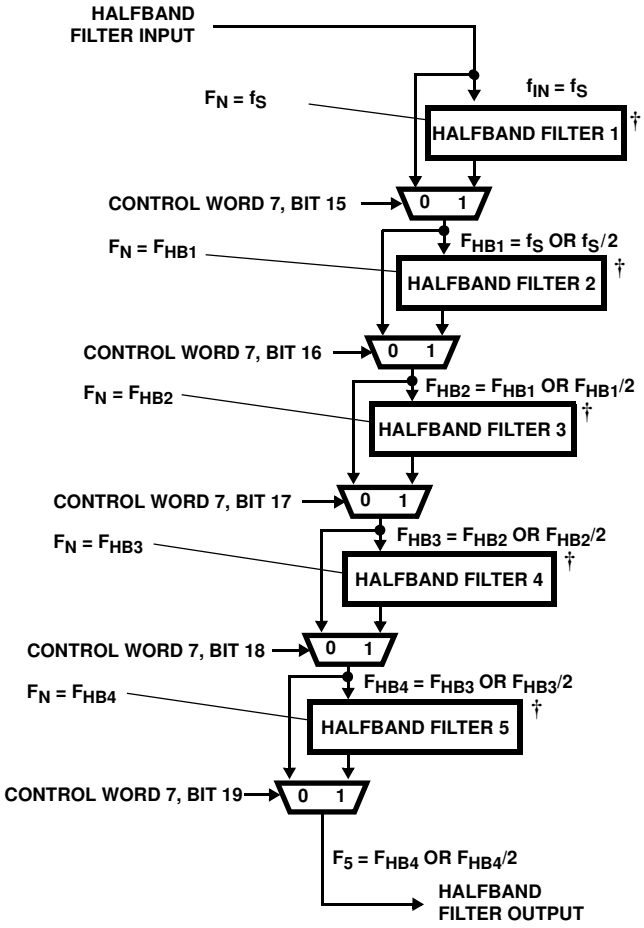
***NOTE:** If 14 input bits are not needed, the gain adjust can be increased by one for each bit that the input is shifted down at the input. For example, if only 12-bits are needed, an offset range of 24dB is possible for a decimation of 24.*

FIGURE 16. CIC FILTER BIT WEIGHTING

Since each halfband filter section decimates by 2, the total decimation through the halfband filter is given by:

$$DEC_{HB} = 2^N \quad \text{(EQ. 9)}$$

where N = Number of Halfband Filters Selected (1 - 5).



† Each halfband section decimates by 2.

FIGURE 17. BLOCK DIAGRAM OF HALFBAND FILTER SECTION

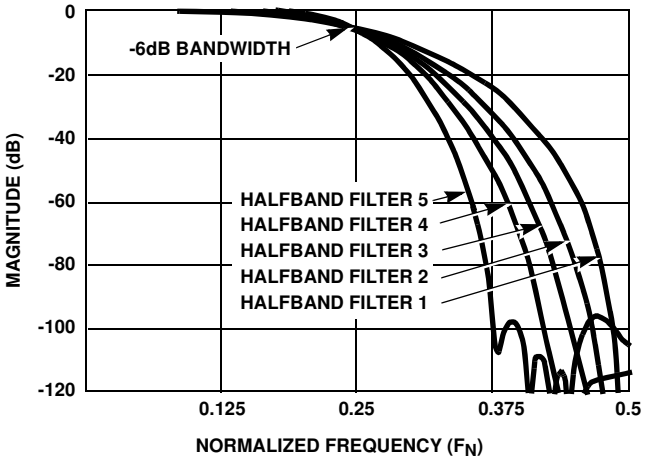


FIGURE 18. HALFBAND FILTER FREQUENCY RESPONSE

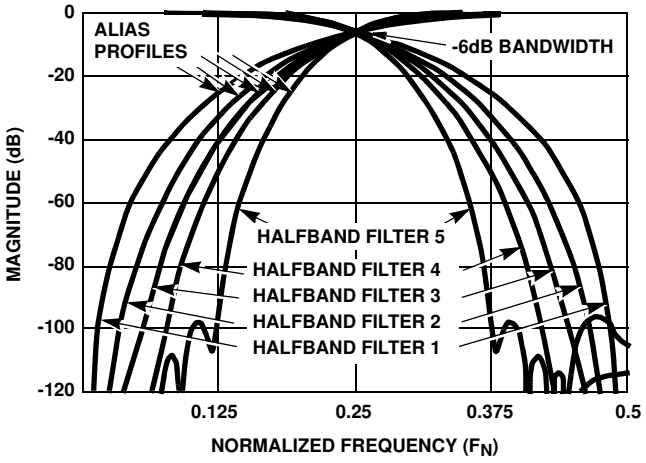


FIGURE 19. HALFBAND FILTER ALIAS CONSIDERATIONS

TABLE 4. HALFBAND FILTER COEFFICIENTS

COEFFICIENTS	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C0	- 0.031303406	0.005929947	-0.00130558	0.000378609	-0.000347137
C1	0.000000000	0.000000000	0.000000000	0.000000000	0.000000000
C2	0.281280518	-0.049036026	0.012379646	-0.003810883	0.00251317
C3	0.499954224	0.000000000	0.000000000	0.000000000	0.000000000
C4	0.281280518	0.29309082	-0.06055069	0.019245148	-0.010158539
C5	0.000000000	0.499969482	0.000000000	0.000000000	0.000000000
C6	- 0.031303406	0.29309082	0.299453735	-0.069904327	0.03055191
C7		0.000000000	0.499954224	0.000000000	0.000000000
C8		-0.049036026	0.299453735	0.304092407	-0.081981659
C9		0.000000000	0.000000000	0.500000000	0.000000000
C10		0.005929947	-0.06055069	0.304092407	0.309417725
C11			0.000000000	0.000000000	0.500000000
C12			0.012379646	-0.069904327	0.309417725
C13			0.000000000	0.000000000	0.000000000
C14			-0.00130558	0.019245148	-0.081981659
C15				0.000000000	0.000000000
C16				-0.003810883	0.03055191
C17				0.000000000	0.000000000
C18				0.000378609	-0.010158539
C19					0.000000000
C20					0.00251317
C21					0.000000000
C22					-0.000347137

NOTE: While Halfband filters are typically selected starting with the last stage in the filter chain to give the maximum alias free bandwidth, a higher throughput rate may be obtained using other filter combinations. See Application Note 9720, "Calculating Maximum Processing Rates of the PDC".

Depending on the number of halfbands used, PROCCLK must operate at a minimum rate above the input sample rate, f_S, to the halfband. This relationship depends on the number of multiplies for each of the halfband filter stages. The filter calculations take 3, 4, 5, 6, and 7 multiplies per input for HB1, HB2, HB3, HB4, and HB5 respectively. If we keep the assumption that f_S is the input sampling frequency, then Equation 10 shows the minimum ratio needed.

$$f_{PROCCLK}/f_S \geq ([(7)(HB5)(2^{HB5})+ (6)(HB4)(2^{(HB4 + HB5)})+ (5)(HB3)(2^{(HB3+HB4+HB5)})+ (4)(HB2)(2^{(HB2+HB3+ HB4+HB5)})+ (3)(HB1)(2^{(HB1+HB2+HB3+HB4+HB5)})]/2^T \quad \text{(EQ. 10)}$$

where

HB1 = 1 if this section is selected and 0 if it is bypassed;
HB2 = 1 if this section is selected and 0 if it is bypassed;
HB3 = 1 if this section is selected and 0 if it is bypassed;
HB4 = 1 if this section is selected and 0 if it is bypassed;
HB5 = 1 if this section is selected and 0 if it is bypassed;
T = number of Halfband Filters Selected. The range for T is from 0 to 5.

Examples of PROCCLK Rate Calculations

Suppose we enable HB1, HB3, and HB5. Using Figure 16, HB1= 1, HB3 = 1, and HB5 = 1. Since stage 2 and stage 4 are not used, HB2 and HB4 = 0. PROCCLK must operate faster than (7x2+5x4+3x8)/8 = 7.25 times faster than f_S.

If all five halfbands are used, then PROCCLK must operate at (7x2+6x4+5x8+4x16+3x32)/32 = 7.4375 times faster than f_S.

255-Tap Programmable FIR Filter

The Programmable FIR filter can be used to implement real filters with even or odd symmetry, using up to 255 filter taps, or complex filters with up to 64 taps. The FIR filter takes advantage of symmetry in coefficients by summing data samples that share a common coefficient, prior to multiplication. In this manner, two filter taps are calculated per multiply accumulate cycle. Asymmetric filters cannot share common coefficients, so only one tap per multiply accumulate cycle is calculated. The filter can be effectively bypassed by setting the coefficient $C_0 = 1$ and all other coefficients, $C_N = 0$.

Additionally, the Programmable FIR filter provides for decimation factors, R, from 1 to 16. The processing rate of the Filter Compute Engine is PROCCLK. As a result, the frequency of PROCCLK must exceed a minimum value to ensure that a filter calculation is complete before the result is required for output. In configurations which do not use decimation, one input sample period is available for filter calculation before an output is required. For configurations which employ decimation, up to 16 input sample periods may be available for filter calculation.

For real filter configurations, use Equations 11A and 11B to calculate the number of taps available at a given input filter sample rate.

$$TAPS = (floor[PROCCLK/(F_{SAMP}/R) - R])(1 + SYM) - [(SYM)(ODD\#)] \quad \text{(EQ. 11A)}$$

for real filters, and

$$TAPS = floor[(PROCCLK/(F_{SAMP}/R) - R)/2] \quad \text{(EQ. 11B)}$$

for complex filters, where floor is defined as the integer portion of a number; PROCCLK is the compute clock; f_{SAMP} = the FIR input sample rate; R = Decimation Factor; SYM = 1 for symmetrical filter, 0 for asymmetrical filter; ODD# = 1 for an odd number of filter taps, 0 = an even number of taps.

Use Equation 12A to calculate the maximum input rate.

$$F_{SAMP} = (PROCCLK)\ (R)/[R + [floor[(Taps) + (SYM)(ODD\#)]/(1 + SYM)]] \quad \text{(EQ. 12A)}$$

for real filters, and

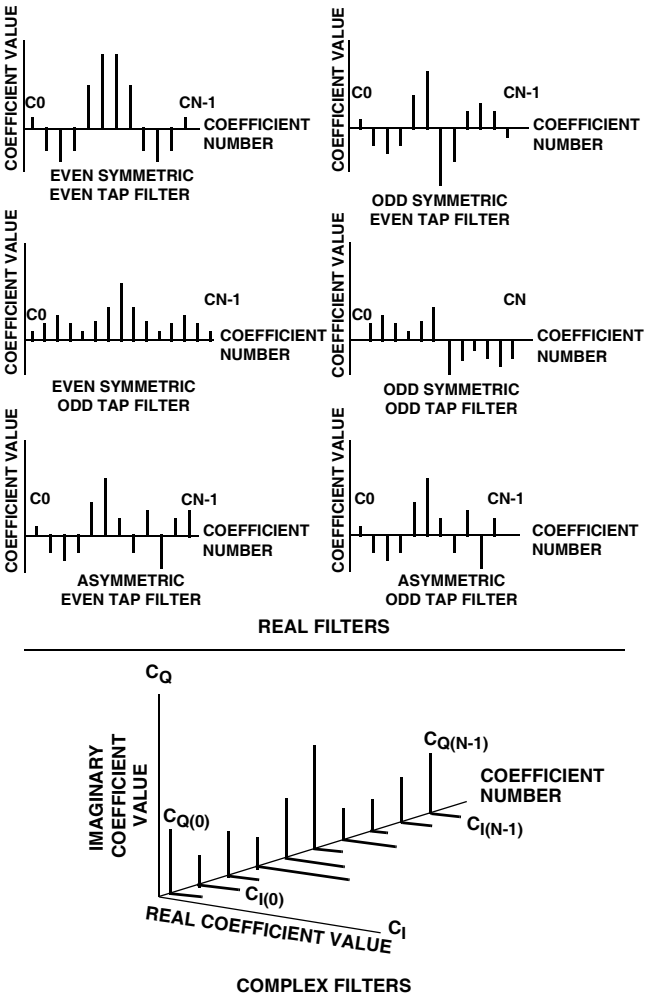
$$F_{SAMP} = [(PROCCLK)(R)]/[R + floor[(Taps)(2)]] \quad \text{(EQ. 12B)}$$

for complex filters, where floor[x], PROCCLK, f_{SAMP}, R = Decimation Factor, SYM, and ODD# are defined as in Equation 11A.

Use Equation 13 to calculate the maximum output sample rate for both real and complex filters.

$$F_{FIROUT} = (F_{SAMP})/R \quad \text{(EQ. 13)}$$

The coefficients are 22-bits and are loaded using writes to Control Words 128 through 255 (see Microprocessor Write Section). For real filters, the same coefficients are used by I and Q paths. If the filter is configured as a symmetric filter using Control Word 17, Bit 9, then coefficients are loaded starting with the center coefficient in Control Word 128 and proceeding to last coefficient in Control Word 128+n. The filter symmetry type can be set to even or odd symmetric, and the number of filter coefficients can be even or odd, as illustrated in Figure 20. Note that complex filters can also be realized but are only allowed to be asymmetric. Only the coefficients that are used need to be loaded.



Definitions:

Even Symmetric: h(n) = h(N-n-1) for n = 0 to N-1

Odd Symmetric: h(n) = -h(N-n-1) for n = 0 to N-1

Asymmetric: A filter with no coefficient symmetry.

Even Tap filter: A filter where N is an even number.

Odd Tap filter: A filter where N is an odd number.

Real Filter: A filter implemented with real coefficients.

Complex Filters: A filter with quadrature coefficients.

FIGURE 20. DEMONSTRATION OF DIFFERENT TYPES OF DIGITAL FIR FILTERS CONFIGURED IN THE PROGRAMMABLE DOWNCONVERTER

Automatic Gain Control (AGC)

The AGC Section provides gain to small signals, after the large signals and out-of-band noise have been filtered out, to ensure that small signals have sufficient bit resolution in the Resampling/Interpolating Halfband filters and the Output Formatter. The AGC can also be used to manually set the gain. The AGC optimizes the bit resolution for a variety of input amplitude signal levels. The AGC loop automatically adds gain to bring small signals from the lower bits of the 26-bit programmable FIR filter output into the 16-bit range of the

output section. Without gain control, a signal at -72dBFS = $20\log_{10}(2^{-12})$ at the input would have only 4-bits of resolution at the output (12-bits less than the full scale 16-bits). The potential increase in the bit resolution due to processing gain of the filters can be lost without the use of the AGC.

Figure 23 shows the Block Diagram for the AGC Section. The FIR filter data output is routed to the Resampling and Halfband filters after passing through the AGC multipliers and Shift Registers. The outputs of the Interpolating Halfband filters are routed to the Cartesian to Polar coordinate converter. The magnitude output of the coordinate converter is routed through the AGC error detector, the AGC error scaler and into the AGC loop filter. This filtered error term is used to drive the AGC multiplier and shifters, completing the AGC control loop.

The AGC Multiplier/Shifter portion of the AGC is identified in Figure 23. The gain control from the AGC loop filter is sampled when new data enters the Multiplier/Shifter. The limit detector detects overflow in the shifter or the multiplier and saturates the output of I and Q data paths independently. The shifter has a gain from 0 to 90.31dB in 6.021dB steps, where $90.31\text{dB} = 20\log_{10}(2^N)$, when N = 15. The mantissa provides an additional 6dB of gain in 0.0338dB steps where $6.0204\text{dB} = 20\log_{10}[1+(X)2^{-15}]$, where $X = 2^{15}-1$. Thus, the AGC multiplier/shifter transfer function is expressed as:

$$\text{AGC Mult/Shift Gain} = 2^N[1+(X)2^{-15}], \quad \text{(EQ. 14)}$$

where N, the shifter exponent, has a range of $0<N<15$ and X, the mantissa, has a range of $0<X<(2^{15}-1)$.

Equation 14 can be expressed in dB,

$$(\text{AGC Mult/Shift Gain})\text{dB} = 20\log_{10}(2^N[1+(X)2^{-15}]) \quad \text{(EQ. 14A)}$$

The full AGC range of the Multiplier/Shifter is from 0 to 96.331dB ($20\log_{10}[1+(2^{15}-1)2^{-15}] + 20\log_{10}[2^{15}] = 96.331$). Figure 21 illustrates the transfer function of the AGC multiplier versus mantissa control for N = 0. Figure 22 illustrates the complete AGC Multiplier/Shifter Transfer function for all values of exponent and mantissa control.

The resolution of the mantissa was increased to 16-bits in the A Version, to provide a theoretical AM modulation level of -96dBc (depending on loop gain, settling mode and SNR). This effectively eliminates AM spurious caused by the AGC resolution.

For fixed gains, either set the upper and lower AGC limits to the same value, or set the limits to minimum and maximum gains and set the AGC loop gain to zero.

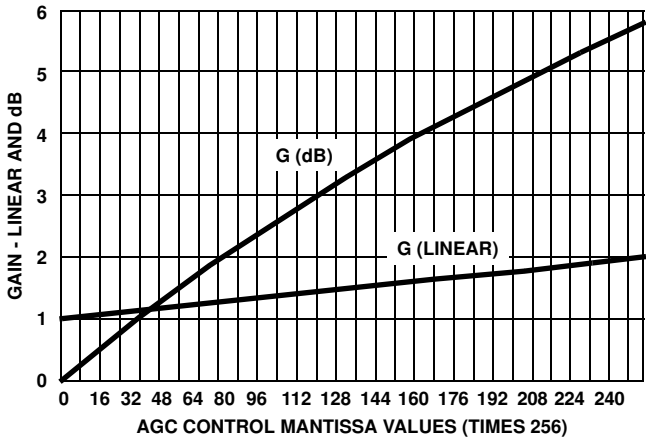


FIGURE 21. AGC MULTIPLIER LINEAR AND dB TRANSFER FUNCTION

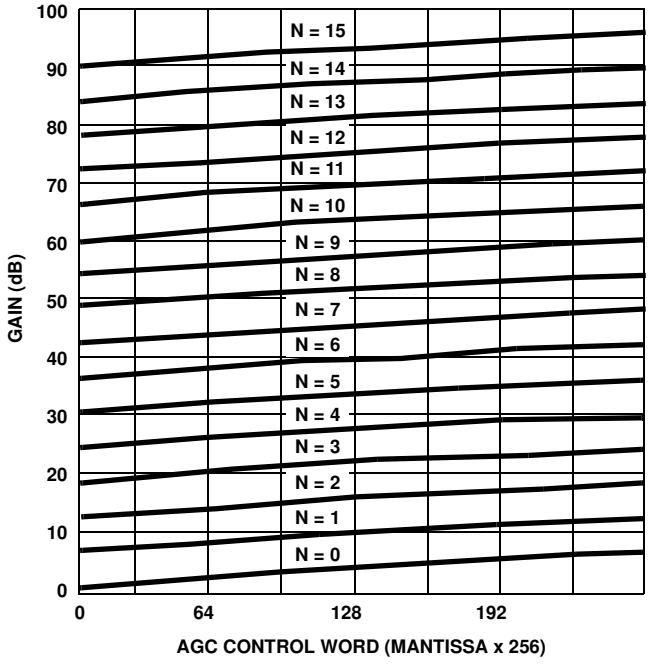


FIGURE 22. AGC GAIN CONTROL TRANSFER FUNCTION

The Cartesian to Polar Coordinate converter accepts I and Q data and generates magnitude and phase data. The magnitude output is determined by the Equation 15:

$$|r| = 1.64676\sqrt{I^2+Q^2}. \quad \text{(EQ. 15)}$$

where the magnitude limits are determined by the maximum I and Q signal levels into the Cartesian to Polar converter. Taking fractional 2's complement representation, magnitude ranges from 0 to 2.329, where the maximum output is

$$|r| = 1.64676\sqrt{(1.0)^2+(1.0)^2} = 1.64676 \times 1.414 = 2.329 \cdot$$

The AGC loop feedback path consists of an error detector, error scaling, and an AGC loop filter. The error detector subtracts the magnitude output of the coordinate converter from the programmable AGC THRESHOLD value. The bit weighting of

the AGC THRESHOLD value (Control Word 8, Bits 16-28) is shown in Table 5. Note that the MSB is always zero. The range of the AGC THRESHOLD value is 0 to +3.9995. The AGC Error Detector output has the identical range.

TABLE 5. AGC THRESHOLD (CONTROL WORD 8) BIT WEIGHTING

28	27	26	25	24	23	22	21	20	19	18	17	16
2^2	2^1	2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

The loop gain is set in the AGC Error Scaling circuitry, using the two programmable mantissas and exponents. The mantissa, M, is a 4-bit value which weights the loop filter input from 0.0 to 0.9375. The exponent, E, defines a shift factor that provides additional weighting from 2^0 to 2^{-15}. Together the mantissa and exponent define the loop gain as given by,

$$\text{AGC Loop Gain} = M_{LG}2^{-4}\ 2^{-(15-E_{LG})} \quad \text{(EQ. 16)}$$

where M_{LG} is a 4-bit binary value ranging from 0 to 15, and E_{LG} is a 4-bit binary value ranging from 0 to 15. Table 7 and 8 detail the binary values and the resulting scaling effects of the AGC scaling mantissa and exponent. The composite (shifter and multiplier) AGC scaling Gain range is from 0.0000 to $2.329(0.9375)2^0$ = 0.0000 to 2.18344. The scaled gain error can range (depending on threshold) from 0 to 2.18344, which maps to a “gain change per sample” range of 0 to 3.275dB/sample.

The AGC Gain mantissa and exponent values are programmed into Control Word 8, Bits 0-15. The PDC provides for the storing of two values of AGC Scaling Gain (both exponent and mantissa). This allows for quick adjustment of the loop gain by simply asserting the external control line AGCGNSEL. When AGCGNSEL = 0, then AGC GAIN 0 is selected, and when AGCGNSEL = 1, AGC Loop Gain 1 is selected. Possible applications include acquisition/tracking, no burst present/burst present, strong signal/weak signal, track/hold, or fast/slow AGC values.

The AGC loop filter consists of an accumulator with a built in limiting function. The maximum and minimum AGC gain limits are provided to keep the gain within a specified range and are programed by 12-bit Control Words using Equation 17:

$$\text{AGC Gain Limit} = (1 + m_{AGC}2^{-9})2^e \quad \text{(EQ. 17)}$$

$$(\text{AGC Gain Limit})\text{dB} = (6.02)(\text{eeee}) + 20\log(1.0 + 0.\text{mmmmmmmm}) \quad \text{(EQ. 17A)}$$

where m is an 8-bit mantissa value between 0 and 255, and e is the 4-bit exponent ranging from 0 to 15. Control Word 9, Bits 16-27 are used for programming the upper limit, while bits 0-11 are used to program the lower threshold. The ranges and format for these limit values are shown in Tables 6A through 6C. The bit weightings for the AGC Loop Feedback elements are detailed in Table 9A.

TABLE 6A. AGC LIMIT EXPONENT vs GAIN

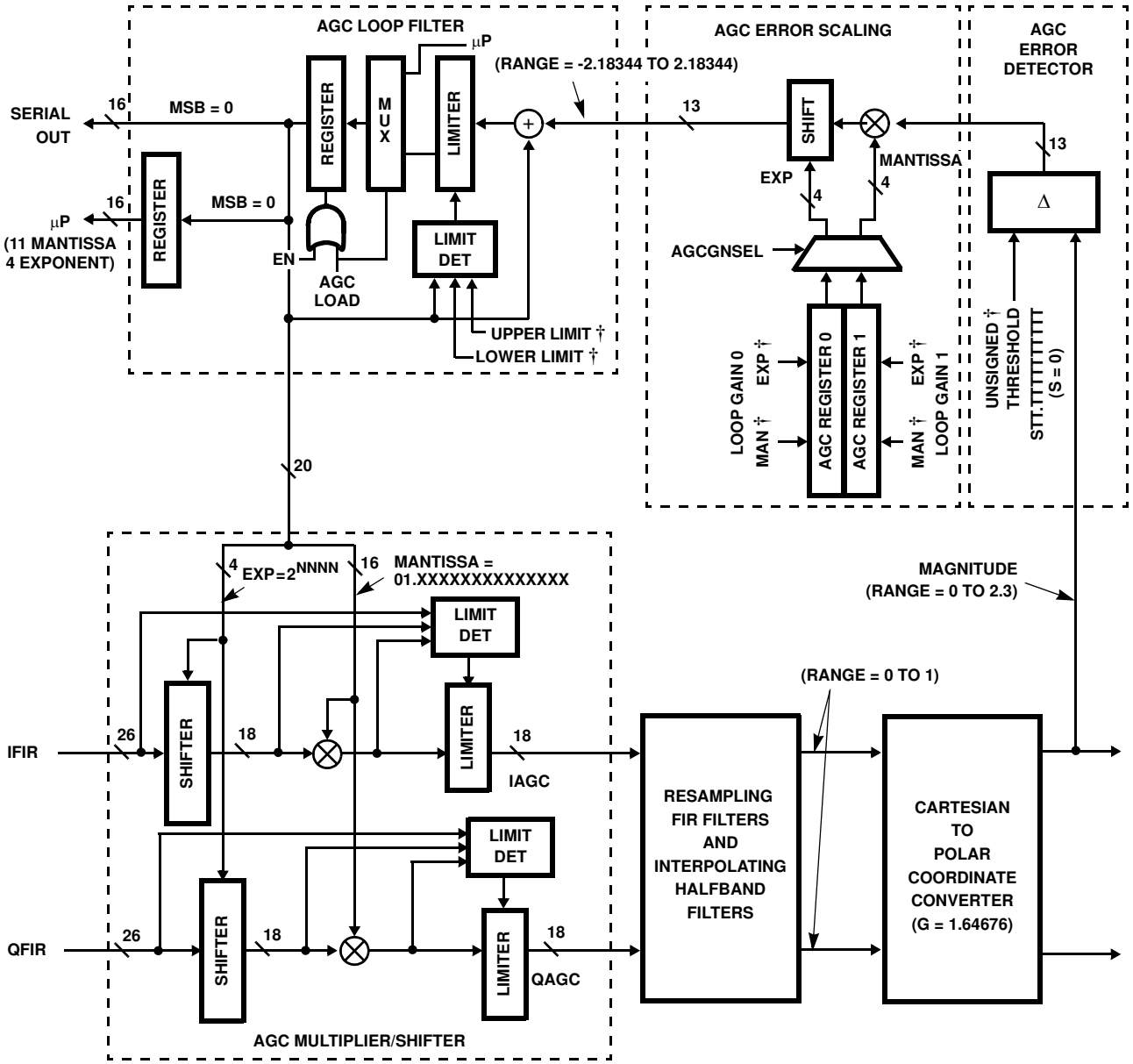
GAIN(dB)	EXPONENT	MANTISSA
96.332	15	255
90.309	15	0
84.288	14	0
78.268	13	0
72.247	12	0
66.227	11	0
60.206	10	0
54.185	9	0
48.165	8	0
42.144	7	0
36.124	6	0
30.103	5	0
24.082	4	0
18.062	3	0
12.041	2	0
6.021	1	0
0.000	0	0

TABLE 6B. AGC LIMIT MANTISSA vs GAIN

GAIN(dB)	EXPONENT	MANTISSA
6.000	0	255
5.750	0	240
5.500	0	226
5.250	0	212
5.000	0	199
4.750	0	185
4.500	0	173
4.250	0	161
4.000	0	149
3.750	0	138
3.500	0	127
3.250	0	116
3.000	0	105
2.750	0	95
2.500	0	85
2.250	0	75
2.000	0	66
1.750	0	57
1.500	0	48
1.250	0	39
1.000	0	31
0.750	0	23
0.500	0	15
0.250	0	7
0.020	0	1

TABLE 6C. AGC LIMIT DATA FORMAT

CONTROL WORD 9 BIT:	27	26	25	24	23	22	21	20	19	18	17	16
FORMAT	e	e	e	e	m	m	m	m	m	m	m	m



† Controlled via microprocessor interface.

FIGURE 23. AGC BLOCK DIAGRAM

Using AGC loop gain, the AGC range, and expected error detector output, the gain adjustments per output sample for the Loop Filter Section of the Digital AGC can be given by:

$$\text{AGC Slew Rate} = 1.5\text{dB}(\text{THRESH} - (\text{MAG}*1.64676)) \times (M_{LG})(2^{-4})\left(2^{-(15-E_{LG})}\right) \quad \text{(EQ. 18)}$$

The loop gain determines the growth rate of the sum in the loop accumulator which, in turn, determines how quickly the AGC gain traces the transfer function given in Figures 21 and 22. Since the log of the gain response is roughly linear, the loop response can be approximated by multiplying the maximum AGC gain error by the loop gain. The expected

range for the AGC rate is ~ 0.000106 to 3.275dB/output sample time for a threshold of 1/2 scale. See the notes at the bottom of Table 9A for calculation of the AGC response times. The maximum AGC Response is given by:

$$\text{AGC Response}_{Max} = \text{Input(Cart/Polar Gain)(Error Det Gain)(AGC Loop Gain)(AGC Output Weighting)} \quad \text{(EQ. 19)}$$

Since the AGC error is scaled to adjust the gain, the loop settles asymptotically to its final value. The loop settles to the mean of the signal.

TABLE 7. AGC LOOP GAIN BINARY MANTISSA TO GAIN SCALE FACTOR MAPPING

BINARY CODE (MMMM)	SCALE FACTOR	BINARY CODE (MMMM)	SCALE FACTOR
0000	0.0000	1000	0.5000
0001	0.0625	1001	0.5625
0010	0.1250	1010	0.6250
0011	0.1875	1011	0.6875
0100	0.2500	1100	0.7500
0101	0.3125	1101	0.8125
0110	0.3750	1110	0.8750
0111	0.4375	1111	0.9375

TABLE 8. AGC LOOP GAIN BINARY EXPONENT TO GAIN SCALE FACTOR MAPPING

BINARY CODE (EEEE)	SCALE FACTOR	BINARY CODE (EEEE)	SCALE FACTOR
0000	2^{15}	1000	2^{7}
0001	2^{14}	1001	2^{6}
0010	2^{13}	1010	2^{5}
0011	2^{12}	1011	2^{4}
0100	2^{11}	1100	2^{3}
0101	2^{10-}	1101	2^{2}
0110	2^{9}	1110	2^{1}
0111	2^{8}	1111	2^{0}

For example, if M_{LG} = 0101 and E_{LG} = 1100, the AGC Loop Gain = $0.3125*2^{-7}$. The loop gain mantissas and exponents are set in the AGC Loop Parameter Control Register (Control Word 8, Bits 0-15).

Two AGC loop gains are provided in the Programmable Down Converter, for quick adjustment of the AGC loop. The AGC Gain select is a control input to the device, selecting Gain 0 when AGCGNSEL = 0, and selecting Gain 1 when AGCGNSEL = 1.

In the HSP50214, a reset event (caused by SYNCIN2 or CW25) would clear the AGC loop filter accumulator. In the HSP50214B, if Control Word 27, Bit 15 is set to zero, the AGC loop filter accumulator will clear as in the original HSP50214. If Control Word 27, Bit 15 is set to a one, the backend reset (from CW25) will not clear the AGC loop filter accumulator.

In the HSP50214, the settling mode of the AGC forces the mean of the signal magnitude error to zero. The gain error is scaled and used to adjust the gain up or down. This proportional scaling mode causes the AGC to settle to the final gain value asymptotically. This AGC settling mode is preferred in many applications because the loop gain adjustments get smaller and smaller as the loop settles, reducing any AM distortion caused by the AGC.

With this AGC settling mode, the proportional gain error causes the loop to settle more slowly if the threshold is small. This is because the maximum value of the threshold minus the magnitude is smaller. Also, the settling can be asymmetric, where the loop may settle faster for “over range” signals than for “under range” signals (or vice versa).

In some applications, such as burst signals or TDMA signals, a very fast settling time and/or a more predictable settling time is desired. The AGC may be turned off or slowed down after an initial AGC settling period.

To minimize the settling time, a median AGC settling mode has been added to the HSP50214B. This mode uses a fixed gain adjustment with only the direction of the adjustment controlled by the gain error. This makes the settling time independent of the signal level.

For example, if the loop is set to adjust 0.5dB per output sample, the loop gain can slew up or down by 16dB in 16 symbol times, assuming a 2 samples per symbol output sample rate. This is called a median settling mode because the loop settles to where there is an equal number of magnitude samples above and below the threshold. The disadvantage of this mode is that the loop will have a wander (dither) equal to the programmed step size. For this reason, it is advisable to set one loop gain for fast settling at the beginning of the burst and the second loop gain for small adjustments during tracking.

The median settling mode is enabled by setting Control Word 27, Bit 16 to a logic one. If Control Word 27, Bit 16 is zero, the mean loop settling mode is selected and the loop works identically to the HSP50214.

In the median mode, the loop works as follows:

The sign of the true gain error selects a fixed gain error of 0010000000000_b or 1110000000000_b.

These gain error values are scaled by the programmable AGC loop gains to adjust the data path gain.

The maximum slew rate is ~1.5dB per output sample. See Equation 18.

In order to fully evaluate the dynamic range of the PDC, Table 9B is provided, which details the bit weighting from the input to the AGC Multiplier.

Re-Sampler/Halfband Filter

The re-sampler is an NCO controlled polyphase filter that allows the output sample rate to have a non-integer relationship to the input sample rate. The filter engine can be viewed conceptually as a fixed interpolation filter, followed by an NCO controlled decimator.

The prototype polyphase filter has 192 taps designed at 32 times the input sample rate. Each of the 32 phases has 6 filter taps (6)(32) = 192. The stopband attenuation of the prototype filter is greater than 60dB, as shown in Figure 24. The signal to total image power ratio is approximately 55dB, due to the aliasing of the interpolation images. The filter is capable of decimation factors from 1 to 4. If the output is at least 2x the baud rate, the 32 interpolation phases yield an effective sample rate of 64x the baud rate or approximately 1.5%, (1/64), maximum timing error.

Following the Re-sampler are two interpolation halfband filters. The halfband filters allow the user to up-sample by 2 or 4 to recover time resolution lost by decimating. Interpolating by 2 or 4 gives 1/4 or 1/8 baud time resolution (assuming 2x baud at the re-sampler output). The halfband filters use the same coefficients as HB3 and HB5 from the Halfband Filters Section. If one halfband is used, the 23-tap filter is chosen. If two are used, the 23-tap filter runs first followed by the 15-tap filter operating at twice the first halfband's rate. The 23-tap filter requires 7 multiplies, and the 15-tap filter requires 5 multiplies to complete a filter calculation.

Using the interpolation halfband filters allows for reduction in the FIR filter sample rate. This optimizes the use of the programmable FIR filter by allowing the FIR output sample rate to be closer to the Nyquist rate of the desired bandwidth. Optimizing the FIR filter performance provides better use of the programmable FIR taps. Table 10 details the maximum clocking rates for the possible resampling and interpolation halfband filter configurations of this section of the PDC. Control Word 16, Bits 2-0 identify the filter configuration. Control Word 16, Bit 3 is used to bypass the polyphase re-sampler filter.

For proper data output from the interpolation filters, the data ready signal must account for the interpolation process. Figure 25 illustrates the insertion of additional data ready pulses to provide sufficient pulses for the new output sample rate. The Re-sampler Output Pulse Delay parameter is set in Control Word 16, Bits 4-11. These bits set the delay between the output samples when interpolation is utilized. Program this distance between pulses using

$$N = [(f_{PROCCLK}/f_{OUT}) - 1] \quad \text{(EQ. 20)}$$

A value of at least 5 is required to have sufficient time to update the Output Buffer Register. (Writing 5 samples requires 5 clock cycles) A value of at least 16 is required for proper serial output from the part. (Conversion from 16-bit parallel to serial). The value is programmed in numbers of PROCCLK's.

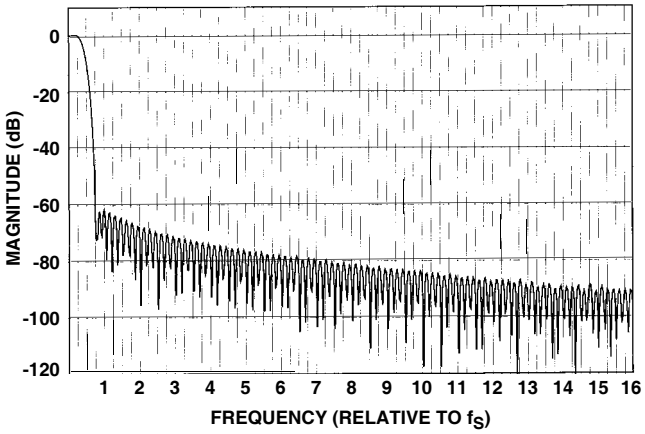


FIGURE 24A. POLYPHASE RESAMPLER FILTER BROADBAND FREQUENCY RESPONSE

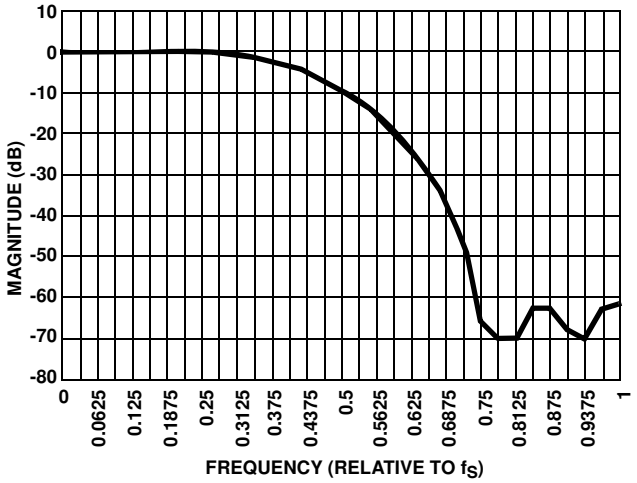


FIGURE 24B. POLYPHASE RESAMPLER FILTER PASS BAND FREQUENCY RESPONSE

There is a 65dB limitation in SNR using the Re-Sampler Filter. When only the Interpolation FIRs are used, the full SNR range is passed.

FIGURE 24.