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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Four-Channel Programmable Digital Downconverter

The HSP50216 Quad Programmable Digital Downconverter (QPDC) is designed for high dynamic range applications such as cellular basestations where multiple channel processing is required in a small physical space. The QPDC combines into a single package, a set of four channels which include: digital mixers, a quadrature carrier NCO, digital filters, a resampling filter, a Cartesian-to-polar coordinate converter and an AGC loop.

The HSP50216 accepts four channels of 16-bit real digitized IF samples which are mixed with local quadrature sinusoids. Each channel carrier NCO frequency is set independently by the microprocessor. The output of the mixers are filtered with a CIC and FIR filters, with a variety of decimation options. Gain adjustment is provided on the filtered signal. The digital AGC provides a gain adjust range of up to 96dB with programmable thresholds and slew rates. A cartesian to polar coordinate converter provides magnitude and phase outputs. A frequency discriminator provides a frequency output via the FIR filter. Selectable outputs include I samples, Q samples, Magnitude, Phase, Frequency and AGC gain. The output resolution is selectable from 4-bit fixed point to 32-bit floating point.

The maximum output bandwidth achievable using a single channel is at least 1MHz.

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
HSP50216KIZ (Note)	HSP50216KIZ	-40 to +85	196 Ld BGA (Pb-free)	V196.12x12

NOTE: These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

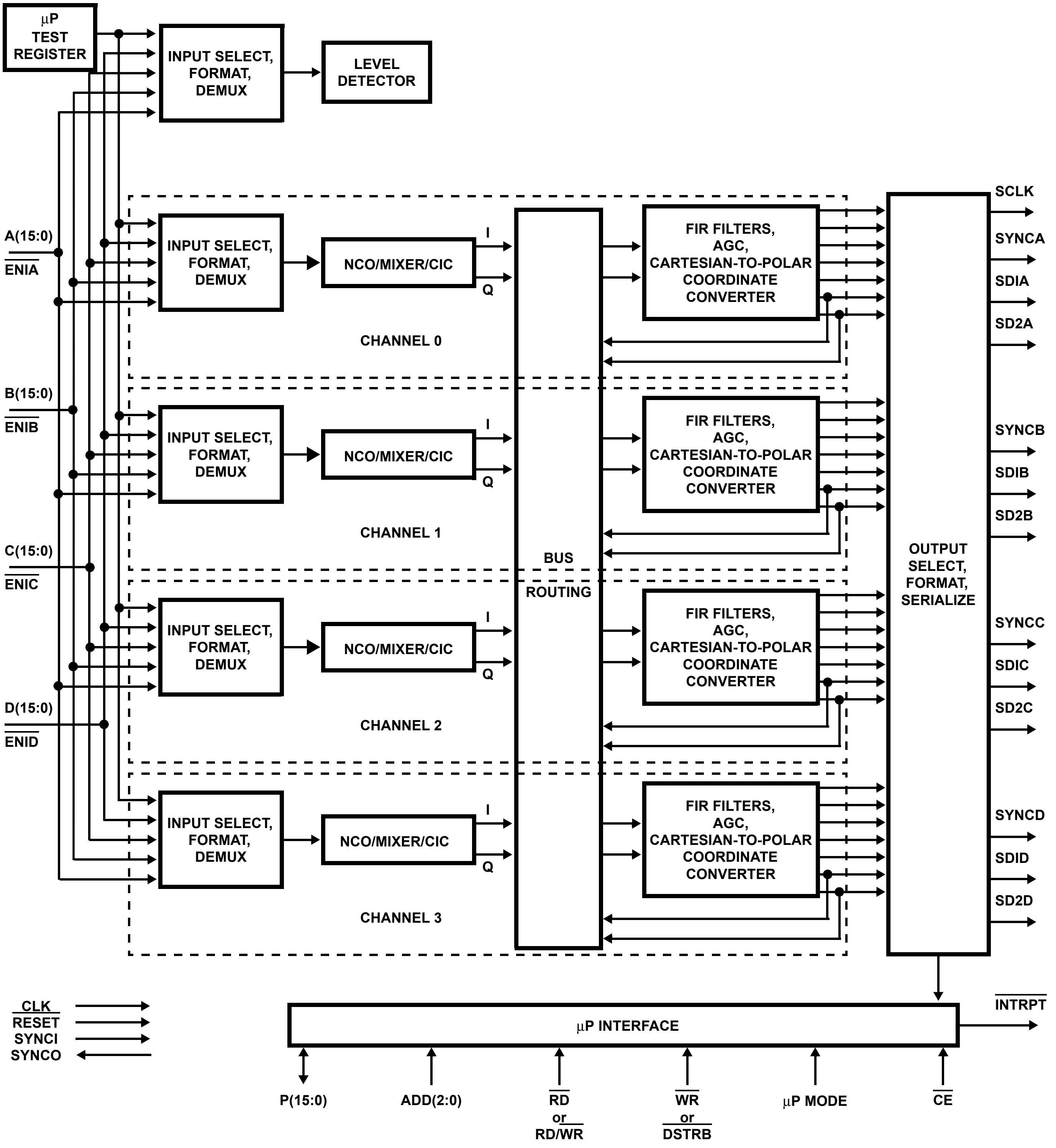
- Up to 70MSPS Input
- Four Independently Programmable Downconverter Channels in a single package
- Four Parallel 16-Bit Inputs - Fixed or Floating Point Format
- 32-Bit Programmable Carrier NCO with >115dB SFDR
- 110dB FIR Out of Band Attenuation
- Decimation from 8 to >65536
- 24-bit Internal Data Path
- Digital AGC with up to 96dB of Gain Range
- Filter Functions
  - 1 to 5 Stage CIC Filter
  - Halfband Decimation and Interpolation FIR Filter
  - Programmable FIR Filter
  - Resampling FIR Filter
- Cascadable Filtering for Additional Bandwidth
- Four Independent Serial Outputs
- 3.3V Operation
- Pb-Free Available (RoHS Compliant)

Applications

- Narrow-Band TDMA through IS-95 CDMA Digital Software Radio and Basestation Receivers
- Wide-Band Applications: W-CDMA and UMTS Digital Software Radio and Basestation Receivers

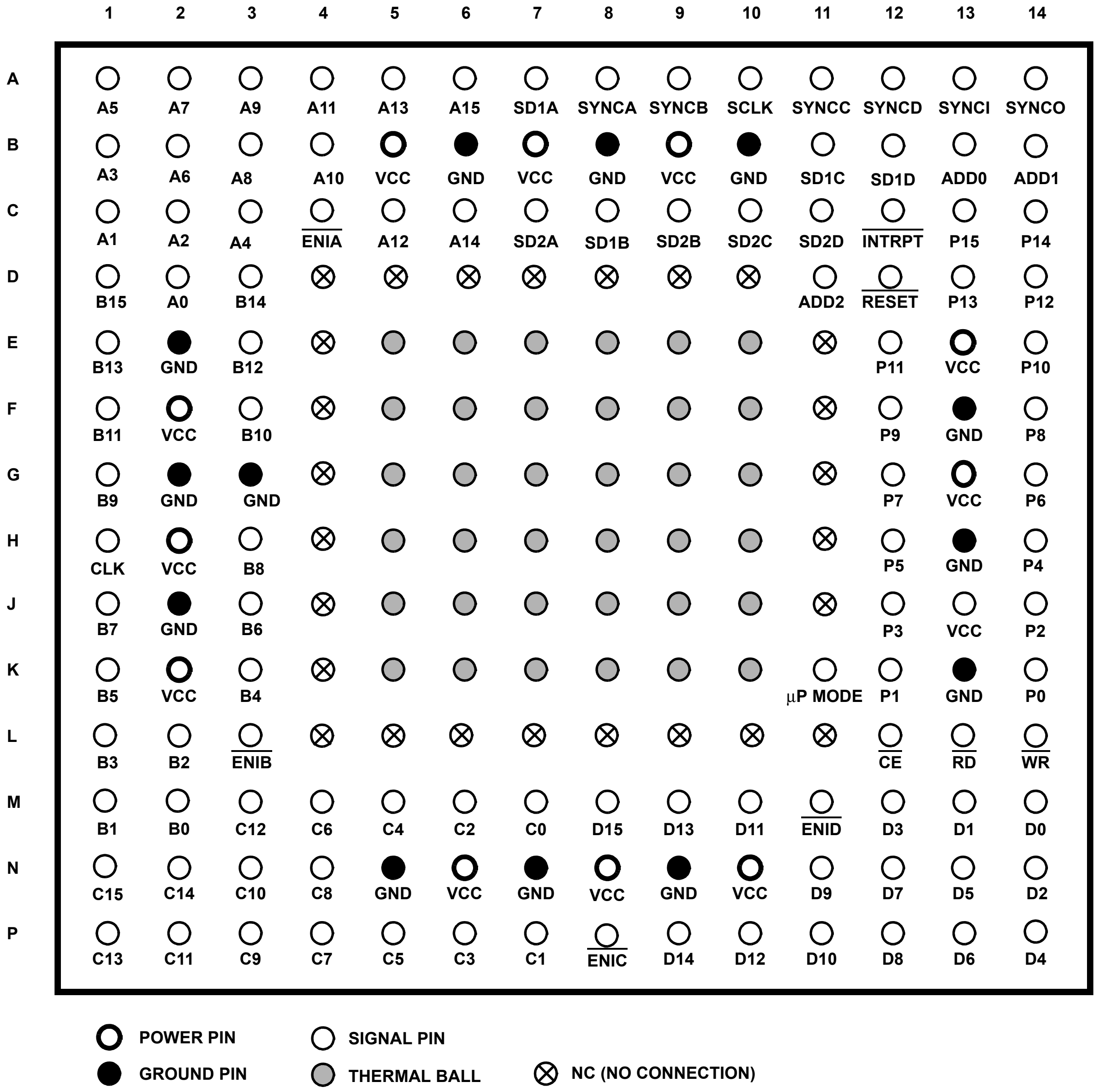
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.

Block Diagram



Pinout

196 LD BGA
TOP VIEW



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	A5	A7	A9	A11	A13	A15	SD1A	SYNCA	SYNCB	SCLK	SYNCC	SYNCD	SYNCI	SYNCO
B	A3	A6	A8	A10	VCC	GND	VCC	GND	VCC	GND	SD1C	SD1D	ADD0	ADD1
C	A1	A2	A4	$\overline{ENIA}$	A12	A14	SD2A	SD1B	SD2B	SD2C	SD2D	$\overline{INTRPT}$	P15	P14
D	B15	A0	B14	⊗	⊗	⊗	⊗	⊗	⊗	⊗	ADD2	$\overline{RESET}$	P13	P12
E	B13	GND	B12	⊗	◍	◍	◍	◍	◍	◍	⊗	P11	VCC	P10
F	B11	VCC	B10	⊗	◍	◍	◍	◍	◍	◍	⊗	P9	GND	P8
G	B9	GND	GND	⊗	◍	◍	◍	◍	◍	◍	⊗	P7	VCC	P6
H	CLK	VCC	B8	⊗	◍	◍	◍	◍	◍	◍	⊗	P5	GND	P4
J	B7	GND	B6	⊗	◍	◍	◍	◍	◍	◍	⊗	P3	VCC	P2
K	B5	VCC	B4	⊗	◍	◍	◍	◍	◍	◍	µP MODE	P1	GND	P0
L	B3	B2	$\overline{ENIB}$	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	$\overline{CE}$	$\overline{RD}$	$\overline{WR}$
M	B1	B0	C12	C6	C4	C2	C0	D15	D13	D11	$\overline{ENID}$	D3	D1	D0
N	C15	C14	C10	C8	GND	VCC	GND	VCC	GND	VCC	D9	D7	D5	D2
P	C13	C11	C9	C7	C5	C3	C1	$\overline{ENIC}$	D14	D12	D10	D8	D6	D4

◯ POWER PIN
● GROUND PIN
○ SIGNAL PIN
◍ THERMAL BALL
⊗ NC (NO CONNECTION)

Pin Descriptions

NAME	TYPE	DESCRIPTION
POWER SUPPLY		
VCC	-	Positive Power Supply Voltage, 3.3V ±0.15
GND	-	Ground, 0V.
INPUTS		
A(15:0)	I	Parallel Data Input bus A. Sampled on the rising edge of clock when $\overline{\text{ENIA}}$ is active (low).
B(15:0)	I	Parallel Data Input bus B. Sampled on the rising edge of clock when $\overline{\text{ENIB}}$ is active (low).
C(15:0)	I	Parallel Data Input bus C. Sampled on the rising edge of clock when $\overline{\text{ENIC}}$ is active (low).
D15	I	Parallel Data Input D15 or tuner channel A COF.
D14	I	Parallel Data Input D14 or tuner channel A COFSync.
D13	I	Parallel Data Input D13 or tuner channel A SOF.
D12	I	Parallel Data Input D12 or tuner channel A SOFSync.
D11	I	Parallel Data Input D11 or tuner channel B COF.
D10	I	Parallel Data Input D10 or tuner channel B COFSync.
D9	I	Parallel Data Input D9 or tuner channel B SOF.
D8	I	Parallel Data Input D8 or tuner channel B SOFSync.
D7	I	Parallel Data Input D7 or tuner channel C COF.
D6	I	Parallel Data Input D6 or tuner channel C COFSync.
D5	I	Parallel Data Input D5 or tuner channel C SOF.
D4	I	Parallel Data Input D4 or tuner channel C SOFSync.
D3	I	Parallel Data Input D3 or tuner channel D COF.
D2	I	Parallel Data Input D2 or tuner channel D COFSync.
D1	I	Parallel Data Input D1 or tuner channel D SOF.
D0	I	Parallel Data Input D0 or tuner channel D SOFSync.
$\overline{\text{ENIA}}$	I	Input enable for Parallel Data Input bus A. Active low. This pin enables the input $\overline{\text{to the}}$ part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
$\overline{\text{ENIB}}$	I	Input enable for Parallel Data Input bus B. Active low. This pin enables the input $\overline{\text{to the}}$ part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
$\overline{\text{ENIC}}$	I	Input enable for Parallel Data Input bus C. Active low. This pin enables the input $\overline{\text{to the}}$ part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
$\overline{\text{ENID}}$	I	Input enable for Parallel Data Input bus D. Active low. This pin enables the input $\overline{\text{to the}}$ part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
CONTROL		
CLK	I	Input clock. All processing in the HSP50216 occurs on the rising edge of CLK.
SYNCI	I	Synchronization Input Signal. Used to align the processing with an external event or with other HSP50216 devices. SYNCI can update the carrier NCO, reset decimation counters, restart the filter compute engine, and restart the output section among other functions. For most of the functional blocks, the response to SYNCI is programmable and can be enabled or disabled.
SYNCO	O	Synchronization Output Signal. The processing of multiple HSP50216 devices can be synchronized by tying the SYNCO from one HSP50216 device (the master) to the SYNCI of all the HSP50216 devices (the master and slaves).
$\overline{\text{RESET}}$	I	Reset Signal. Active low. Asserting reset will halt all processing and set certain registers to default values.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
OUTPUTS		
SD1A	O	Serial Data Output 1A. A serial data stream output which can be programmed to consist of I1, Q1, I2, Q2, magnitude, phase, frequency (dϕ/dt), AGC gain, and/or zeros. In addition, data outputs from Channels 0, 1, 2 and 3 can be multiplexed into a common serial output data stream. Information can be sequenced in a programmable order. *See Serial Data Output Formatter Section.*
SD2A	O	Serial Data Output 2A. This output is provided as an auxiliary output for Serial Data Output 1A to route data to a second destination or to output two words at a time for higher sample rates. SD2A has the same programmability as SD1A except that floating point format is not available. *See Serial Data Output Formatter Section* and *Microprocessor Interface* section.
SD1B	O	Serial Data Output 1B. See description for SD1A.
SD2B	O	Serial Data Output 2B. See description for SD2A.
SD1C	O	Serial Data Output 1C. See description for SD1A.
SD2C	O	Serial Data Output 2C. See description for SD2A.
SD1D	O	Serial Data Output 1D. See description for SD1A.
SD2D	O	Serial Data Output 2D. See description for SD2A.
SCLK	O	Serial Output Clock. Can be programmed to be at 1, 1/2, 1/4, 1/8, or 1/16 times the clock frequency. The polarity of SCLK is programmable.
SYNCA	O	Serial Data Output 1A sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCA is programmable.
SYNCB	O	Serial Data Output 1B sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCB is programmable.
SYNCC	O	Serial Data Output 1C sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCC is programmable.
SYNCD	O	Serial Data Output 1D sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCD is programmable.
MICROPROCESSOR INTERFACE		
P(15:0)	I/O	Microprocessor Interface Data bus. See *"Microprocessor Interface" on page 29*. P15 is the MSB.
ADD(2:0)	I	Microprocessor Interface Address bus. ADD2 is the MSB. See *"Microprocessor Interface" on page 29*. Note: ADD2 **is not** used but designated for future expansion.
$\overline{\text{WR}}$ or $\overline{\text{DSTRB}}$	I	Microprocessor Interface Write or Data Strobe Signal. When the Microprocessor Interface Mode Control, µP MODE, is a low data transfers (from either P(15:0) to the internal write holding register or from the internal write holding register to the target register specified) occur on the low to high transition of $\overline{\text{WR}}$ when $\overline{\text{CE}}$ is asserted (low). When the µP MODE control is high this input functions as a data read/write strobe. In this mode with RD/$\overline{\text{WR}}$ low data transfers (from either P(15:0) to the internal write holding register or from the internal write holding register to the target register specified) occur on the low to high transition of Data Strobe. With RD/$\overline{\text{WR}}$ high the data from the address specified is placed on P(15:0) when Data Strobe is low. See *"Microprocessor Interface" on page 29*.
$\overline{\text{RD}}$ or RD/$\overline{\text{WR}}$	I	Microprocessor Interface Read or Read/$\overline{\text{Write}}$ Signal. When the Microprocessor Interface Mode Control, µP MODE, is a low the data from the address specified is placed on P(15:0) when $\overline{\text{RD}}$ is asserted (low) and $\overline{\text{CE}}$ is asserted (low). When the µP MODE control is high this input functions as a Read/$\overline{\text{Write}}$ control input. Data is read from P(15:0) when high or written to the appropriate register when low. See *"Microprocessor Interface" on page 29*.
µP MODE	I	Microprocessor Interface Mode Control. This pin is used to select the Read/Write mode for the Microprocessor Interface. Internally pulled down. See *"Microprocessor Interface" on page 29*.
$\overline{\text{CE}}$	I	Microprocessor Interface Chip Select. Active low. This pin has the same timing as the address pins.
$\overline{\text{INTRPT}}$	O	Microprocessor Interrupt Signal. Asserted for a programmable number of clock cycles when new data is available on the selected Channel.

Functional Description

The HSP50216 is a four channel digital receiver integrated circuit offering exceptional dynamic range and flexibility. Each of the four channels consists of a front-end NCO, digital mixer, and CIC-filter block and a back-end FIR, AGC and Cartesian to polar coordinate-conversion block. The parameters for the four channels are independently programmable. Four parallel data input busses (A(15:0), B(15:0), C(15:0) and D(15:0)) and four pairs of serial data outputs (SDxA, SDxB, SDxC, and SDxD; x = 1 or 2) are provided. Each input can be connected to any or all of the internal signal processing channels, Channels 0, 1, 2 and 3. The output of each channel can be routed to any of the serial outputs. Outputs from more than one channel can be multiplexed through a common output if the channels are synchronized. The four channels share a common input clock and a common serial output clock, but the output sample rates can be synchronous or asynchronous. Bus multiplexers between the front end and back end sections provide flexible routing between channels for cascading back-end filters or for routing one front end to multiple back ends for polyphase filtering or systolic arrays (to provide wider bandwidth filtering). A level detector is provided to monitor the signal level on any of the parallel data input busses, facilitating microprocessor control of gain blocks prior to an A/D converter.

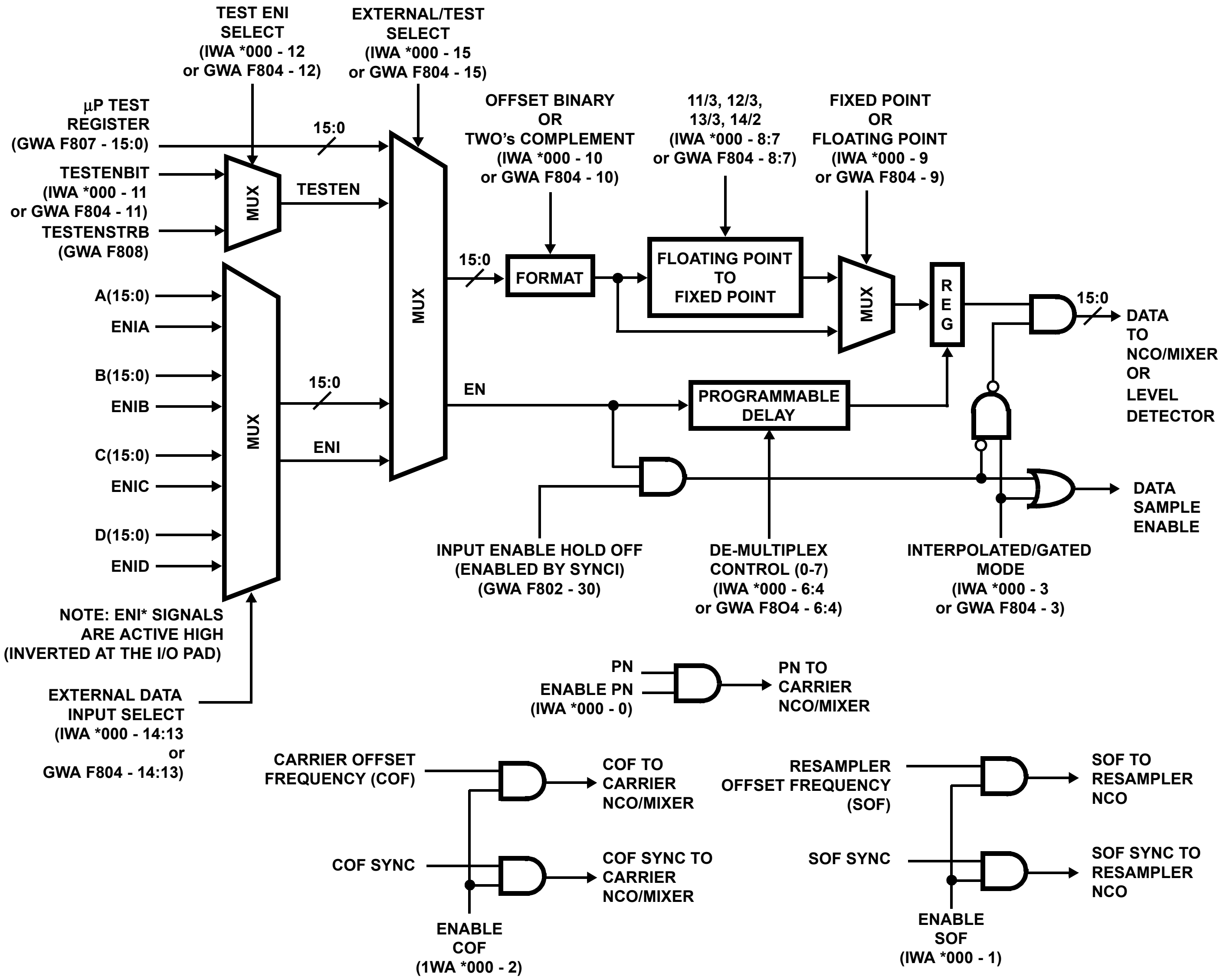
Each front end NCO/digital mixer/CIC filter section includes a quadrature numerically controlled oscillator (NCO), digital mixer, barrel shifter and a cascaded-integrator-comb filter (CIC). The NCO has a 32-bit frequency control word for 16.3mHz tuning resolution at an input sample rate of 70MSPS. The SFDR of the NCO is >115dB. The barrel shifter provides a gain of between 2^{-45} and 2^{-14} to prevent overflow in the CIC. The CIC filter order is programmable between 1 and 5 and the CIC decimation factor can be programmed from 4 to 512 for 5th order, 2048 for 4th order, 32768 for 3rd order, or 65536 for 1st or 2nd order filters.

Each channel back end section includes an FIR processing block, an AGC and a cartesian-to-polar coordinate converter. The FIR processing block is a flexible filter compute engine that can compute a single FIR or a set of cascaded decimating filters. A single filter in a chain can have up to 256 taps and the total number of taps in a set of filters can be up to 384 provided that the decimation is sufficient. The HSP50216 calculates 2 taps per clock (on each channel) for symmetric filters, generally making decimation the limiting factor for the number of taps available. The filter compute engine supports a variety of filter types including decimation, interpolation and resampling filters. The coefficients for the programmable digital filters are 22 bits wide. Coefficients are provided in ROM for several halfband filter responses and for a resampler. The AGC section can provide up to 96dB of either fixed or automatic gain control. For automatic gain control, two settling modes and two sets of loop gains are provided. Separate attack and decay slew rates are provided for each loop gain. Programmable limits allow the user to select a gain range less than 96dB. The outputs of the cartesian-to-polar coordinate conversion block, used by the AGC loop, are also provided as outputs to the user for AM and FM demodulation.

The HSP50216 supports both fixed and floating point parallel data input modes. The floating point modes support gain ranging A/D converters. Gated, interpolated and multiplexed data input modes are supported. The serial data output word width for each data type can be programmed to one of ten output bit widths from 4-bit fixed point through 32-bit IEEE 754 floating point.

The HSP50216 is programmed through a 16-bit microprocessor interface. The output data can also be read via the microprocessor interface for all channels that are synchronized. The HSP50216 is specified to operate to a maximum clock rate of 70MSPS over the industrial temperature range (-40°C to 85°C). The power supply voltage range is 3.3V ± 0.15V. The I/Os **are not** 5V tolerant.

Input Select/Format Block


TEST ENI SELECT (IWA *000 - 12 or GWA F804 - 12)
EXTERNAL/TEST SELECT (IWA *000 - 15 or GWA F804 - 15)
µP TEST REGISTER (GWA F807 - 15:0)
15:0
TESTENBIT (IWA *000 - 11 or GWA F804 - 11)
TESTENSTRB (GWA F808)
MUX
TESTEN
OFFSET BINARY OR TWO's COMPLEMENT (IWA *000 - 10 or GWA F804 - 10)
11/3, 12/3, 13/3, 14/2 (IWA *000 - 8:7 or GWA F804 - 8:7)
FIXED POINT OR FLOATING POINT (IWA *000 - 9 or GWA F804 - 9)
15:0
FORMAT
FLOATING POINT TO FIXED POINT
MUX
REG
15:0
DATA TO NCO/MIXER OR LEVEL DETECTOR
A(15:0)
ENIA
B(15:0)
ENIB
C(15:0)
ENIC
D(15:0)
ENID
MUX
15:0
ENI
MUX
EN
PROGRAMMABLE DELAY
DATA SAMPLE ENABLE
INPUT ENABLE HOLD OFF (ENABLED BY SYNCI) (GWA F802 - 30)
DE-MULTIPLEX CONTROL (0-7) (IWA *000 - 6:4 or GWA F8O4 - 6:4)
INTERPOLATED/GATED MODE (IWA *000 - 3 or GWA F804 - 3)
NOTE: ENI* SIGNALS ARE ACTIVE HIGH (INVERTED AT THE I/O PAD)
EXTERNAL DATA INPUT SELECT (IWA *000 - 14:13 or GWA F804 - 14:13)
PN
ENABLE PN (IWA *000 - 0)
PN TO CARRIER NCO/MIXER
CARRIER OFFSET FREQUENCY (COF)
COF TO CARRIER NCO/MIXER
COF SYNC
COF SYNC TO CARRIER NCO/MIXER
ENABLE COF (1WA *000 - 2)
RESAMPLER OFFSET FREQUENCY (SOF)
SOF TO RESAMPLER NCO
SOF SYNC
SOF SYNC TO RESAMPLER NCO
ENABLE SOF (IWA *000 - 1)

Each front end block and the level detector block contains an input select/format block. A functional block diagram is provided in the above figure. The input source can be any of the four parallel input busses (See *Microprocessor Interface* section, Table 3, "CHANNEL INPUT SELECT/FORMAT REGISTER (IWA = *000h)," on page 32 or a test register loaded via the processor bus (see *Microprocessor Interface* section, Table 42, "mP/TEST INPUT BUS REGISTER (GWA = F807h)," on page 45).

The input to the part can operate in a gated or interpolated mode. Each input channel has an input enable (ENIx, x = A, B, C or D). In the gated mode, one input sample is processed per clock that the ENIx signal is asserted (low). Processing is disabled when ENIx is high. The ENIx signal is pipelined through the part to minimize delay (latency). In the interpolated mode, the input is zeroed when the ENIx signal is high, but processing inside the part continues. This mode inserts zeros between the data samples, interpolating the input data stream up to the clock rate. On reset, the part is set to gated mode and the input enables are disabled. The inputs are enabled by the first SYNCI signal.

The input section can select one channel from a multiplexed data stream of up to 8 channels. The input enable is delayed by 0 to 7 clock cycles to enable a selection register. The register following the selection register is enabled by the non-delayed input enable to realign the processing of the channels. The one-clock-wide input enable must align with the data for the first channel. The desired channel is then selected by programming the delay. A delay of zero selects the first channel, a delay of 1 selects the second, etc.

The parallel input busses are 16 bits wide. The input format may be twos complement or offset binary format. A floating point mode is also supported. The floating point modes and the mapping of the parallel 16-bit input format is discussed below.

Floating Point Input Mode Bit Mapping

The input bit weighting for fixed point inputs on busses A, B, C, and D is: bit 15 (MSB): 2^{0}, bit 14: 2^{-1}, bit 13: 2^{-2}, ..., bit 0: 2^{-15}.

For floating point modes, the least significant 2 or 3 bits are used as exponent bits (See Floating Point Input Mode Bit Mapping Tables). The difference between the four floating point modes with three exponent bits is where the exponent saturates.

Floating Point Input Mode Bit Mapping Tables

A(15:0), B(15:0), C(15:0) or D(15:0):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{0}	**2^{-1}**	**2^{-2}**	**2^{-3}**	**2^{-4}**	**2^{-5}**	**2^{-6}**	**2^{-7}**	**2^{-8}**	**2^{-9}**	**2^{-10}**	**2^{-11}**	**2^{-12}**	**2^{-13}/(exp2)**	**(exp1)**	**(exp0)**

11-BIT MODE: 11 to 13-BIT MANTISSA, 3-BIT EXPONENT, 30dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING															
000	0	X15	X15	X15	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5
001	6	X15	X15	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4
010	12	X15	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3
011	18	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0
100	24	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0	0
101 (Note 1)	30	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0	0	0

NOTES:

1. Or 110 or 111, the exponent input saturates at 10.
2. “Xnn” = input A, B, C, or D bit nn.

12-BIT MODE: 12 to 13-BIT MANTISSA, 3-BIT EXPONENT, 24dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING															
000	0	X15	X15	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4
001	6	X15	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3
010	12	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0
011	18	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0	0
100 (Note 3)	24	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0	0	0

NOTE:

3. Or 101, 110, or 111, the exponent input saturates at 100.

13-BIT MODE: 13-BIT MANTISSA, 3-BIT EXPONENT, 18dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING															
000	0	X15	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3
001	6	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0
010	12	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0	0
011 (Note 4)	18	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	0	0	0

NOTE:

4. Or 100, 101, 110, or 111, the exponent input saturates at 011.

14-BIT MODE: 14-BIT MANTISSA, 2-BIT EXPONENT, 12dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING															
00	0	X15	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2
01	6	X15	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	0
10 (Note 5)	12	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	0	0

NOTE:

5. Or 11, the exponent input saturates at 10.

Level Detector

An input level detector is provided to monitor the signal level on any of the input busses. Which input bus, the input format, and the level detection type are programmable (see Microprocessor Interface section, Table 39, "INPUT LEVEL DETECTOR SOURCE SELECT/FORMAT REGISTER (GWA = F804h)," on page 44, Table 40, "INPUT LEVEL DETECTOR CONFIGURATION REGISTER (GWA = F805h)," on page 45 and Table 41, "INPUT LEVEL DETECTOR START STROBE REGISTER (GWA = F806h)," on page 45). This signal level represents the wideband signal from the A/D and is useful for controlling gain/attenuation blocks ahead of the converter. The supported monitoring modes are: integrated magnitude (like the HSP50214 without the threshold), leaky integration ($Y_n = X_n \times A + Y_{n-1} \times (1-A)$) where A = 1, 2^{-8}, 2^{-12}, or 2^{-16} (see GWA = F805h), and peak detection. The measurement interval can be programmed from 2 to 65537 samples (or continuous for the leaky integrator and peak detect cases). The output is 32 bits and is read via the µP interface.

NCO/Mixer

After the input select/format section, the samples are multiplied by quadrature sine wave samples from the carrier NCO. The NCO has a 32-bit frequency control, providing sub-hertz resolution at the maximum clock rate. The quadrature sinusoids have exceptional purity. The purity of the NCO should not be the determining factor for the receiver dynamic range performance. The phase quantization to the sine/cosine generator is 24 bits and the amplitude quantization is 19 bits.

The carrier NCO center frequency is loaded via the µP bus. The center frequency control is double buffered - the input is loaded into a center frequency holding register via the µP interface. The data is then transferred from the holding register to the active register by a write to a address IWA *006h or by a SYNCI signal, if loading via SYNCI is enabled. To synchronize multiple channels, the carrier NCO phase accumulator feedback can be zeroed on loading to restart all of the NCOs at the same phase. A serial offset frequency input is also available for each channel through the D(15:0) parallel data input bus (if that bus is not needed for data input). This is legacy support for HSP50210 type tracking signals. See IWA = *000 and *004 for carrier offset frequency parameters.

After the mixers, a PN (pseudonoise) signal can be added to the data. This feature is provided for test and to digitally reduce the input sensitivity and adjust the receiver range (sensitivity). The effect is the same as increasing the noise figure of the receiver, reducing its sensitivity and overall dynamic range. For testing, the PN generator provides a wideband signal which may be used to verify the frequency response of a filter. The one bit PN data is scaled by a 16-bit programmable scale factor. The overall range for the PN is 0 to 1/4 full scale (see IWA = *001h). A gain of 0 disables the PN input. The PN value is formed as

PN Value

			2^{-3}	2^{-4}	·	·	·	·	·	·	·	·	·	·	·	·	2^{-17}	2^{-18}
S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

where S is the PN generator output bit (treated as a sign bit) and the 16 X's refer to the PN Gain Register IWA = *001h.

The minimum, non-zero, PN value is 2^{-18} of full scale (-108dBFS) on each axis (-105dBFS total). For an input noise level of -75dBFS, this allows the SNR to be decreased in steps of 1/8dB or less. The I and Q PN codes are offset in time to decorrelate them. The PN code is selected and enabled in the test control register (F800h). The PN is added to the signal after the mix with the three sign bits aligned with the most significant three bits of the signal, so the maximum level is -12dBFS and the minimum, non-zero level is -108dBFS. The PN code can be 2^{15}-1, 2^{23}-1 or 2^{15}-1 * 2^{23}-1.

CIC Filter

Next, the signal is filtered by a cascaded integrator/comb (CIC) filter. A CIC filter is an efficient architecture for decimation filtering. The power or magnitude squared frequency response of the CIC filter is given by:

$$P(f) = \left(\frac{\sin(\pi M f)}{\sin\left(\frac{\pi f}{R}\right)}\right)^{2N}$$

where

M = Number of delays (1 for the HSP50216)

N = Number of stages

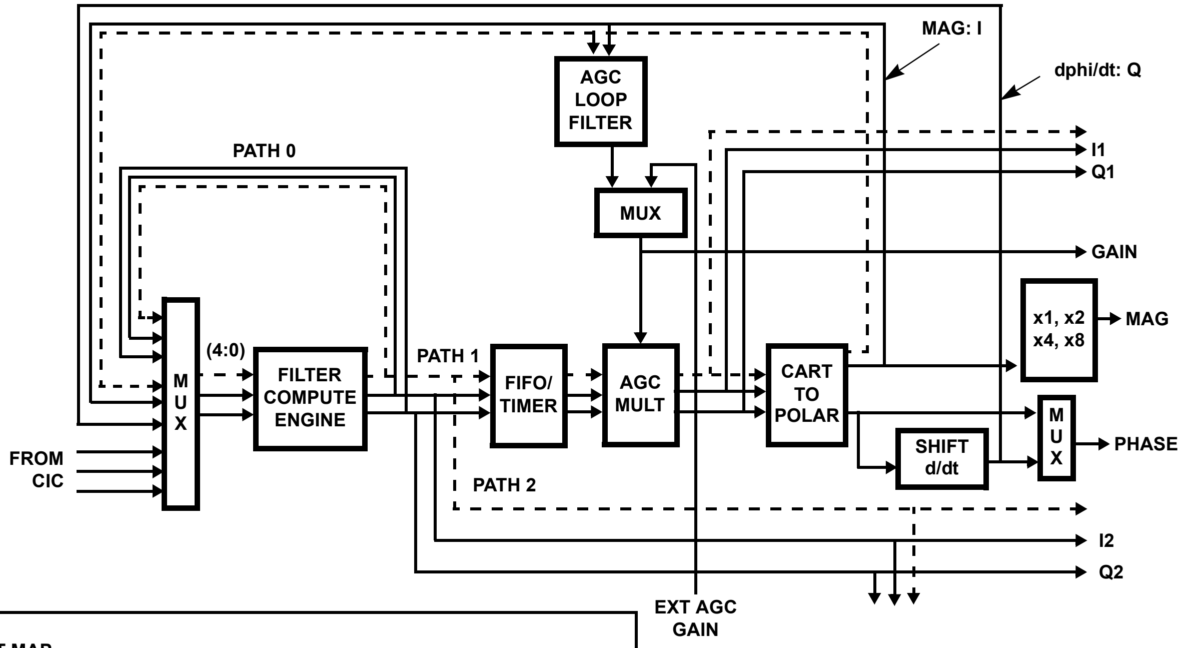
and R = Decimation factor.

The passband frequency response for 1st (N = 1) though 5th (N=5) order CIC filters is plotted in Figure 8. The frequency axis is normalized to f_S/R, making $f_S/R = 1$ the CIC output sample rate. Figure 10 shows the frequency response for a 5th order filter but extends the frequency axis to $f_S/R = 3$ (3 times the CIC output sample rate) to show alias rejection for the out of band signals. Figure 9 uses information from Figure 10 to provide the amplitude of the first (strongest) alias as a function of the signal frequency or bandwidth from DC. For example, with a 5th order CIC and $f_S/R = 0.125$ (signal frequency is 1/8 the CIC output rate) Figure 9 shows a first alias level of about -87dB. Figure 9 is also listed in table form in Table 47.

The CIC filter order is programmable from 0 to 5. The minimum decimation is 4. If the order is set to 0, there must be at least 4 clocks between samples or the decimation counter must be set to 4 to chose every 4th sample.

The integrator bit widths are 69, 62, 53, 44, and 34 for the 1st through 5th stages, respectively, while the comb bit widths are all 32. The integrators are sized for decimation factors of up to 512 with 5 stages, 2048 with 4 stages, 32768 with 3 stages, and 65536 with 1 or 2 stages. Higher decimations in the CIC should be avoided as they will cause integrator overflow. In the HSP50216, the integrators are slightly oversized to reduce the quantization noise at each stage.

Backend Data Routing



DESTINATION BIT MAP
(BITS 28:18 OF FIR INSTRUCTIONS BIT FIELD)

28	27	26	25	24	23	22	21	20	19	18

28	AGC LOOP GAIN SELECT (PATH 01 ONLY)
27	UPDATE AGC LOOP (PATH 01 ONLY)
26, 25	PATH 00 - - IMMEDIATE FILTER PROCESSOR FEEDBACK PATH 01 - - FIFO/AGC PATH 10 - - DIRECT OUT/CASCADE PATH 11 - - BOTH 00 AND 10 PATHS (FOR TEST)
24	STROBE OUTPUT SECTION (START SERIAL OUTPUT WITH THIS SAMPLE)
23	FEED MAG/PHASE BACK TO FILTER PROCESSOR
22:18	FILTER PROCESSOR SEQUENCE STEP NUMBER

A CIC filter has a gain of R^N, where R is the decimation factor and N is the number of stages. Because the CIC filter gain can become very large with decimation, an attenuator is provided ahead of the CIC to prevent overflow. The 24 bits of sample data are placed on the low 24 bits of a 69 bit bus (width of the first CIC integrator) for a gain of 2^{-45}. A 32 bit barrel shifter then provides a gain of 2^0 to 2^{31} inclusive before passing the data onto the CIC. The overall gain in the pre-CIC attenuator can therefore be programmed to be any one of 32 values from 2^{-45} to 2^{-14}, inclusive (see IWA=*004, bits 18:14). This shift factor is adjusted to keep the total barrel shifter and CIC filter between 0.5 and 1.0. The equation which should be used to compute the necessary shift factor is:

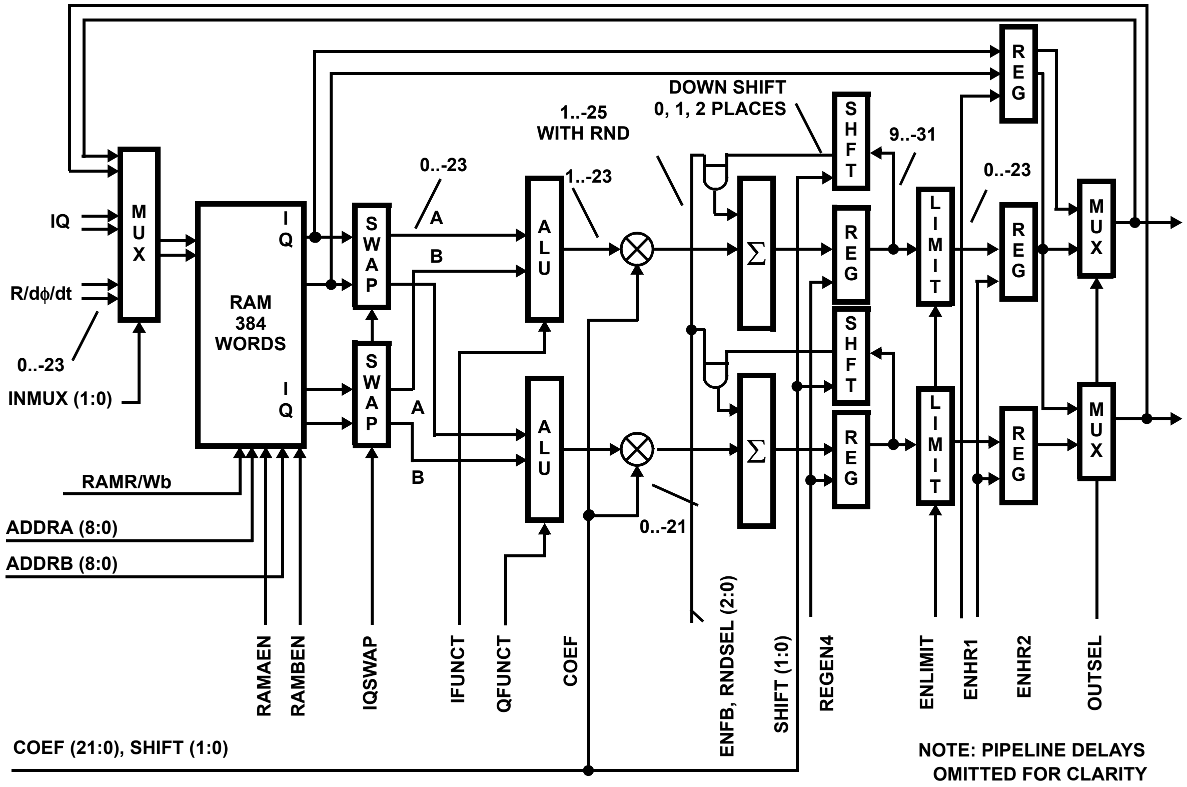
$$\text{Shift Factor} = 45 - \text{Ceiling}(\log_2(R^N)).$$

NOTE: With a CIC order of zero, the CIC shifter does not have sufficient range to route more than 10 bits to the back end since the maximum gain is 2^{-14} (the least significant 14 bits are lost).

Back End Section

One back-end processing section is provided per channel. Each back end section consists of a filter compute engine, a FIFO/timer for evenly spacing samples (important when implementing interpolation filters and resamplers), an AGC and a cartesian-to-polar coordinate conversion block. A block diagram showing the major functional blocks and data routing is shown above. The data input to the back end section is through the filter compute engine. There are two other inputs to the filter compute engine, they are a data recirculation path for cascading filters and a magnitude and $d\phi/dt$ feedback path for AM and FM filtering. There are seven outputs from each back end processing section. These are I and Q directly out of the filter compute engine (I2, Q2), I and Q passed through the FIFO and AGC multipliers (I1, Q1), magnitude (MAG), phase (or $d\phi/dt$), and the AGC gain control value (GAIN). The I2/Q2 outputs are used when cascading back end stages. The routing of signals within the back end processing section is controlled by the filter compute engine. The routing information is embedded in the instruction bit fields used to define the digital filter being implemented in the filter compute engine.

Filter Compute Engine



The filter compute engine is a dual multiply-accumulator (MAC) data path with a microcoded FIR sequencer. The filter compute engine can implement a single FIR or a set of filters. For example, the filter chain could include two halfband filters, a shaping (matched) filter and a resampling filter, all with different decimations. The following filter types are currently supported by the architecture and microcode:

- Even symmetric with even # of taps decimation filters
- Even symmetric with odd # of taps decimation filters (including HBFs)
- Odd symmetric with even # of taps decimation filters
- Odd symmetric with odd # of taps decimation filters
- Asymmetric decimation filters
- Complex filters
- Interpolation filters (up to interpolate by 4)
- Interpolation halfband filters
- Resampling filters (under resampler NCO control)
- Fixed resampling ratio filter (within the available number of coefficients)
- Quadrature to real filtering (w/ fs/4 up conversion)

The input to the filter compute engine comes from one of three sources - a CIC filter output (which can also be another backend section), the output of the filter compute engine (fed back to the input) or the magnitude and dϕ/dt fed back from the cartesian-to-polar coordinate converter.

The number and size of the filters in the chain is limited by the number of clock cycles available (determined by the decimation) and by the data and coefficient RAM/ROM resources. The data RAM is 384 words (I/Q pairs) deep. The data addressing is modulo in power-of-2 blocks, so the maximum filter size is 256. The block size and the block starting memory address for each filter is programmable so that the available memory can be used efficiently. The coefficient RAM is 192 words deep. It is half the size of the data memory because filter coefficients are typically symmetric. ROMs are provided with halfband filter coefficients, resampling filter coefficients, and constants. The filter compute engine exploits symmetry where possible so that each MAC can compute two filter taps per clock, by doing a pre-add before multiplying. In the case of halfband filters, the zero-valued coefficients are skipped for extra efficiency. There is an overhead of one clock cycle per input sample for each filter in the chain (for writing the data into the data RAM) and (except in special cases) a two clock cycle overhead for the entire chain for program flow control instructions.

The output of the filter compute engine is routed through a FIFO in the main output path. The FIFO is provided to more evenly space the FIR outputs when they are produced in bursts (as when computing resampling or interpolation filters). The FIFO is four samples deep. The FIFO is loaded by the output of the filter when that path is selected. It is unloaded by a counter. The spacing of the output samples is specified in clock periods. The spacing can be set from 1 (fall through) to 4096 samples (approximately the spacing for a 16KSPS output sample rate when using 65MSPS clock) using IWA = *00Ah bits 11:0.

The number and order of the filtering in the filter chain is defined by a FIR control program. The FIR control program is a sequence of up to 32 instruction words. Each instruction word can be a filter or program flow instruction. The filter instruction defines a FIR in the chain, specifying the type of FIR, number of taps, decimation, memory allocation, etc. For program flow, a wait for input sample(s) instruction, a loop counter load, and several jumps (conditional and unconditional) are provided. The HSP50216 evaluation board includes software for automatically generating FIR control programs for most filter requirements. Examples of programs FIR control programs are given below.

The simplest filter program computes a single filter. It has three instructions (see Sample Filter #1 Program Instructions below):

SAMPLE FILTER #1 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (equal to the decimation factor)
1	FIR Type = even symmetric 95 taps Decimate by 2 Compute one output Decrement wait counter Memory block size 128 Memory block start at 64, Coefficient block start at 64 Step size 1 Output to AGC
2	Jump, Unconditional, to step 0

The parameters of the FIR (including type, number of taps, decimation and memory usage) are specified in the bit fields of the step 1 instruction word. To change the filtering the only other change needed is the number of samples in the wait threshold register (IWA = *00C, bits 9:0). The filter in this example requires 52 clock cycles to compute, allocated as follows:

SAMPLE FILTER #1 CLOCK CYCLES CALCULATION

CLOCK CYCLES	FUNCTION PERFORMED
48	Clocks for FIR computation (two taps/clock due to symmetry)
2	Clocks for writing the input data into the data RAMs (Decimate by 2 requires 2 inputs per output)
2	Clocks for the program flow instructions (wait and jump)
52	Total

Using a 65MSPS clock, the output sample rate could be as high as 65MSPS/52 clocks = 1.25MSPS. The input sample rate to the FIR from the CIC filter would be 2.5MSPS. The impulse response length would be 38 µsec (95 taps at 0.4µs/tap).

Each additional filter added to the signal processing chain requires one instruction step. As an example of this, a typical filter chain might consist of two decimate-by-2 halfband filters being followed by a shaping filter with the final filter being a resampling filter. The program for this case might be (see Sample Filter Program #2 Program Instructions below):

SAMPLE FILTER #2 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (usually equal to the total decimation -- 8 in this case)
1	FIR Type = even symmetry 15 taps Halfband Decimate by 2 Compute four outputs Memory block size 32 Memory block start at 0 Coefficient block start at 13 Output to step 2 Decrement wait count
2	FIR Type = even symmetry 23 taps Halfband Decimate by 2 Compute two outputs Memory block size 32 Memory block start at 32 Coefficient block start at 24 Output to step 3
3	FIR Type = even symmetry 95 taps Decimate by 2 Compute one output Memory block size 128 Memory block start at 64 Coefficient block start at 64 Step size 1 Output to step 4
4	FIR Type = resampler Increment NCO 6 taps Compute one output Memory block size 8 Memory block starts at 192 Coefficient block start at 512 Step size 32 Output to AGC
5	Jump, Unconditional, to 0

Sample filter #2 requires:

- 32 + 32 + 128 + 8 = 200 data RAM locations
- (95+1)/2=48 coefficient RAM location (resampler and HBF coefficients are in ROM).

The number of clock cycles required to compute an output for Sample filter #2 is calculated as follows:

SAMPLE FILTER #2 CLOCK CYCLES CALCULATION

CLOCK CYCLES	FUNCTION PERFORMED
20	Halfband 1 compute clocks (5 per compute x 4 computes)
8	Halfband 1 input sample writes (8 input samples)
14	Halfband 2 compute clocks (7 per compute x 2 computes)
4	Halfband 2 input sample writes (4 input samples)
48	95 tap symmetric FIR, 2 clocks per tap
2	FIR input sample writes (2 input samples)
6	resampler (6 taps, nonsymmetric)
1	Resampler input sample write (1 input samples)
1	Jump instruction
1	Wait instruction
105	Clock cycles per output

Total decimation is 8, so the input sample rate for the FIR chain (CIC output rate) could be up to:

f_{CLK}/(ceil(105/8)) = f_{CLK}/14.

With a 65MHz clock, this would support a maximum input sample rate to the FIR processor of 4.6MHz and an output sample rate up to 0.580MHz. The shaping filter impulse response length would be:

(95 x 2)/580,000 = 82µs.

The maximum output sample rate is dependent on the length and number of FIRs and their decimation factors.

Illustrating this concept with Filter Example #3, a higher speed filter chain might be comprised of one 19 tap decimate-by-2 halfband filter followed by a 30 tap shaping FIR filter with no decimation. The program for this example could be:

SAMPLE FILTER #3 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (2 in this case)
1	FIR Type = even symmetry 19 taps Halfband Decimate by 2 Compute one output Memory block size 32 Memory block start at 0 Coefficient block start at 18 Output to step 2 Reset wait count
2	FIR Type = even symmetry 30 taps Decimate by 1 Compute one output Memory block size 64 Memory block start at 32 Coefficient block start at 64 Step size 1 Output to AGC
3	Jump, Unconditional, to 0

The number of clock cycles required to compute an output for Sample filter #3 is calculated as follows:

SAMPLE FILTER #3 CLOCK CYCLES CALCULATION

CLOCK CYCLES	FUNCTION PERFORMED
6	19 tap halfband, one output
2	halfband input writes (2 input samples)
15	30 tap symmetric FIR, 2 taps per clock
1	1 FIR input write
1	1 wait
1	1 jump
26	Clock cycles per output

For Filter Example #3 and a 65MSPS input, the maximum FIR input rate would be 65MSPS/ceil(26/2) = 5MSPS giving a decimate-by-2 output sample rate of 2.5MSPS. At 70MSPS, the FIR could have up to 34 taps with the same output rate.

Channels 0, 1, 2 and 3 can be combined in a polyphase structure for increased bandwidth or improved filtering.

Filter Example #4 will be used to demonstrate this capability.

Symbol rate of 4.096 MSym. The desired output sample rate is 8.192MSPS. Arrange the four back end sections as four filters operating on the same CIC output at a rate of

65.536MHz/4=16.384MHz, where the factor of 4 is the CIC decimation we have chosen.

Each channel computes the same sequence, offset by one output sample from the previous sample (see IWA = *00Bh). Each channel decimates down to 2.048M and then the channels are multiplexed together in the output formatter to get the desired 8.192MSPS. The input sample rate to the final filter of each channel must meet Nyquist requirements for the final output to assure that no information is lost due to aliasing.

SAMPLE FILTER #4 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (8 in this case)
1	FIR type = even symmetry 44 taps decimate by 8 compute one output memory block size 64 memory block start at 0 coefficient block start at 64 step size 1 output to AGC offset memory read pointers by 0, -2, -4, -6
2	Jump, Unconditional, to 0

The number of FIR taps available for these requirements is calculated as follows:

65536/2048 = 32 clocks

minus (8 writes + 1 wait + 1 jump = 10 clocks)

= 22 clocks

Therefore, the number of taps available is:

22 x 2 = 44 taps.

Multiplexing the four outputs gives a final output sample rate of 8.192MSPS.

The impulse response is 44 taps at 16.384M or 22 output samples (11 symbols at 4.096M).

The AGC loop filter output of channel 4 can be routed to control the forward AGC gain control of all four channels. This assures that the gains of the four back end sections are the same. The gain error, however, is only computed from every fourth output sample.

The back end processing sections of two or more HSP50216s can be combined using the same polyphase approach, but the AGC gain from one part cannot be shared with another part (except via the µP interface), so polyphase filter using multiple parts would typically usually use a fixed gain.

The filter sequencer is programmed via an instruction RAM and several control registers. These are described below.

Instruction RAMs

The filter compute engine is controlled by a simple sequencer supporting up to 32 steps. Each step can be a filter or one of four sequence flow instructions - wait, jump (conditional or unconditional), load loop counter, or NOP. There are 128 bits per instruction word with each word consisting of condition code selects, FIR parameters and data routing controls. Not all of the instruction word bits are used for all instruction types. The actual sequencer instruction is only 9 bits. The rest of the bits are used for filter parameters or for the loop counter preload. Each sequence step is loaded in four 32-bit writes. The mapping of the bit fields for the instruction types is shown in the instruction bit field table that follows. These FIR instruction words can be generated using software tools provided with the HSP50216 evaluation board.

When the filter is reset, the instruction pointer is set to 31 (the last instruction step). The read and write pointers are initialized on reset, so a reset must be done when the channel is initialized or restarted.

A fixed offset can be added to the starting read address of one of the filters in the program. This function is provided to offset the data reads of the filters in a polyphase filter bank -- all filters in the bank will write the same data to the same RAM location. To offset the computations the RAM read address is offset. See IWA = *00Bh for details.

The instruction word bits (127:0) are assigned to memory words as follows:

31:0 to destination C C C C 0 0 0 1 0 x x x x x 0 0

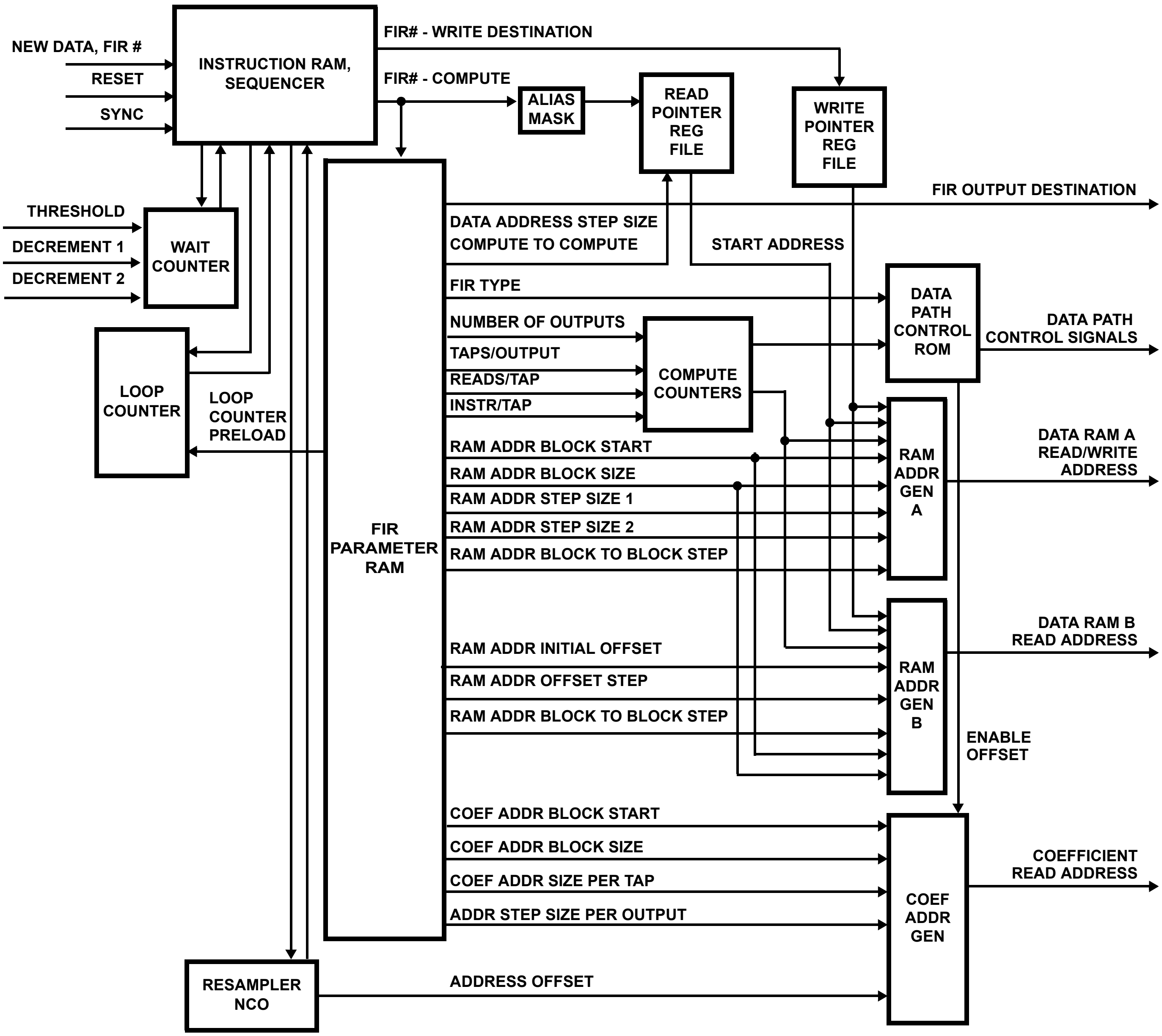
63:32 to destination C C C C 0 0 0 1 0 x x x x x 0 1

95:64 to destination C C C C 0 0 0 1 0 x x x x x 1 0

127:96 to destination C C C C 0 0 0 1 0 x x x x x 1 1

where CCCC is the channel number and xxxxx is the instruction sequence step number (0 - 31 decimal). Note the µPHold bit in the filter compute engine control register (IWA = *00Ah) must be set for the microprocessor to read from or write to the instruction or coefficient RAMs.

Filter Sequencer



Instruction Bit Fields

INSTRUCTION BIT FIELDS

BIT POSITIONS	FUNCTION	DESCRIPTION
8:0	Instruction	Instruction Field Bit Mapping Bit Type 8 7 6 5 4 3 2 1 0 WAIT 0 0 X X X X C C C FIR 0 1 Start IncrRS DecrSel DecrEn LdLp DecrLp EnU/C JUMP 1 J J J J J C C C (NOPs and loading the loop counter are special cases of the FIR instruction). XXXX = ignored. JJJJJ = jump destination (sequence step number). CCC = condition code. 000 = $\overline{(\text{waitcount} \geq \text{threshold})}$ -- See IWA = *00Ch, bits 9:0 for threshold details. 001 = waitcount ≥ threshold -- See IWA = *00Ch, bits 9:0 for threshold details. 010 = loop counter ≠ 0. 011 = loop counter = 0. 100 = $\overline{\text{RSCO}}$ Tab (RSCO - resampler NCO carry output). 101 = RSCO. 110 = sync (if enabled) or µP controlled bit. 111 = always. Start = load parameters and start filter computation, set to zero for no-ops, loop counter loads. IncrRS = increment resampler during this filter. Increments on start or at each FIR output depending on µPcontrol bit. DecrSel = selects between two decrement values for the wait counter. DecrEn = decrement wait count on starting this instruction. LdLp = load loop counter with the data in the I(20:9) bit field. The start bit should not be set when this bit is set. DecrLp = decrement loop counter on starting this instruction. EnU/C = enable U/C counter with this FIR. This multiplies the data by 1, j, -1, -j. The multiplication factor changes each time the filter runs.
14:9	FIR Type	FIR Parameter Bit Fields 14:9 FIR type. 000000 NOP. 000001 Decimating FIR, Even Symmetric, Even # Taps. 000010 Decimating FIR, Even Symmetric, Odd # Taps. 000011 Decimating FIR, Odd Symmetric, Even # Taps. 000100 Decimating FIR, Odd Symmetric, Odd # Taps. 000101 Decimating FIR, Asymmetric. 001000 Resampling FIR, Asymmetric. 001001 Interpolating HBF. 100000 Decimating FIR, Complex (Asymmetric). NOTES: 1. Regular interpolation FIRs are successive runs of a FIR with no data address increment, but with coefficient start address increments. 2. Decimating HBFs are even symmetric, odd number of taps but with different data step sizes. 3. U/C FIR is a normal FIR with the U/C bit enabled. 4. Other codes may be added in the future.
17:15	Steps per FIR	Specifies the number of steps per FIR instruction sequence (load with value minus 1) (set to 0 for all FIR types except complex which is set to 1).

INSTRUCTION BIT FIELDS (Continued)

BIT POSITIONS	FUNCTION	DESCRIPTION
28:18	Destination	Destination Field Bit Mapping 28 27 26 25 24 23 22 21 20 19 18 AGCLFGN AGCLF Path1 Path0 OS FB F4 F3 F2 F1 F0 AGCLFGNAGC loop gain select. Only applies to Path 1. Loop gain 0 or 1 if AGCLF bit is set. Set to 0 (1 is a test mode for future chips). AGCLF AGC loop filter enable. Only applies to Path 1. The AGC loop is updated with the magnitude of this sample (Path(1:0) = 01). Path(1:0) Back End Data Routing Path Selection. 00Route output back to filter compute engine input to another FIR in the filter chain. 01Route output through the FIFO and AGC forward path to the cartesian-to-polar coordinate converter conversion and output (I1, Q1, magnitude, phase, gain) and also to route to a discriminator (i.e., dϕ/dt FIR). 10Route output directly to the output, bypassing the FIFO and AGC (I2, Q2). This path also routes to next channel FIR input. OS Enable output strobe. Setting this bit generates a data ready signal when the data reaches the output section and starts the serial output sequence (paths 1, 2, 3). If OS is not set, there will be no output to the outside world from this channel, for that output calculation, but the data will be loaded into its output holding register (OS would not be set when routing the data to another back end when cascading channels). FB Feedback data path. When set, the magnitude and dphi/dt from the cartesian-to-polar coordinate converter block are routed to the filter compute engine input (magnitude goes to the I input and dphi/dt goes to the Q input). Provided for discriminator filtering. F(4:0) Filter select. For data recirculated to the input of the FIR processor by path 0 or from the cartesian to polar coordinate converter output, these bits tell which filter sequencer step gets it as an input.
31:29	Round Select	31:29 Round Select (Add rounding bit at specified location). 000 2^{-24}, use this code when downshifting is not used. 001 2^{-23} 010 2^{-22} 011 2^{-21} 100 2^{-20} 101 2^{-19} 110 2^{-18} 111 no rounding. Provided for use with the coefficient down-shift bits.
41:32	Data Memory Block Start	Memory block base address, 0-1023, 0-383 are valid for the HSP50216.
44:42	Data Memory Block Size	44:42 Block Size. 0 8 1 16 2 32 3 64 4 128 5 256 6 512 7 1024 (modulo addressing is used).
52:45	Data Memory Block-to-Block Step	0-255, usually equal to the decimation factor for the FIR in this instruction.

INSTRUCTION BIT FIELDS (Continued)

BIT POSITIONS	FUNCTION	DESCRIPTION
62:53	Coefficient Memory Block Start	Memory base address of coefficients, 0-1023, 0-511 are valid on the HSP50216.
63	Reserved	Set to 0.
66:64	Coefficient Memory Block Size	66:64 Memory Block Size 0 8 1 16 2 32 3 64 4 128 5 256 6 512 7 1024 (Modulo addressing can be used, but is usually not needed. If not needed this bit field can always be set to 7).
75:67	Number of FIR Outputs	Number of FIR outputs (range is 1 to 512, load w/ desired value minus 1). This is usually equal to the total decimation that follows the filter.
84:76	Read Address Pointer Step	Read address pointer step (for next run). This is usually equal to the filter decimation times the number of outputs from the instruction.
93:85	Initial Address Offset	Initial address offset (to ADDRB). This is the offset from the start address to other end of filter. For symmetric filters, usually equal to -1 x (number of taps -1).
95:94	Reserved	Set to 0
104:96	Memory Reads Per FIR Output	This is based on the number of taps (load with value below minus 1). Type Value Symmetric even number of taps(taps/2) or floor((taps+1)/2). Symmetric odd number of taps (taps+1)/2 or floor((taps+1)/2). Decimating HBF (taps+5)/4. Asymmetric taps. Complex taps. Resampling taps/phase (six taps per phase for the ROM'd coefficients provided). Interpolating HBF (taps+5)/4-1.
106:105	Clocks Per Memory Read	Set to 0 for all but complex FIR, which is set to 1.
115:107	Data Memory Step Size 1	(ADDRA) Step size for all but the last tap computation of the FIR. Set to -2 for HBF, -1 otherwise.
117:116	Data Memory Step Size 2	(ADDRA) Step size for last tap computation. Set to -1. 117:116 Step size 0 0 1 -1 2 -2 3 step size value.
119:118	Data Memory Address Offset Step	(ADDRB) Step size for opposite end of symmetric filter. Set to +2 for Decimating HBF, to +1 for others (the B data is not used for asymmetric, resampling, and complex filters).

INSTRUCTION BIT FIELDS (Continued)

BIT POSITIONS	FUNCTION	DESCRIPTION
122:120	Coefficient Memory Step Size	(ADDRC) Usually set to 1. 122:120 Step size 0 0 1 1 2 2 3 4 4 8 5 16 6 32 7 64
125:123	Coefficient Memory Block-to-Block Step	(ADDRC) Usually set to 0. 125:123 Step size 0 0 1 1 2 2 3 4 4 8 5 16 6 32 7 64
127:126	Reserved	Set to 0

Basic Instruction Set Examples

1. Wait for number of input samples ≥ threshold
   127:9 = 0
   8:0 = 001
   0000,0000,0000,0001h
2. Jump unconditional
   127:9 = 0
   8:0 = 1JJJJJ111b
   example: jump to step 0 = 0000,0000,0000,0107h
3. Jump RSCO (jump on resampler NCO carry output)
   127:9 = 0
   8:0 = 1JJJJJ101b
   example: jump RSCO, step 0= 0000,0000,0000,0105h
4. Jump $\overline{\text{RSCO}}$ (jump on no resampler NCO carry output)
   127:9 = 0
   8:0 = 1JJJJJ100b
   example: jump $\overline{\text{RSCO}}$, step 0 = 0000,0000,0000,0104h
5. NOP single clock
   127:9 = 0
   8:0 = 010000000b
   NOP1 = 0000,0000,0000,0080h
6. Load Loop Counter
   127:21 = 0
   20:9 = Loop counter preload (tested against 0)
   8:0 = 010000100b
   example: LdLpCntr 14 = 0000,0000,0000,1C84h

Single FIR Basic Program

This is the basic program for a single FIR. This program applies to decimation filters (including DECx1) that are symmetric or asymmetric (but not complex). The FIR output is routed through path A with the AGC enabled.

0 - WAIT FOR ENOUGH SAMPLES

0000	0000	0000	0000	0000	0000	0000	0000	127:96	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	95:64	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	64:32	00000000h
0000	0000	0000	0000	0000	0000	0000	0001	31:0	00000001h

1 - FIR

0000	0001	0101	1111	1111	100R	RRRR	RRRR	127:96	015FF---h
00TT	TTTT	TTTD	DDDD	DDDD	0000	0000	0111	95:64	-----007h
0000	1000	0000	0000	0000	1010	0000	0000	63:32	08000A00h
0000	1011	0000	0000	0FFF	FFF0	1100	1000	31:0	0B00--C8h

2 - JUMP TO STEP 0

0000	0000	0000	0000	0000	0000	0000	0000	127:96	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	95:64	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	64:32	00000000h
0000	0000	0000	0000	0000	0001	0000	0111	31:0	00000107h

Four bit fields must be filled in:
F - filter type (this example applies to types 1-5)
D - decimation (also loaded into wait threshold)
T - number of taps minus 1
R - clocks/calculation (= floor((taps+1)/2) for symmetric, = taps for asymmetric)

The rest of the instruction RAM would typically be filled with NOP instructions:

0000	0000	0000	0000	0000	0000	0000	0000	127:96	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	95:64	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	64:32	00000000h
0000	0000	0000	0000	0000	0000	1000	0000	31:0	00000080h

Wait Preload Register

This register (IWA register *00Ch) holds the wait counter threshold and two wait counter decrement values. Each is 10 bits. The wait counter counts filter input samples until the count is greater than or equal to the threshold. The wait counter then asserts a flag to the filter compute engine.

The wait counter threshold is typically set to the total number of input samples needed to generate a filter output. A “WAIT” instruction in the filter compute engine waits for the wait counter flag signal before proceeding. The filter compute engine would then compute all the filters needed to produce an output and then would jump back to the “WAIT” instruction.

The wait counter is implemented with an accumulator. This allows the count to go beyond the threshold without losing the sample count. Two bits in the FIR instruction decrement the wait counter (subtract a value) and select the decrement value. The decrement value is typically the number of samples needed for an output (total decimation), though it can be a different value to ignore inputs and shift the timing. (The read pointer increment must be adjusted as well.)

The filter compute engine sequencer does not count each input sample or track whether each filter is ready to run. Instead, the wait counter is used to determine whether there are enough input samples to compute all the filters in the chain and get an output sample from the entire filter chain. This adds some additional delay since intermediate results are not precalculated, but it simplifies the filter control. The number of samples needed is equal to the total decimation of the filter chain. For example, with two decimate-by-2 halfband filters and a decimate-by-2 shaping FIR, the total decimation would be 8 so 8 samples are needed to compute an output. HBF1 would compute four times to generate four inputs to HBF2. HBF2 would compute twice to generate the two samples that the shaping FIR needs to compute an output.

Resampler

The resampler is an NCO controlled polyphase filter that allows the output sample rate to have a non-integer relationship to the input sample rate. The filter engine can be viewed conceptually as a fixed interpolate-by-32 filter, followed by an NCO controlled decimator. The Resampler NCO is similar to the carrier NCO phase accumulator but does not include the SIN/COS section. It provides the resampler output pulse and associated phase information to logic that determines the nearest of the 32 available phase points for a given output sample.

The center frequency (output sample rate) control is double buffered, i.e., the control word is written to one register via the microprocessor interface and then transferred to another (active) register on a write to the timing NCO center frequency update strobe location (IWA register *009h) or on a SYNCI (if enabled). As it is not possible to represent some frequencies exactly with an NCO and therefore, phase error accumulates eventually causing a bit slip, the phase accumulator length has been sized to where the error is insignificant. At a resampler input rate of 1MHz, half an LSB of error in loading the 56-bit accumulator is $7*10^{-12}$ degrees. After 1 year, the accumulated phase error is only $0.2*10^{-3}$ of a bit (< 1/10 of a degree). The NCO update by the filter compute engine is typically at the resampler's input rate, and is enabled by the IncrRS bit in the filter instruction word. The NCO then rolls over at a fraction of the resampler input rate. The output sample rate is $(f_{IN}/ 2^{56})*N$, where f_{IN} is the resampler input rate and N is the phase accumulated per resampler input sample. N must be between 40000000000000h and FFFFFFFFFFFFFFh corresponding to decimations from 4 to $(1 + 2^{-56})$, respectively. Generally, however, a range of 80000000000000h to FFFFFFFFFFFFFFh (providing decimation from 2 to $(1 + 2^{-56})$, respectively) is sufficient for most applications since integer decimation can be done more efficiently in the preceding CIC and halfband filters. The resampler changes the sample rate by computing an output at each input which causes the NCO to roll over. If an output is to be computed, the nearest of the 32 available points from the polyphase structure is used. Because outputs are generated only on input samples which cause an NCO roll over, output samples will in general not be evenly spaced. The FIFO/TIMER block between the filter compute engine and the AGC is provided to improve output sample spacing for presentation to the serial data output formatter section (see IWA=*00Ah bits 11:0 description). If D/A converted directly, there would be artifacts from the uneven sample spacing, but if the samples are stored and reconstructed at the proper rate (the NCO rollover rate), the signal would have only the distortion produced by interpolation image leakage and the time quantization (phase jitter) due to the finite number of interpolation filter phases.

The polyphase filter has 192 coefficients implemented as 32 phases, each of which having 6 taps (6 x 32 = 192). These coefficients are provided in Table 50. The stopband attenuation of the filter is greater than 60dB, as shown in Figures 13 through 15. The signal to total image power ratio is approximately 55dB, due to the aliasing of the interpolation images. If the output is at least 2x the baud rate, the 32 interpolation phases yield an effective sample rate of 64x the baud rate or approximately 1.5% (1/64 resampler input sample period) maximum timing error.

AGC

The AGC Section provides gain to small signals, after the large signals and out-of-band noise have been filtered out, to ensure that small signals have sufficient bit resolution in the output formatter. The AGC can also be used to manually set the gain. The AGC optimizes the bit resolution for a variety of input amplitude signal levels. The AGC loop automatically adds gain to bring small signals from the lower bits of the 24-bit programmable FIR filter output into the range of 20-bit and shorter words in the output section. Without gain control, a signal at -72dBFS = $20\log_{10}(2^{-12})$ at the input would have only 4 bits of resolution at the output if a 16 bit word length were to be used (12 bits less than the full scale 16 bits). The potential increase in the bit resolution due to processing gain of the filters can be lost without the use of the AGC.

Figure 1 shows the Block Diagram for the AGC Section. The FIR filter data output is routed to the Cartesian to polar coordinate converter after passing through the AGC multipliers and shift registers. The magnitude output of the Cartesian to polar coordinate converter is routed through the AGC error detector, the AGC error scaler and into the AGC loop filter. This filtered error term is used to drive the AGC multiplier and shifters, completing the AGC control loop.

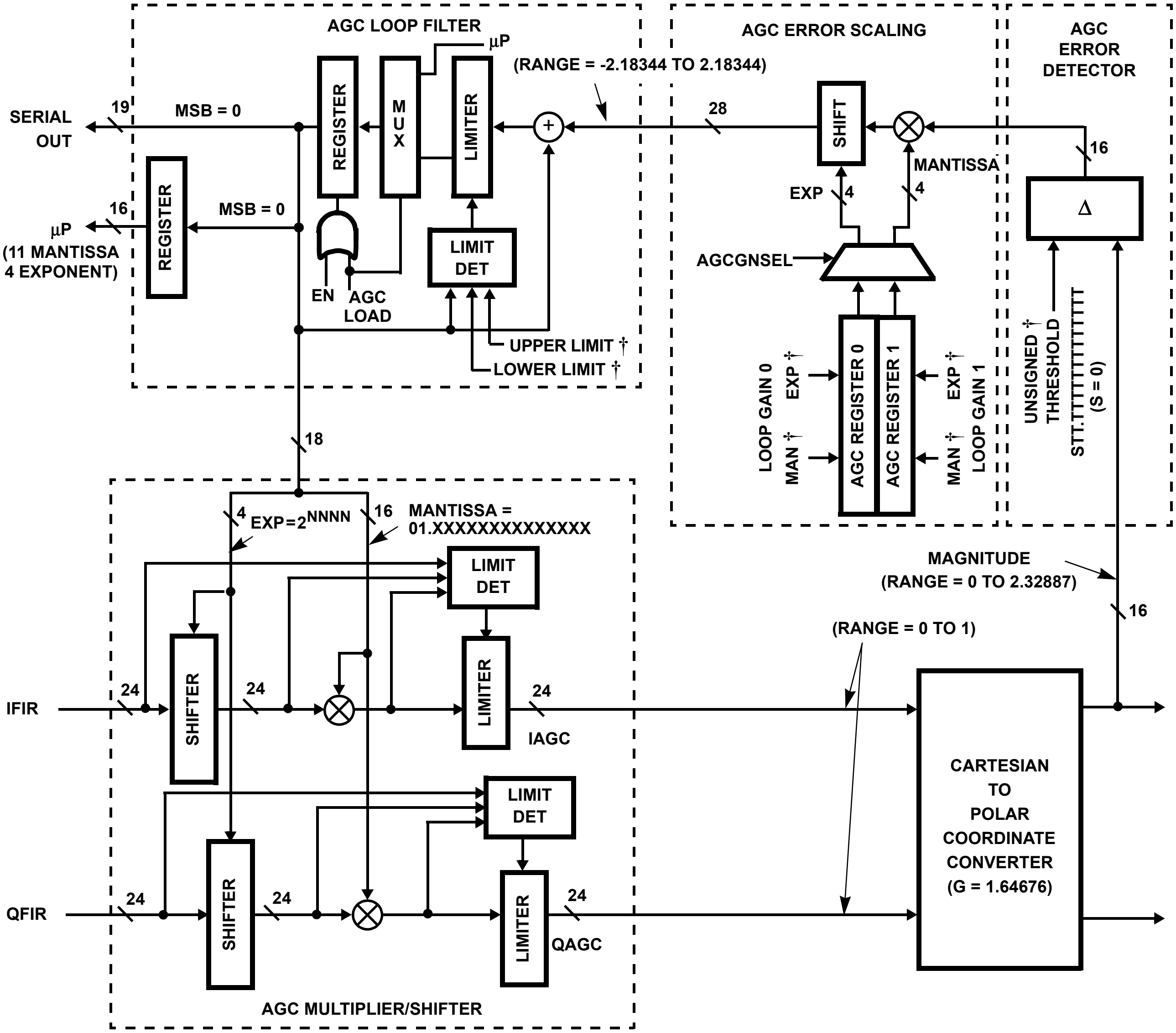
The AGC multiplier/shifter portion of the AGC is identified in Figure 1. The gain control from the AGC loop filter is sampled when new data enters the multiplier/shifter. The limit detector detects overflow in the shifter or the multiplier and saturates the output of I and Q data paths independently. The shifter has a gain from 0 to 90.31dB in 6.021dB steps, where 90.31dB = $20\log_{10}(2^{N})$ when N = 15. The mantissa provides up to an additional 6.02dB of gain. The gain in dB from the mantissa is:

$20\log_{10}[1 + (X)2^{-14}]$, where X is the fractional part of the mantissa interpreted as an unsigned integer ranging from 0 to $2^{14} - 1$.

Thus, the AGC multiplier/shifter transfer function is expressed as:

AGC Mult/Shift Gain = $2^{N}[1 + (X)2^{-14}]$

where N, the shifter exponent, has a range of 0 < N < 15 and X, the mantissa, has a range of $0 < X < (2^{14} -1)$.



† Controlled via microprocessor interface.

FIGURE 1. AGC FUNCTIONAL BLOCK DIAGRAM

In dB, this can be expressed as:

$$(\text{AGC Mult/Shift Gain})\text{dB} = 20\ \log_{10}(2^N[1 + (X)2^{-14}])$$

The full AGC range of the multiplier/shifter is from 0 dB to $20\log_{10}[1+(2^{14}-1)2^{-14}] + 20\log_{10}[2^{15}] = 96.329$ dB.

The 16 bit resolution of the mantissa provides a theoretical AM modulation level of -96dBc (depending on loop gain, settling mode and SNR). This effectively eliminates AM spurious caused by the AGC resolution.

The Cartesian to polar coordinate converter accepts I and Q data and generates magnitude and phase data. The magnitude output is determined by the equation:

$$|r| = 1.64676\sqrt{I^2 + Q^2}$$

where the magnitude limits are determined by the maximum I and Q signal levels into the Cartesian to polar converter. Taking fractional 2's complement representation, magnitude ranges from 0 to 2.329, where the maximum output is

$$|r| = 1.64676\sqrt{1^2 + 1^2} = 1.64676x1.414 = 2.329$$

The AGC loop feedback path consists of an error detector, error scaling, and an AGC loop filter. The error detector subtracts the magnitude output of the coordinate converter from the programmable AGC THRESHOLD value. The AGC THRESHOLD value is set in IWA register *012h and is equal to 1.64676 times the desired magnitude of the I1/Q1 output. Note that the MSB is always zero. The range of the AGC THRESHOLD value is 0 to +3.9999. The AGC Error Detector output has the identical range.

The loop gain register values adjust the response/settling time of the AGC loop. The loop gain is set in the AGC Error Scaling circuitry, using four values in two sets of programmable mantissa and exponent pairs (see IWA register *010h). Each set has both an attack and a decay gain. This allows asymmetric adjustment for applications such as VOX systems where the signal turns on and off. In these applications, the gains would be set for fast attack and slow decay so that the part decreases the gain quickly when the signal turns on, but increases the gain slowly when the signal turns off (in anticipation of it turning back on shortly).

For fixed gains, either set the upper and lower AGC limits to the same value, or set the limits to minimum and maximum gains and set the AGC attack and decay loop gains to zero.

The mantissa, M, is a 4-bit value which weights the loop filter input from 0.0 to $15/2^4 = 0.9375$. The exponent, E, defines a shift factor that provides additional weighting from 2^0 to 2^{-15}. Together the mantissa and exponent define the loop gain as given by,

AGC Loop Gain = $M_{LG}\ 2^{-4}\ 2^{-(15-E_{LG})}$

where M_{LG} is a 4-bit binary mantissa value ranging from 0 to 15, and E_{LG} is a 4-bit binary exponent value ranging from 0 to 15. The composite (shifter and multiplier) AGC scaling Gain range is from 0.0000 to $2.329(0.9375)2^0$ = 0.0000 to 2.18344. The scaled gain error can range (depending on threshold) from 0 to 2.18344, which maps to a “gain change per sample” range of 0 to 3.275dB/sample.

The AGC attack and decay gain mantissa and exponent values for loop gains 0 and 1 are programmed into IWA register *010h. The PDC provides for the storing of two values of AGC attack and decay scaling gains to allow for quick adjustment of the loop gain by simply setting IWA register *013h bits 9 and 10 accordingly. Possible applications include acquisition/tracking, no burst present/burst present, strong signal/weak signal, track/hold, or fast/slow AGC values.

The AGC loop filter consists of an accumulator with a built in limiting function. The maximum and minimum AGC gain limits are provided to keep the gain within a specified range and are programmed by 16-bit upper and lower limits using the following the equation:

AGC Gain Limit = $(1 + m_{AGC}\ 2^{-12})\ 2^e$

(AGC Gain Limit)dB = (6.02)(eeee) + 20 log(1.0+0.mmmm mmmm mmmm)

where m is a 12-bit mantissa value between 0 and 4095, and e is the 4-bit exponent ranging from 0 to 15. IWA register *011h Bits 31:16 are used for programming the upper limit, while bits 15:0 are used to program the lower limit. The format for these limit values are:

(31:16) or (15:0): E E E E M M M M M M M M M M M M

for a gain of 0 1. M M M M M M M M M M M M * $2^{E\ E\ E\ E}$

and the possible range of AGC limits from the previous equations is 0 to 96.328dB. The bit weightings for the AGC Loop Feedback elements are detailed in Table 51.

Using AGC loop gain, the AGC range, and expected error detector output, the gain adjustments per output sample for the loop filter section of the digital AGC can be given by

AGC Slew Rate = (1.5 dB) (THRESHOLD - (MAG * 1.64676)) x $(M_{LG})\ (2^{-4})\ (2^{-(15\ -\ E_{LG})})$

The loop gain determines the growth rate of the sum in the loop accumulator which, in turn, determines how quickly the AGC gain scales the output to the threshold value. Since the log of the gain response is roughly linear, the loop response can be approximated by multiplying the maximum AGC gain error by the loop gain. The expected range for the AGC rate is ~ 0.000106 to 3.275dB/output sample time for a threshold of 1/2 scale. For a full scale error, the minimum non-zero AGC slew rate would be approximately 0.0002dB/output or 20dB/sec at 100ksps. The maximum gain would be 6dB/output. This much gain, however, would probably result in significant AM on the output.

The maximum AGC Response is given by:

AGC Response_{Max} = (Input)(Cart/Polar Gain)(Error Det. Gain)(AGC Loop Gain)(AGC Output Weighting)

Since the AGC error is scaled to adjust the gain, the loop settles asymptotically to its final value. The loop settles to the mean of the signal. For example, if M_{LG} = 0101 and E_{LG} = 1100, the AGC Loop Gain = 0.3125 * 2^{-7}. The loop gain mantissas and exponents are set in IWA register *010h, with IWA register *013h selecting loop gain 0 or 1 and the settling mode.

In the HSP50216, a SYNCI signal will clear the AGC loop filter accumulator if GWA register F802h bit 27 is set.

The settling mode of the AGC forces either the mean or the median of the signal magnitude error to zero, as selected by IWA register *013h bit 8. For mean mode, the gain error is scaled and used to adjust the gain up or down. This proportional scaling mode causes the AGC to settle to the final gain value asymptotically. This AGC settling mode is preferred in many applications because the loop gain adjustments get smaller and smaller as the loop settles, reducing any AM distortion caused by the AGC.

With this AGC settling mode, the proportional gain error causes the loop to settle more slowly if the threshold is small. This is because the maximum value of the threshold minus the magnitude is smaller. Also, the settling can be asymmetric, where the loop may settle faster for “over range” signals than for “under range” signals (or vice versa).

In some applications, such as burst signals or TDMA signals, a very fast settling time and/or a more predictable settling time is desired. The AGC may be turned off or slowed down after an initial AGC settling period.

The median mode minimizes the settling time. This mode uses a fixed gain adjustment with only the direction of the adjustment controlled by the gain error. This makes the settling time independent of the signal level.

For example, if the loop is set to adjust 0.5dB per output sample, the loop gain can slew up or down by 16dB in 16 symbol times, assuming a 2 samples per symbol output sample rate. This is called a median settling mode because the loop settles to where there is an equal number of magnitude samples above and below the threshold. The disadvantage of this mode is that the loop will have a wander (dither) equal to the programmed step size. For this reason, it is advisable to set one loop gain for fast settling at the beginning of the burst and the second loop gain for small adjustments during tracking.

In the median mode, the maximum gain step is approximately 3dB/output. The step is fixed (it does not decrease as the error decreases) so a large gain will cause AM on the output at least that large. The gain should be lowered after the settling. The fixed gain step is set by the programmable AGC loop gain register IWA *010h.

For median mode, The AGC gain limits register sets the minimum and maximum limits on the AGC gain. The total AGC gain range is 96dB, but only a portion of the range should be needed for most applications. For example, with a 16-bit output to a processor, the 16 bits may be sufficient for all but 24dB of the total input range possible. The AGC would only need to have a range of 24dB. This allows faster settling and the AGC would be at its maximum gain limit except when a high power signal was received. The AGC may be disabled by setting both limits to the same value.

The median settling mode is enabled by setting IWA register *013h bit 8 to 0 while the mean loop settling mode is selected by setting bit 8 to 1.

Cartesian to Polar Converter

The Cartesian to Polar converter computes the magnitude and phase of the I/Q vector. The I and Q inputs are 24 bits. The converter phase output is 24 bits, MSB's routed to the output formatter and all 24 bits routed to the frequency discriminator. The 24-bit output phase can be interpreted either as two's complement (-0.5 to approximately 0.5) or unsigned (0.0 to approximately 1.0), as shown in Figure 2. The phase conversion gain is 1/2π. The phase resolution is 24 bits. The 24-bit magnitude is unsigned binary format with a range from 0 to 2.32. The magnitude conversion gain is 1.64676. The magnitude resolution is 24 bits. The MSB is always zero.

Table 1 details the phase and magnitude weighting for the 16 bits output from the PDC.

TABLE 1. MAG/PHASE BIT WEIGHTING

BIT	MAGNITUDE	PHASE (^{o})
23 (MSB)	2^2	180
22	2^1	90
21	2^0	45
20	2^{-1}	22.5
19	2^{-2}	11.25
18	2^{-3}	5.625
17	2^{-4}	2.8125
16	2^{-5}	1.40625
15	2^{-6}	0.703125
14	2^{-7}	0.3515625
13	2^{-8}	0.17578125
12	2^{-9}	0.087890625
11	2^{-10}	0.043945312
10	2^{-11}	0.021972656
9	2^{-12}	0.010986328
8	2^{-13}	0.005483164
7	2^{-14}	0.002741582
6	2^{-15}	0.001370791
5	2^{-16}	0.0006853955
4	2^{-17}	0.00034269775
3	2^{-18}	0.00017134887
2	2^{-19}	0.00008567444
1	2^{-20}	0.00004283722
0 (LSB)	2^{-21}	0.00002141861

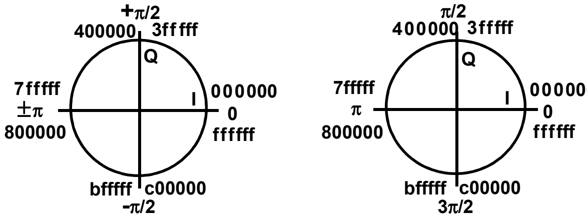


FIGURE 2. PHASE BIT MAPPING OF COORDINATE CONVERTER OUTPUT

The magnitude and phase computation requires 17 clocks for full precision. At the end of the 17 clocks, the magnitude and phase are latched into a register to be held for the next stage, either the output formatter or frequency discriminator. If a new input sample arrives before the end of the 17 cycles, the results of the computations up until that time, are latched. This latching means that an increase in speed causes only a decrease in resolution. Table 2 details the exact resolution that can be obtained with a fixed number of clock cycles up to the required 17. The input magnitude and phase errors induced by normal SNR values will almost always be worse than the Cartesian to Polar conversion.