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Electronic Telephone Line Switch

Features

- 350V breakdown voltage
- 18Ω maximum switch resistance
- Current limiting protection
- Operates at 2.3V input

Applications

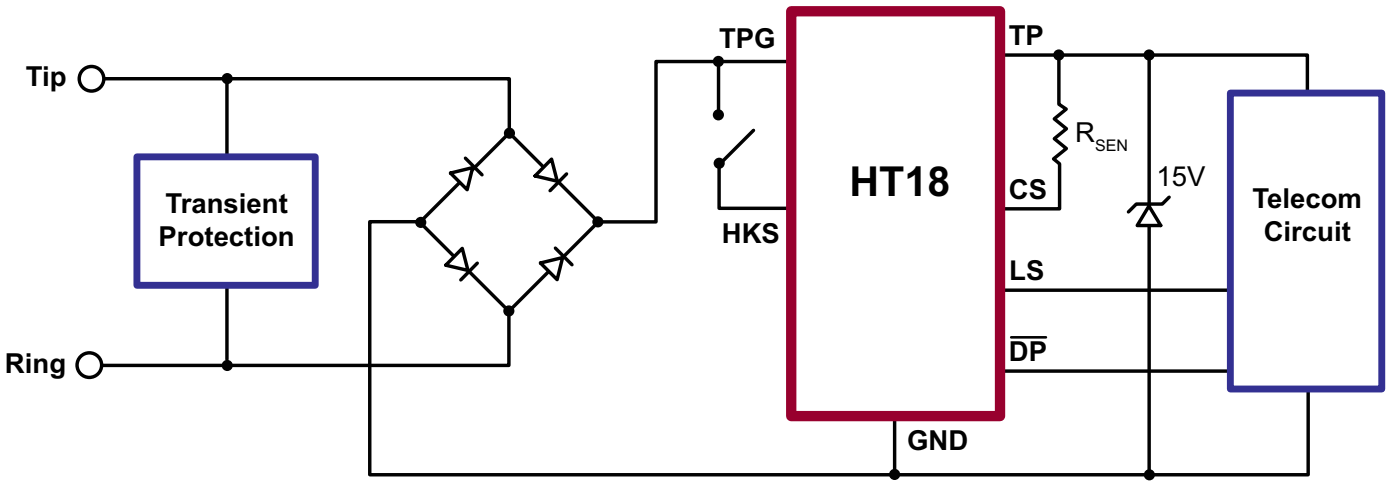
- Telephone handsets
- Modems
- Fax machines
- Answering machines
- Remote meter reading
- Telephone interface products

General Description

The Supertex HT18LG is an electronic line switch circuit that replaces the mechanical hook switch contact or a discrete hook switch in a telephone handset or modem. It switches the positive side of the telephone line using control inputs that are referenced to the negative side of the line. In its off state, it can withstand 350V on the positive input. In its on state, it has a maximum series resistance of 18Ω.

The device provides current limiting determined by an external resistor. There are three control inputs. The HKS pin turns on the hook switch when connected to the TPG pin. This can be accomplished by using a mechanical switch which closes when the handset is physically off-hook. The LS pin allows a logic signal to turn on the hook switch. The dial pulse, Pin 6, is used to turn the hook switch off for pulse dialing. The dial pulse ($\overline{DP}$) is active high.

Typical Application Circuit



Ordering Information

Part Number	Package	Packing
HT18LG-G	8-Lead SOIC (Narrow Body)	2500/Reel

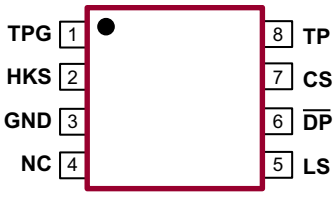
-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{TPG}, Input line voltage	+350V
V_{TP}, Output line voltage	+18V
$\overline{DP}$ continuous input voltage	+10V
Operating temperature range	0°C to +50°C
Storage temperature range	-65°C to +150°C
Power dissipation	0.8W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



8-Lead SOIC (Narrow Body)
(top view)

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (Narrow Body)

Typical Thermal Resistance

Package	θ_{ja}
8-Lead SOIC (Narrow Body)	101°C/W

Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

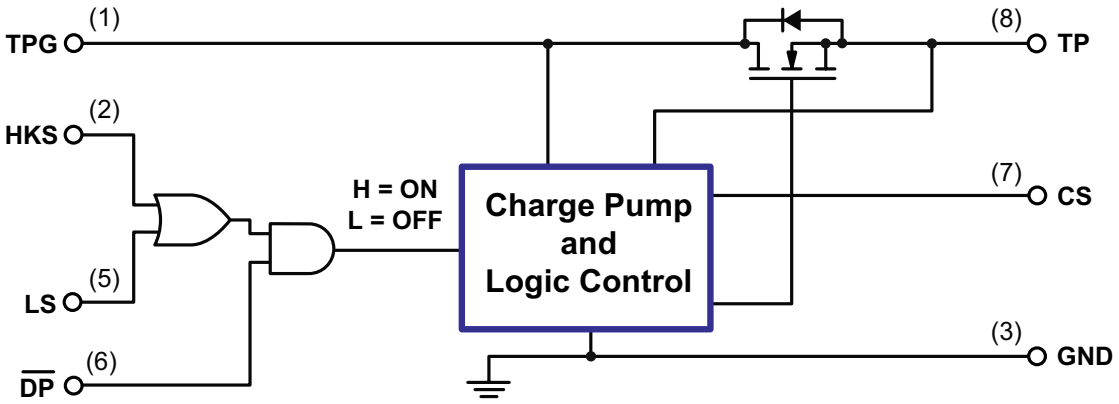
Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{TPG}	High voltage positive supply	-	-	350	V	I_{TPG} = 500µA, HKS, LS, $\overline{DP}$ = open circuit
I_{TPG}	Input leakage current	-	-	2.0	µA	V_{TPG} = 100V, HKS, LS, $\overline{DP}$ = open circuit
		-	-	200		V_{TPG} = 290V, HKS, LS, $\overline{DP}$ = open circuit
R_{SW}	TPG to TP switch resistance	-	-	18	Ω	V_{TPG} = 17V, I_{TPG} = 180mA, SW = on
		-	-	18		V_{TPG} = 3.0V, I_{TPG} = 20mA, SW = on
		-	-	30		V_{TPG} = 2.3V, I_{TPG} = 5.0mA, SW = on
I_{TPG} - I_{TP}	Bias current	-	-	75	µA	V_{TPG} = 5.0V, SW = on
		-	-	100		V_{TPG} = 10V, SW = on
I_{LIM}	I_{TPG} current limiting	188	250	330	mA	R_{EXT} = 200Ω ± 1%
I_{HKS}	HKS input current	-	-	200	µA	V_{HKS} = 40 to 70V
I_{LS}, I_{DP}	LS and $\overline{DP}$ logic input current	-	-	30	µA	V_{LS} = 3.0V, V_{DP} = 3.0V
$V_{IL(HKS)}$	HKS input low	0	-	0.2	V	V_{TPG} = 3.0 to 70V
$V_{IH(HKS)}$	HKS input high	2.0	-	V_{TPG}	V	V_{TPG} = 3.0 to 70V
$V_{IL(LS)}$,$V_{IL(DP)}$	Input logic low for $\overline{DP}$ and LS	0	-	0.2	V	V_{TPG} = 3.0 to 70V
$V_{IH(LS)}$,$V_{IH(DP)}$	Input logic high for $\overline{DP}$ and LS	1.5	-	10	V	V_{TPG} = 3.0 to 70V
T_{ON}	Turn-on time	-	-	1.0	ms	V_{TPG} = 4.5V
T_{OFF}	Turn-off time	-	-	1.0	ms	V_{TPG} = 4.5V

Logic Truth Table

HKS	LS	$\overline{DP}$	Switch State
H	L or Z	L or Z	ON
H	H	L or Z	ON
L or Z	L or Z	L or Z	OFF
L or Z	H	L or Z	ON
X	X	H	OFF

Z = high impedance, open circuit
X = irrelevant
L = logic level low
H = logic level high

Block Diagram

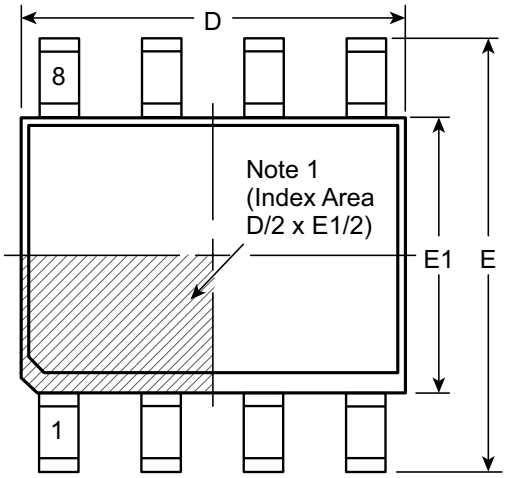


Pin Description

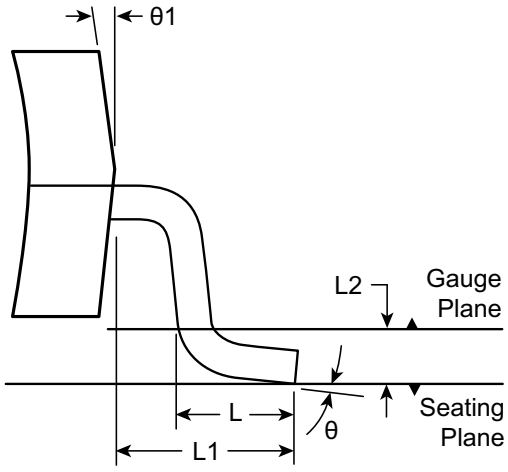
Pin	Name	Description
1	TPG	Positive input side of a telephone line, typically tip side.
2	HKS	Hookswitch input. Connect HKS to TPG to turn on the hook switch. Internally pulled low with a high value resistor.
3	GND	Device ground. Negative side of a telephone line, typically ring side.
4	NC	No connect. Open circuit. No internal connections to the device.
5	LS	Line switch input. Input logic high turns on the hook switch. Internally pulled low with a high value resistor.
6	$\overline{DP}$	Dial pulse input. Input logic high turns off the hook switch. Used for pulse dialing. Internally pulled low with a high value resistor.
7	CS	Current sense input. An external resistor connected between CS and TP sets the current limit.
8	TP	Positive output side of a telephone line. Zener protection to prevent this output from rising above 18V is required.

8-Lead SOIC (Narrow Body) Package Outline (LG)

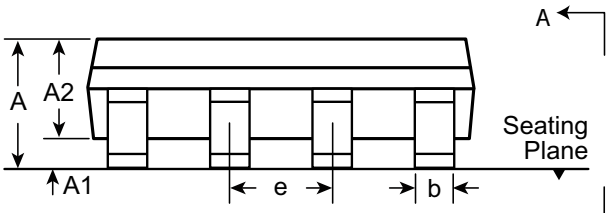
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



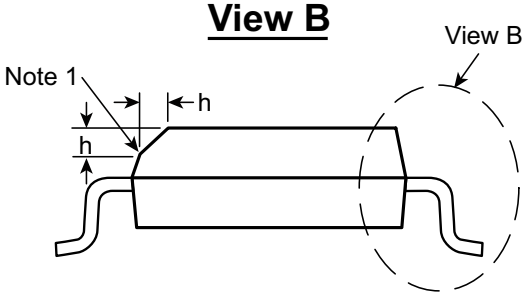
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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