Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

HITAG µ

ISO 18000 transponder IC

Rev. 3.0 — 18 March 2010
184430

Product data sheet
PUBLIC

1. General description

The HITAG product line is well known and established in the contactless identification market.

Due to the open marketing strategy of NXP Semiconductors there are various manufacturers well established for both the transponders/cards as well as the read/write devices. All of them supporting HITAG 1, HITAG 2 and HITAG S transponder ICs.

With the new HITAG µ family, this existing infrastructure is extended with the next generation of ICs being substantially smaller in mechanical size, lower in cost, offering more operation distance and speed, but still being operated with the same reader infrastructure and transponder manufacturing equipment.

The protocol and command structure for HITAG µ ISO 18000 is design to support Reader Talks First (RTF) operation, including anti-collision algorithm.

2. Features and benefits

2.1 Features

- Integrated circuit for contactless identification transponders and cards
- Integrated resonance capacitor of 210 pF with ± 3% tolerance or 280 pF with ± 5% tolerance over full production
- Frequency range 100 kHz to 150 kHz

2.2 Protocol

- Modulation read/write device → transponder: 100 % ASK and binary pulse length coding
- Modulation transponder → read/write device: Strong ASK modulation with anti-collision, Manchester coding
- Fast anti-collision protocol
- Data integrity check (CRC)
- Reader Talks First (RTF) Mode
- Data rate read/write device to transponder: 5.2 kbit/s
- Data rates transponder to read/write device: 4 kbit/s

2.3 Memory

- 1760 bit
- Up to 10 000 erase/write cycles
- 10 years non-volatile data retention
- Memory Lock functionality
- 32-bit password feature

2.4 Supported standards

- Full compliant to ISO 18000-2

2.5 Security features

- 48-bit Unique Item Identification (UII)

2.6 Delivery types

- Sawn, gold-bumped 8” wafer
- HVSON2
- SOT-1122

3. Applications

- Industrial applications
- Casino gambling

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Name	Description	Type	Version
HTMS1301FUG/AM	Wafer	sawn, megabumped wafer, 150 µm, 8 inch, UV	HITAG µ ISO 18000, 210pF	-
HTMS8301FUG/AM	Wafer	sawn, megabumped wafer, 150 µm, 8 inch, UV	HITAG µ ISO 18000, 280pF	-
HTMS1301FTB/AF	XSON3	plastic extremely thin small outline package; no leads; 4 terminals; body 1 x 1.45 x 0.5 mm	HITAG µ ISO 18000, 210pF	SOT1122
HTMS8301FTB/AF	XSON3	plastic extremely thin small outline package; no leads; 4 terminals; body 1 x 1.45 x 0.5 mm	HITAG µ ISO 18000, 280pF	SOT1122
HTMS1301FTK/AF	HVSON2	plastic thermal enhanced very thin small outline package; no leads; 2 terminals; body 3 x 2 x 0.85 mm	HITAG µ ISO 18000, 210pF	SOT899-1
HTMS8301FTK/AF	HVSON2	plastic thermal enhanced very thin small outline package; no leads; 2 terminals; body 3 x 2 x 0.85 mm	HITAG µ ISO 18000, 280pF	SOT899-1

5. Block diagram

The HITAG µ ISO 18000 transponder IC require no external power supply. The contactless interface generates the power supply and the system clock via the resonant circuitry by inductive coupling to the read/write device (RWD). The interface also demodulates data transmitted from the RWD to the HITAG µ ISO 18000 transponder IC, and modulates the magnetic field for data transmission from the HITAG µ ISO 18000 transponder IC to the RWD.

Data are stored in a non-volatile memory (EEPROM). The EEPROM has a capacity of 1760 bit and is organized in blocks.

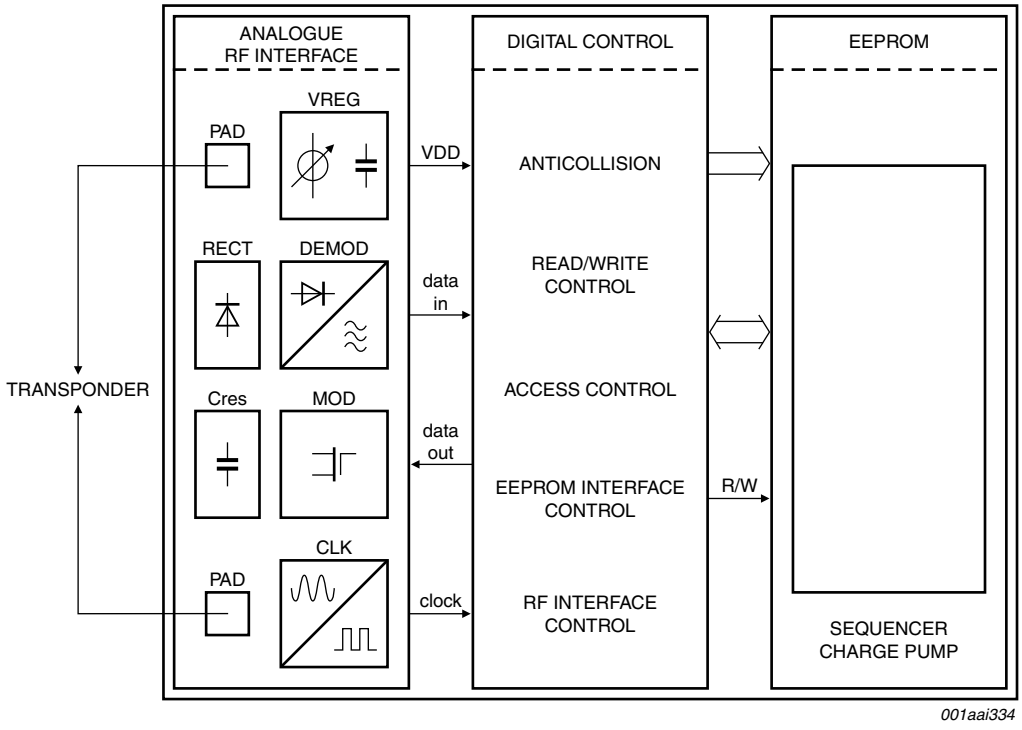

Fig 1. Block diagram of HITAG µ ISO 18000 transponder IC

6. Pinning information

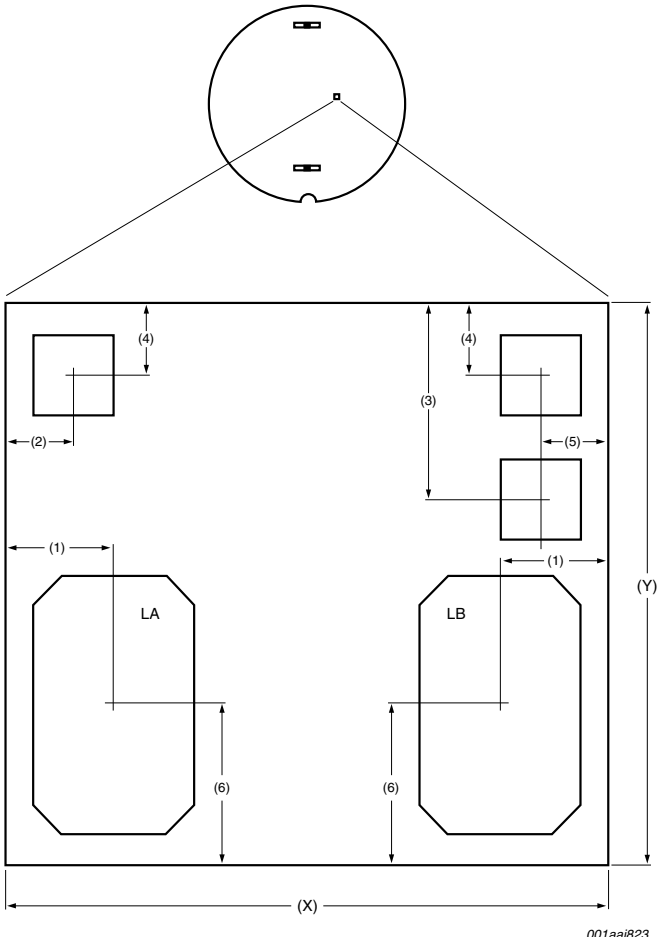

Fig 2. HITAG µ ISO 1800 - Mega bumps bondpad locations

Table 2. HITAG µ ISO 18000 - Mega bumps dimensions

Description	Dimension
(X) chip size	550 µm
(Y) chip size	550 µm
(1) pad center to chip edge	100.5 µm
(2) pad center to chip edge	48.708 µm
(3) pad center to chip edge	180.5 µm
(4) pad center to chip edge	55.5 µm
(5) pad center to chip edge	48.508 µm
(6) pad center to chip edge	165.5 µm
Bump Size:	
LA, LB	294 x 164 µm
Remaining pads	60 x 60 µm

Note: All pads except LA and LB are electrically disconnected after dicing.

7. Mechanical specification

7.1 Wafer specification

See Ref. 2 “General specification for 8” wafer on UV-tape with electronic fail die marking”.

7.1.1 Wafer

- Designation: each wafer is scribed with batch number and wafer number
- Diameter: 200 mm (8”)
- Thickness: 150 µm ± 15 µm
- Process: CMOS 0.14 µm
- Batch size: 25 wafers
- PGDW: 91981

7.1.2 Wafer backside

- Material: Si
- Treatment: ground and stress release
- Roughness: R_a max. 0.5 µm, R_t max. 5 µm

7.1.3 Chip dimensions

- Die size without scribe: 550 µm x 550 µm = 302500 μm^2
- Scribe line width:
  X-dimension: 15 µm (scribe line width is measured between nitride edges)
  Y-dimension: 15 µm (scribe line width is measured between nitride edges)
- Number of pads: 5

7.1.4 Passivation on front

- Type: sandwich structure
- Material: PE-Nitride (on top)
- Thickness: 1.75 µm total thickness of passivation

7.1.5 Au bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 µm
- Bump height uniformity:
  - within a die: ± 2 µm
  - within a wafer: ± 3 µm
  - wafer to wafer: ± 4 µm
- Bump flatness: ± 1.5 µm
- Bump size:
  - LA, LB: 294 x 164 µm
  - TEST, GND, VDD: 60 x 60 µm
  - Bump size variation: ± 5 µm
- Under bump metallization: sputtered TiW

7.1.6 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See Ref. 2 “General specification for 8” wafer on UV-tape with electronic fail die marking”.

7.1.7 Map file distribution

See Ref. 2 “General specification for 8” wafer on UV-tape with electronic fail die marking”.

8. Functional description

8.1 Memory organization

The EEPROM has a capacity of 1760 bit and is organized in blocks of 4 bytes each (1 block = 32 bits). A block is the smallest access unit.

The HITAG µ ISO 18000 transponder IC memory organization is shown in Table 3 “Memory organization”.

For permanent lock of blocks please refer to Section 14.8 “LOCK BLOCK”.

8.1.1 Memory organization

Table 3. Memory organization

Block address	Content	Password Access
FFh	User Config	
FEh	PWD	
36h 35h ... 14h 13h 12h 11h 10h	User Memory	bit6=0 bit5=0 R/W[2] bit6=0 bit5=1 RO[1] bit6=1 bit5=0 R/W(P)[3] bit6=1 bit5=1 R/W(P)[3]
0Fh 0Eh 0Dh 0Ch 0Bh 0Ah 09h 08h 07h 06h 05h 04h 03h 02h 01h 00h	User Memory	bit4=0 R/W[2] bit4=1 RO[1] bit3=0 R/W[2] bit3=1 RO[1]

[1] RO: Read without password, write with password

[2] R/W: Read and write without password

[3] R/W(P): Read and write with password

8.2 Memory configuration

The User Configuration Bock consists of one configurable byte (Byte0) and three reserved bytes (Byte1 to Byte3)

The bits in the User Configuration Block enable a customized memory configuration of the HITAG µ ISO 18000 transponder ICs.

Three areas (1 to 127bit, 1 to 511 bits and upper memory) can be restricted to read/write access.

The User Configuration Block (User Config) is programmable by using WRITE SINGLE BLOCK command at address FFh. Bits 7 to 31 (Byte1 to Byte3) are reserved for further usage.

The user configuration block (block address FFh) and the password block (block address FEh) can be locked with the LOCK BLOCK command.

Attention: The lock of the blocks is permanently and therefore irreversible!

Table 4. User configuration block to Byte0

Byte0							Description
bit6	bit5	bit4	bit3	bit2	bit1	bit 0	Bit-no.
PWD (r/w) [2] Bit512… Max	PWD (w) [1] Bit512… Max	PWD (w) [1] Bit128… 511	PWD (w) [1] Bit0… 127	RFU	RFU	RFU	
							Value/meaning

[1] PWD(w)=1: read without password and write with password

[2] PWD(r/w)=1: read and write with password

9. General requirements

The HITAG µ ISO 18000 transponder IC is compatible with the ISO 18000-2 standard.

At the time a HITAG µ ISO 18000 based transponder is in the interrogator field it doesn't respond until it receives a request from the RWD.

All communication from reader to HITAG µ ISO 18000 transponder ICs and vice versa and the CRC error detection bits (if applicable) are transmitted starting with LSB first.

In the case that multiple HITAG µ ISO 18000 based transponders are in the interrogation field which cause collisions the RWD has to start the anticollision procedure as described in this document.

10. HITAG µ ISO 18000 transponder IC air interface

10.1 Downlink communication signal interface - RWD to HITAG µ ISO 18000 transponder IC

10.1.1 Modulation parameters

Communications between RWD and HITAG µ ISO 18000 transponder IC takes place using ASK modulation with a modulation index of m > 90%.

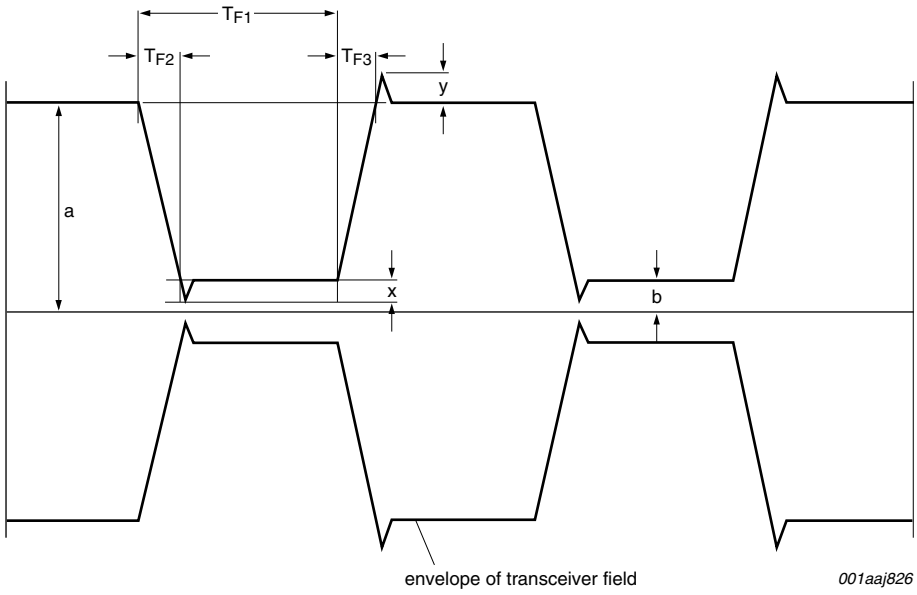

Fig 3. Modulation details of data transmission from RWD to HITAG µ transponder IC

Table 5. Modulation coding times[1][2]

Symbol	Min	Max
m = (a-b)/(a+b)	90%	100%
T_{F1}	$4 \times T_c$	$10 \times T_c$
T_{F2}	0	$0.5 \times T_{F1}$
T_{F3}	0	$0.5 \times T_{Fd0}$
x	0	$0.05 \times a$
y	0	$0.05 \times a$

[1] $T_{Fd0} > T_{F1} + T_{F3} + 3 \times T_c$

[2] $T_{C...}$Carrier period time ($1/_{125kHz}$ = 8 µs nominal)

10.1.2 Data rate and data coding

The RWD to HITAG µ ISO 18000 transponder IC communication uses Pulse Interval Encoding. The RWD creates pulses by switching the carrier off as described in Figure 4. The time between the falling edges of the pulses determines either the value of the data bit ’0’, the data bit ’1’, a code violation or a stop condition.

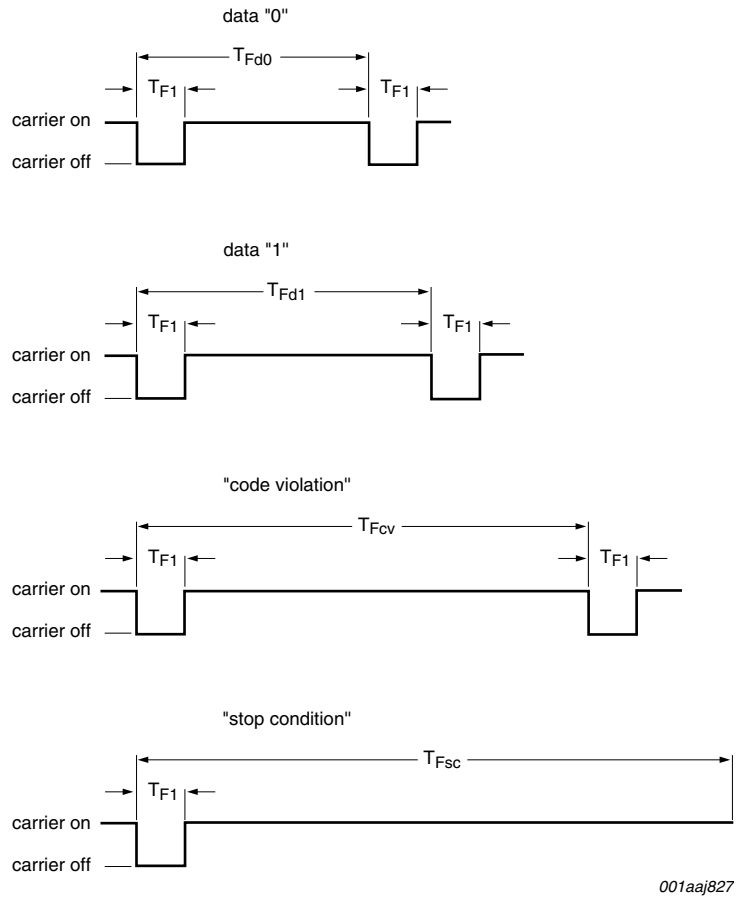

Fig 4. Reader to HITAG µ ISO 18000 transponder IC: Pulse Interval Encoding

Assuming equal distributed data bits ’0’ and ’1’, the data rate is in the range of about 5.2 kbit/s.

Table 6. Data coding times [1]

Meaning	Symbol	Min	Max
Carrier off time	T_{F1}	$4 \times T_c$	$10 \times T_c$
Data “0” time	T_{Fd0}	$18 \times T_c$	$22 \times T_c$
Data “1” time	T_{Fd1}	$26 \times T_c$	$30 \times T_c$
Code violation time	T_{Fcv}	$34 \times T_c$	$38 \times T_c$
Stop condition time	T_{Fsc}	$\geq 42 \times T_c$	n/a

[1] $T_{C...}$ Carrier period time ($1/_{125kHz}$ = 8 µs nominal)

10.1.3 RWD - Start of frame pattern

A RWD request always starts with a SOF pattern for ease of synchronization. The SOF pattern consists of an encoded data bit ’0’ and a ’code violation’.

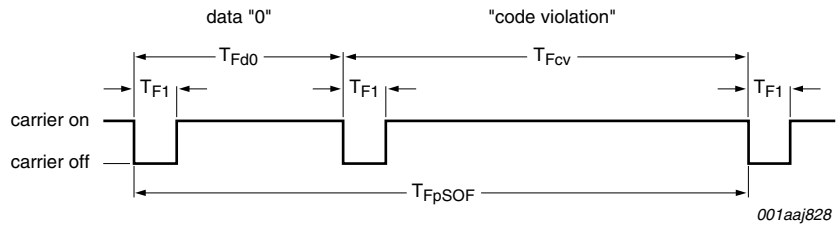

Fig 5. Start of frame pattern

The HITAG µ ISO 18000 transponder IC shall be ready to receive a SOF from the RWD within 1.2 ms after having sent a response to the RWD.

The HITAG µ ISO 18000 transponder IC shall be ready to receive a SOF from the RWD within 2.5 ms after the RWD has established the powering field.

10.1.4 RWD - End of frame pattern

For slot switching during a multi-slot anticollision sequence, the RWD request is an EOF pattern. The EOF pattern is represented by a RWD ’Stop condition’.

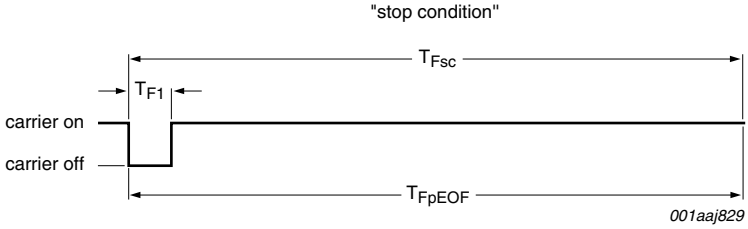

Fig 6. End of frame pattern

10.2 Communication signal interface - HITAG µ ISO 18000 transponder IC to RWD

10.2.1 Data rate and data coding

The HITAG µ ISO 18000 transponder IC accepts the following data rate and encoding scheme:

- $1/T_{Fd}$ Manchester coded data signal on the response to the HITAG µ ISO 18000 transponder IC
- $1/(2 \times T_{Fd})$ dual pattern data coding when responding within the inventory process

$T_{Fd} = 32 / f_c = 32 \times T_c$

Remark: The slower data rate used during the inventory process allows for improving the collision detection when several HITAG µ ISO 18000 transponder ICs are present in the RWD field, especially if some transponder ICs are in the near field and others in the far field.

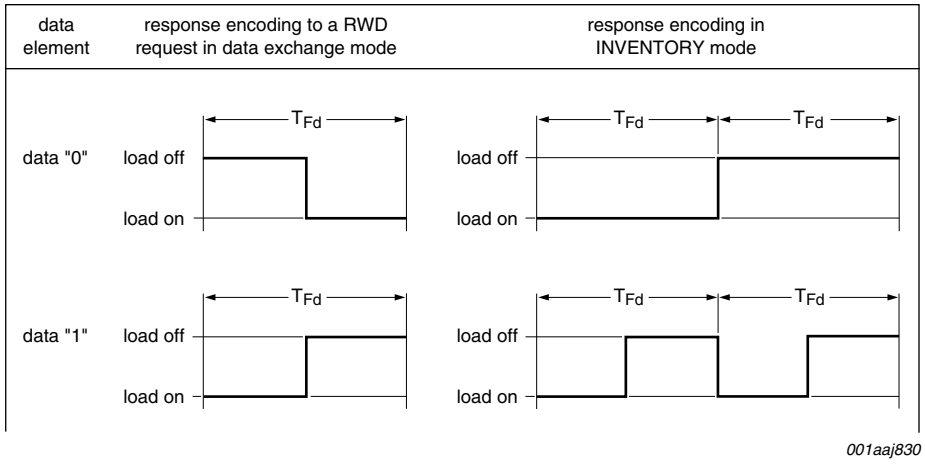

Fig 7. HITAG µ ISO 18000 transponder IC - Load modulation coding

10.2.2 Start of frame pattern

The HITAG µ ISO 18000 transponder IC response always starts with a SOF pattern. The SOF is a Manchester encoded bit sequence of ’110’.

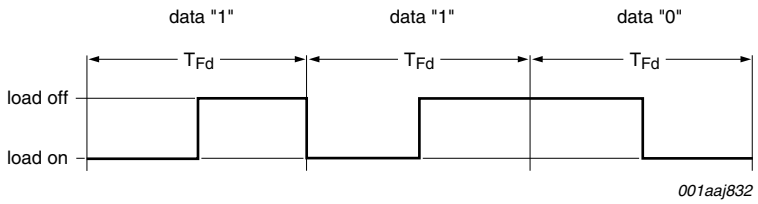

Fig 8. Start of fame pattern

10.2.3 End of frame pattern

A specific EOF pattern is neither used nor specified for the HITAG µ ISO 18000 transponder IC response. An EOF is detected by the RWD if there is no load modulation for more than two data bit periods (T_{Fd}).

11. General protocol timing specification

For requests where an EEPROM erase and/or programming operation is required, the transponder IC returns its response when it has completed the write/lock operation. This will be latest after 20 ms upon detection of the last falling edge of the RWD request or after the RWD has switched off the field.

11.1 Waiting time before transmitting a response after an EOF from the RWD

When the HITAG µ ISO 18000 transponder IC has detected an EOF of a valid RWD request or when this EOF is in the normal sequence of a valid RWD request, it shall wait for T_{Fp1} before starting to transmit its response to a RWD request or when switching to the next slot in an inventory process.

T_{Fp1} starts from the detection of the falling edge of the EOF received from the RWD.

Remark: The synchronization on the falling edge from the RWD to the EOF of the HITAG µ ISO 18000 transponder IC is necessary to ensure the required synchronization of the response.

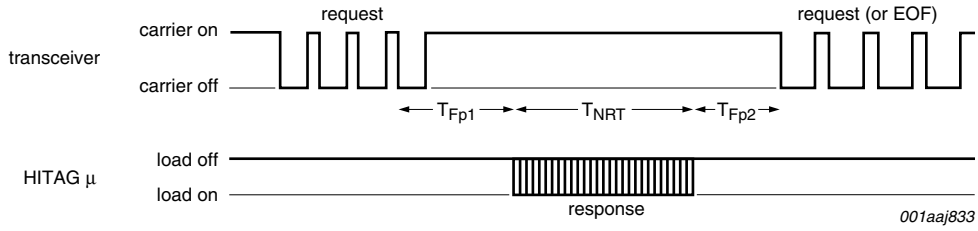

Fig 9. General protocol timing diagram

The minimum value of T_{Fp1} is $T_{Fp1min} = 204 \times T_C$

The typical value of T_{Fp1} is $T_{Fp1typ} = 209 \times T_C$

The maximum value of T_{Fp1} is $T_{Fp1max} = 213 \times T_C$

If the HITAG µ ISO 18000 transponder IC detects a carrier modulation during this time (T_{Fp1}), it shall reset its T_{Fp1}-timer and wait for a further time (T_{Fp1}) before starting to transmit its response to a RWD request or to switch to the next slot when in an inventory process.

11.2 RWD waiting time before sending a subsequent request

- When the RWD has received a HITAG µ ISO 18000 response to a previous request other than inventory or quiet, it needs to wait T_{Fp2} before sending a subsequent request. T_{Fp2} starts from the time the last bit has been received from the HITAG µ ISO 18000.
- When the RWD has sent a quiet request, it needs to wait T_{Fp2} before sending a subsequent request. T_{Fp2} starts from the end of the quiet request's EOF (falling edge of EOF pulse + 42 × T_C). This results in a waiting time of (150 × T_C + 42 × T_C) before the next request.

The minimum value of T_{Fp2} is T_{Fp2min} = 150 × T_C ensures that the HITAG µ ISO 18000 ICs are ready to receive a subsequent request.

Remark: The RWD needs to wait at least 2.5 ms after it has activated the electromagnetic field before sending the first request, to ensure that the HITAG µ ISO 18000 transponder ICs are ready to receive a request.

- When the RWD has sent an inventory request, it is in an inventory process.

11.3 RWD waiting time before switching to next inventory slot

An inventory process is started when the RWD sends an inventory request. For a detailed explanation of the inventory process refer to Section 14.3 and Section 14.4.

To switch to the next slot, the RWD sends an EOF after waiting a time period specified in the following sub-clauses.

11.3.1 RWD started to receive one or more HITAG µ ISO 18000 transponder IC responses

During an inventory process, when the RWD has started to receive one or more HITAG µ a ISO 18000 transponder IC responses (i.e. it has detected a transponder IC SOF and/or a collision), it shall

- wait for the complete reception of the HITAG µ ISO 18000 transponder IC responses (i.e. when a last bit has been received or when the nominal response time T_{NRT} has elapsed),
- wait an additional time T_{Fp2} and then send an EOF to switch to the next slot, if a 16 slot anticollision request is processed, or send a subsequent request (which could be again an inventory request).

T_{Fp2} starts from the time the last bit has been received from the HITAG µ ISO 18000 transponder IC.

The minimum value of T_{Fp2} is T_{Fp2min} = 150 × T_C.

T_{NRT} is dependant on the anticollisions current mask value and on the setting of the CRCT flag.

11.3.2 RWD receives no HITAG µ ISO 18000 transponder IC response

During an inventory process, when the RWD has received no HITAG µ ISO 18000 transponder IC response, it needs to wait T_{Fp3} before sending a subsequent EOF to switch to the next slot, if a 16 slot anticollision request is processed, or sending a subsequent request (which could be again an inventory request).

T_{Fp3} starts from the time the RWD has generated the falling edge of the last sent EOF.

The minimum value of T_{Fp3} is $T_{Fp3min} = T_{Fp1max} + T_{FpSOF}$.

T_{FpSOF} is the time duration for a HITAG µ ISO 18000 transponder IC to transmit an SOF to the RWD.

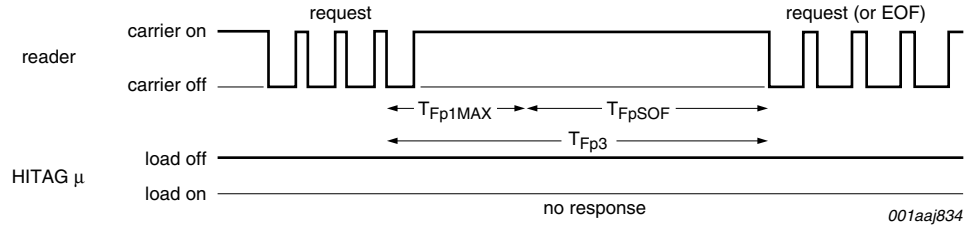

Fig 10. Protocol timing diagram without HITAG µ ISO 18000 transponder IC response

Table 7. Overview timing parameters [1]

Symbol	Min	Max
T_{FpSOF}	$3 \times T_{Fd}$	$3 \times T_{Fd}$
T_{Fp1}	$204 \times T_C$	$213 \times T_C$
T_{Fp2}	$150 \times T_C$	-
T_{Fp3}	$T_{Fp1max} + T_{FpSOF}$	-

[1] $T_{C...}$ Carrier period time ($1/_{125kHz}$ = 8 µs nominal)

12. State diagram

12.1 General description of states

RF Off

The powering magnetic field is switched off or the HITAG µ ISO 18000 transponder IC is out of the field.

READY

The HITAG µ ISO 18000 transponder IC enters this state when it is activated by the RWD.

SELECTED

The HITAG µ ISO 18000 transponder IC enters the Selected state after receiving the SELECT command with a matching UII. In the Selected state the respective commands with SEL=1 are valid only for selected transponder.

Only one HITAG µ transponder IC should be in the selected state at one time. If one transponder is selected and a second transponder receives the SELECT Command, the first transponder will automatically change to Quiet state.

QUIET

The HITAG µ ISO 18000 transponder IC enters this state after receiving a STAY QUIET command or when he was in selected state and receives a SELECT command addressed to another transponder.

In this state, the HITAG µ transponder IC reacts to any request commandos where the ADR flag is set.

Remark:

In case of an invalid command the transponder will remain in his actual state.

12.2 State diagram HITAG µ ISO 18000

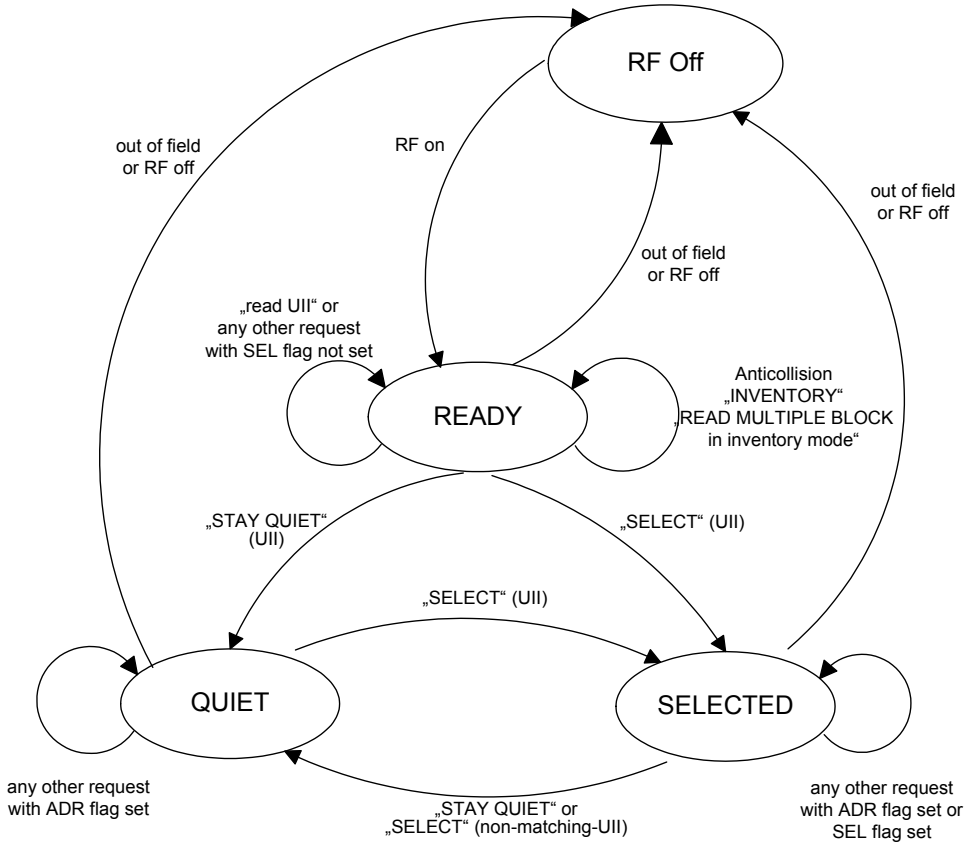

Fig 11. State diagram of HITAG µ ISO18000 transponder ICs

13. Modes

13.1 Anticollision

The RWD is the master of the communication with one or multiple transponder ICs. It starts the anticollision sequence by issuing the inventory request (see Section 14.3). Within the RWD command the NOS flag must be set to the desired setting (1 or 16 slots) and add the mask length and the mask value after the command field.

The mask length n indicates the number of significant bits of the mask value. It can have any value between 0 and 44 when 16 slots are used and any value between 0 and 48 when 1 slot is used.

The next two subsections summarize the actions done by the transponder IC during an inventory round.

13.1.1 Anticollision with 1 slot

The transponder IC will receive one ore more inventory commands with NOS = '1'. Every time the transponder ICs fractional or whole UII matches the mask value of RWD's request it responses with remaining UII without mask value.

Transponder ICs responses are modulated by dual pattern data coding as described in Section 10.2.

13.1.2 Anticollision with 16 slots

The transponder IC will receive several inventory commands with NOS = '0' defining an amount of 16 slots. Within the request there is the mask specified by length and value (sent LSB first).

In case of mask length = '0' the four least significant bits of transponder ICs UII become the starting value of transponder IC's slot counter.

In case of mask length ≠ '0' the received fractional mask is compared to transponder IC's UII. If it matches the starting value for transponder IC's slot number will be calculated. Starting at last significant bit of the sent mask the next four less significant bits of UII are used for this value. At the same time transponder IC's slot counter is reset to '0'.

Now the RWD begins its anticollision algorithm. Every time the transponder IC receives an EOF it increments slot-counter. Now if mask value and slot-counter value are matching the transponder IC responses with the remaining UII without mask value but with slot number

In case of collision within one slot the RWD changes the mask value and starts again running its algorithm.

14. Command set

The first part of this section (Section 14.1) describes the flags used in every RWD command. The following subsections (Section 14.3 until Section 14.11) explain all implemented commands and their suitable transponder IC responses which are done with tables showing the command itself and suitable responses.

Within tables flags, parameter bits and parts of a response written in braces are optional. That means if the suitable flag is set resulting transponder IC's action will be performed according to Section 14.1.

Every command is embedded in SOF and EOF pattern. As described in Table 8 and Table 9 sending and receiving data is done with the least significant bit of every field on first position.

Important information:

In this document the fields (i.e. command codes) are written with most significant bit first.

Table 8. Reader - Transponder IC transmission [1][2]

SOF	Flags	Commands	Parameters	Data	CRC-16	EOF
-	5	6	var.	var.	(16)	-
-	LSB ... MSB	LSB ... MSB	LSB ... MSB	LSB ... MSB	LSB ... MSB	-

[1] Values in braces are optional.

[2] Data is sent with least significant bit first.

Table 9. Transponder IC - Reader transmission [1][2]

SOF	Error flag	Data/Error code	CRC-16	EOF
-	1	var.	(16)	-
-	-	LSB ... MSB	LSB ... MSB	-

[1] Values in braces are optional.

[2] Data is sent with least significant bit first.

14.1 Flags

Every request command contains five flags which are sent in order Bit 1 (LSB) to Bit 5 (MSB). The specific meaning depends on the context.

Table 10. Command Flags

Bit	Flag	Full name	Value	Description
1	PEXT	Protocol EXTension	0	No protocol format extension
			1	RFU
2	INV	INVentory	0	Flag 4 and Flag 5 are 'SEL' and 'ADR' Flag
			1	Flag 4 and Flag 5 are 'RFU' and 'NOS' Flag
3	CRCT	CRC-Transponder	0	Transponder IC respond without CRC
			1	Transponder IC respond contains CRC
4	SEL (INV==0)	SELect		in combination with ADR (see Table 12)
5	ADR (INV==0)	ADdRess		in combination with SEL (see Table 12)
4	AFI (INV==1)	Reserved for future use	0	AFI field is not present
			1	AFI field is present
5	NOS (INV==1)		0	16 slots while performing anti-collision
			1	1 slot while performing anti-collision

Table 11. Command Flags - Bit order

	MSB bit5	bit4	bit3	bit2	LSB bit1
INV==0	ADR	SEL	CRCT	INV	PEXT
INV==1	NOS	AFI	CRCT	INV	PEXT

Table 12. Meaning of ADR and SEL flag

ADR	SEL	Meaning
0	0	Request without UII, all transponder ICs in READY state shall respond
1	0	Request contains UII, one transponder IC (with corresponding UII) shall respond
0	1	Request without UII, the transponder IC in SELECTED state shall respond
1	1	Reserved for future use

14.2 Error handling

In case an error has been occurred the transponder IC responses with the set error flag and the three bit code ’111’ (meaning ’unknown error’).

The general response format in case of an error response is shown in Table 13 whereas commands not supporting error responses are excluded. In case of an unsupported command there will be no response. The format is embedded into SOF and EOF.

Table 13. Response format in error case

Error flag	Error code	CRC-16	Description
1	3	(16)	No. of bits
1	111		

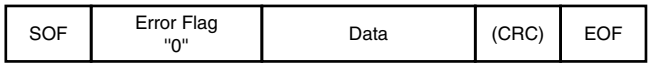

Fig 12. HITAG µ ISO 18000 transponder IC response - in case of no error

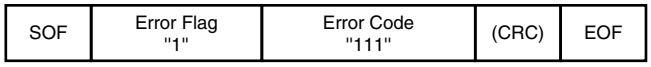

Fig 13. HITAG µ ISO 18000 transponder IC response - in error case

14.3 INVENTORY

Upon reception of this command without error, all transponder ICs in the ready state shall perform the anticollision sequence. The inventory (INV) flag shall be set to '1'. The NOS flag determines whether 1 or 16 slots are used.
If AFI flag is set to ’1’ the transponder handles the request as error.

If a transponder IC detects any error, it shall remain silent.

Table 14. INVENTORY - Request format (00h)

Flags	Command	Mask length	Mask value	CRC-16	Description
5	6	6	n	(16)	No. of bits
10(1)10	000000	0 ≤ n ≤ UII length	UII Mask		AC with 1 timeslot
00(1)10	000000	0 ≤ n ≤ UII length	UII Mask		AC with 16 timeslot

Table 15. Response to a successful INVENTORY request [1][2]

Error Flag	Data	CRC-16	Description
1	48 - n	(16)	No. of bits
0	Remaining UII without mask value		

[1] Error and CRC are Manchester coded, UII is dual pattern coded.

[2] Response within the according time slot.

Error Flag set to ’0’ indicates no error.

14.4 STAY QUIET

Upon reception of this command without error, a transponder IC in either ready state or selected state enters the quiet state and shall not send back a response.

The STAY QUIET command with both SEL and ADR flag set to '0' or both set to '1' is not allowed.

There is no response to the STAY QUIET request, even if the transponder detects an error.

Table 16. STAY QUIET - request format(01h)

Flags	Command	Data	CRC-16	Description
5	6	(48)	(16)	No. of bits:
01(1)00	000001	-		without UII
10(1)00	000001	UII		with UII

14.5 READ UII

Upon reception of this command without error all transponder ICs in the ready state are sending their UII.

The addressed (ADR), the select (SEL), the inventory (INV) and the (PEXT) flag are set to '0'.

Table 17. READ UII - request format (02h)

Flags	Command	CRC-16	Description
5	6	(16)	No. of bits
00(1)00	000010		

Table 18. Response to a successful READ UII request

Error flag	Data	CRC-16	Description
1	48	(16)	No. of bits
0	UII		

Error flag set to ’0’ indicates no error.

14.6 READ MULTIPLE BLOCK

Upon reception of this command without error, the transponder reads the requested block(s) and sends back their value in the response. The blocks are numbered from 0 to 255.

The number of blocks in the request is one less than the number of blocks that the transponder returns in its response i.e. a value of '6' in the 'Number of blocks' field requests to read 7 blocks. A value '0' requests to read a single block.

Table 19. READ MULTIPLE BLOCKS - request format (12h)

Flags	Command	Data 1	Data 2	Data 3	CRC-16	Description
5	6	(48)	8	8	(16)	No. of bits
00(1)00	010010	-	First block number	Number of blocks		without UII in READY state
10(1)00	010010	UII	First block number	Number of blocks		with UII
01(1)00	010010	-	First block number	Number of blocks		without UII in SELECTED state

Table 20. Response to a successful READ MULTIPLE BLOCKS request

Error Flag	Data	CRC-16	Description
1	32 x Number of blocks	(16)	No. of bits
0	User memory block data		

Error Flag set to '0' indicates no error.