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HTMS1x01; HTMS8x01

HITAG µ transponder IC

Rev. 3.4 — 21 May 2015
152934

Product data sheet
COMPANY PUBLIC

1. General description

The HITAG product line is well known and established in the contactless identification market.

Due to the open marketing strategy of NXP Semiconductors there are various manufacturers well established for both the transponders/cards as well as the read/write devices. All of them supporting HITAG 1, HITAG 2 and HITAG S transponder ICs.

With the new HITAG µ family, this existing infrastructure is extended with the next generation of ICs being substantially smaller in mechanical size, lower in cost, offering more operation distance and speed, but still being operated with the same reader infrastructure and transponder manufacturing equipment.

The protocol and command structure for HITAG µ is design to support Reader Talks First (RTF) operation, including anti-collision algorithm.

Different memory sizes are offered and can be operated using exactly the same protocol.

1.1 Target markets

1.1.1 Animal identification

The ISO standards ISO 11784 and ISO 11785 are well established in this market and HITAG µ is especially designed to deliver the optimum performance compliant to these standards. The HITAG µ advanced ICs are offering additional memory for storage of customized offline data like further breeding details.

1.1.2 Laundry automation

- Identify 200 pcs of garment with one read/write device
- Long operation distance with typical small shaped laundry button transponders
- Insensitive to harsh conditions like pressure, heat and water

1.1.3 Beer keg and gas cylinder logistic

- Recognizing a complete pallet of gas cylinders at one time
- Long writing distance
- Voluntarily change between TTF Mode with user defined data length and read/write modes without changing the configuration on the transponder
- Authenticity check at the beer pubs - between beer bumper and supplied beer keg, provides a safe protection of the beer brand

1.1.4 Brand protection

- Authenticity check for high level brands or for original refilling e.g. toner for fax machines.

2. Features and benefits

2.1 Features

- Integrated circuit for contactless identification transponders and cards
- Integrated resonance capacitor of 210 pF with ±3 % tolerance or 280 pF with ±5 % tolerance over full production
- Frequency range 100 kHz to 150 kHz

2.2 Protocol

- Modulation read/write device → transponder: 100 % ASK and binary pulse length coding
- Modulation transponder → read/write device: Strong ASK modulation with anti-collision, Manchester and Biphase coding
- Fast anti-collision protocol
- Cyclic Redundancy Check (CRC)
- Transponder Talks First (TTF) mode
- Temporary switch from Transponder Talks First into Reader Talks First (RTF) Mode
- Data rate read/write device to transponder: 5.2 kbit/s
- Data rates transponder to read/write device: 2 kbit/s, 4 kbit/s, 8 kbit/s

2.3 Memory

- Different memory options
- Up to 10000 erase/write cycles
- 10 years non-volatile data retention
- Memory Lock functionality
- 32-bit password feature

2.4 Supported standards

- Full compliant to ISO 11784 and ISO 11785 Animal ID
- Designed to support ISO/IEC 14223 Animal ID with anticollision and read/write functionality

2.5 Security features

- 48-bit Unique Identification Number (UID)

2.6 Delivery types

- Sawn, gold-bumped 8” wafer
- HVSON2
- SOT-1122

3. Applications

- Animal identification
- Laundry automation
- Beer keg and gas cylinder logistic
- Brand protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Wafer EEPROM characteristics							
t_{ret}	retention time	$T_{amb} \leq 55$ °C		10	-	-	year
$N_{endu(W)}$	write endurance			100000	-	-	cycle
Interface characteristics							
C_i	input capacitance	between LA and LB					
		HTMS1x01	[1][2]	203.7	210	216.3	pF
		HTMS8x01	[1][3]	266	280	294	pF

[1] Measured with an HP4285A LCR meter at 125 kHz/room temperature (25 °C); $V_{IN1-IN2}$ = 0.5 V (RMS)

[2] Integrated Resonance Capacitor: 210 pF ± 3 %

[3] Integrated Resonance Capacitor: 280 pF ± 5 %

5. Ordering information

Table 2. Ordering information

Type number	Package			
	Name	Description	Type	Version
HTMS1001FUG/AM	Wafer	sawn, megabumped wafer, 150 µm, 8 inch, UV	HITAG µ, 210 pF	-
HTMS8001FUG/AM	Wafer	sawn, megabumped wafer, 150 µm, 8 inch, UV	HITAG µ, 280pF	-
HTMS8101FUG/AM	Wafer	sawn, megabumped wafer, 150 µm, 8 inch, UV	HITAG µ Advanced, 280 pF	-
HTMS8201FUG/AM	Wafer	sawn, megabumped wafer, 150 µm, 8 inch, UV	HITAG µ Advanced+, 280 pF	-
HTMS8001FTB/AF	XSON3	plastic extremely thin small outline package; no leads; 4 terminals; body 1 × 1.45 × 0.5 mm	HITAG µ, 280 pF	SOT1122
HTMS8101FTB/AF	XSON3	plastic extremely thin small outline package; no leads; 4 terminals; body 1 × 1.45 × 0.5 mm	HITAG µ Advanced, 280 pF	SOT1122
HTMS8201FTB/AF	XSON3	plastic extremely thin small outline package; no leads; 4 terminals; body 1 × 1.45 × 0.5 mm	HITAG µ Advanced+, 280 pF	SOT1122
HTMS8001FTK/AF	HVSON2	plastic thermal enhanced very thin small outline package; no leads; 2 terminals; body 3 × 2 × 0.85 mm	HITAG µ, 280 pF	SOT899-1
HTMS8101FTK/AF	HVSON2	plastic thermal enhanced very thin small outline package; no leads; 2 terminals; body 3 × 2 × 0.85 mm	HITAG µ Advanced, 280 pF	SOT899-1
HTMS8201FTK/AF	HVSON2	plastic thermal enhanced very thin small outline package; no leads; 2 terminals; body 3 × 2 × 0.85 mm	HITAG µ Advanced+, 280 pF	SOT899-1

6. Block diagram

The HITAG µ transponder ICs require no external power supply. The contactless interface generates the power supply and the system clock via the resonant circuitry by inductive coupling to the Read/Write Device (RWD). The interface also demodulates data transmitted from the RWD to the HITAG µ transponder IC, and modulates the magnetic field for data transmission from the HITAG µ transponder IC to the RWD.

Data are stored in a non-volatile memory (EEPROM). The EEPROM has a capacity of up to 1760 bit and is organized in blocks.

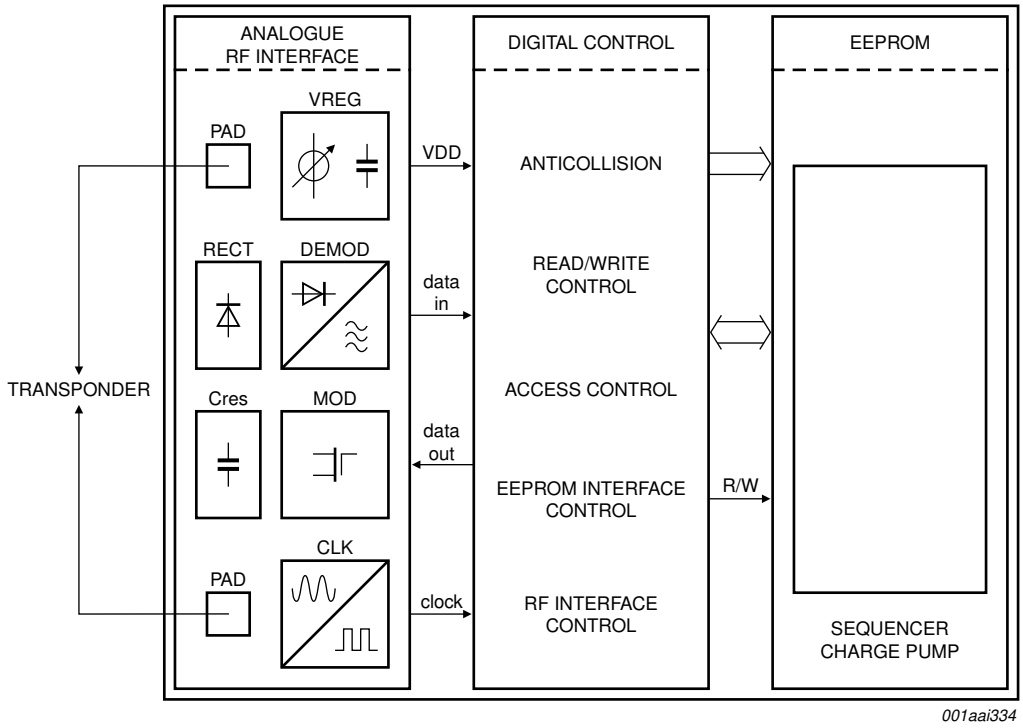

Fig 1. Block diagram of HITAG µ transponder IC

7. Pinning information

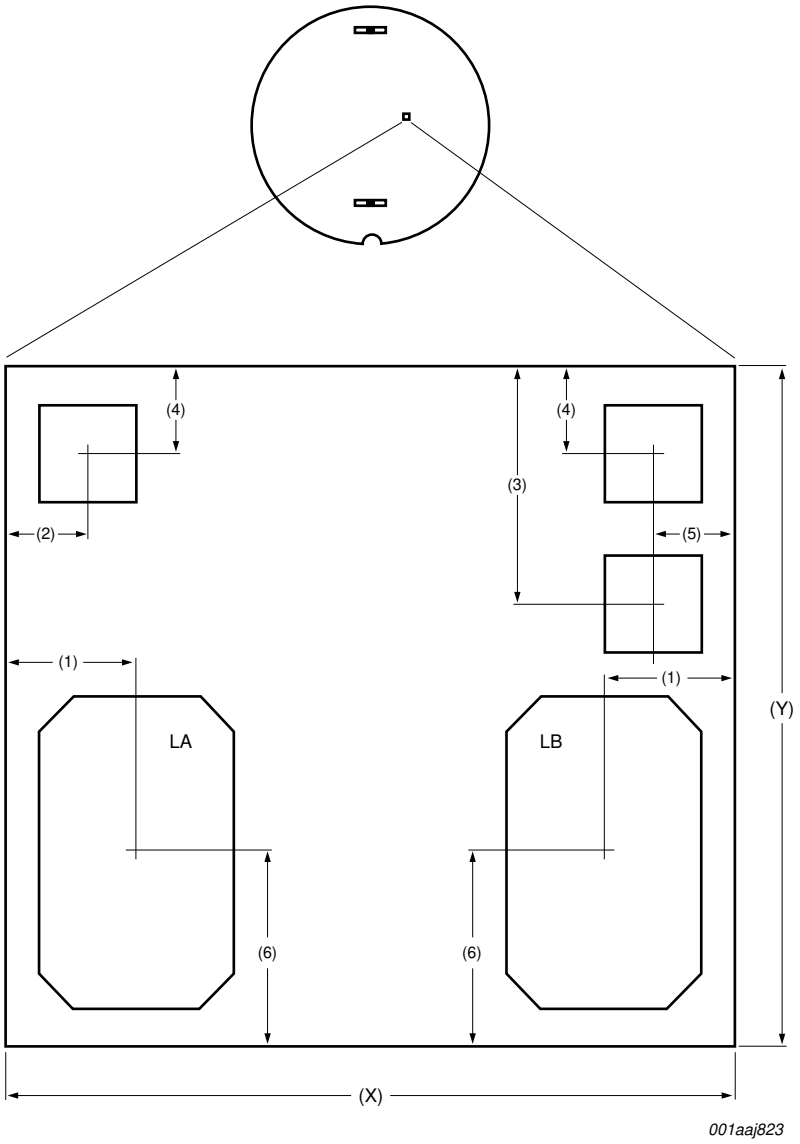

Fig 2. HITAG µ - Mega bumps bondpad locations

Table 3. HITAG µ - Mega bumps dimensions

Description	Dimension
(X) chip size	550 µm
(Y) chip size	550 µm
(1) pad center to chip edge	100.5 µm
(2) pad center to chip edge	48.708 µm
(3) pad center to chip edge	180.5 µm
(4) pad center to chip edge	55.5 µm
(5) pad center to chip edge	48.508 µm

Table 3. HITAG µ - Mega bumps dimensions

Description	Dimension
(6) pad center to chip edge	165.5 µm
Bump Size:	
LA, LB	294 x 164 µm
Remaining pads	60 x 60 µm

Note: All pads except LA and LB are electrically disconnected after dicing.

8. Mechanical specification

8.1 Wafer specification

See Ref. 2 “General specification for 8” wafer on UV-tape with electronic fail die marking”.

Table 4. Wafer specification

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	200 mm (8 inches)
Thickness	150 µm ± 15 µm
Process	CMOS 0.14 µm
Batch size	25 wafers
PGDW	91981
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size without scribe	550 µm x 550 µm = 302500 $µm^2$
Scribe line width	
X-dimension	15 µm (scribe line width measured between nitride edges)
Y-dimension	15 µm (scribe line width measured between nitride edges)
Number of pads	5
Passivation on front	
Type	sandwich structure
Material	PE-nitride (on top)
Thickness	1.75 µm total thickness of passivation
Au bump	
Material	>99.9 % pure Au
Hardness	35 HV to 80 HV 0.005
Shear strength	>70 MPa
Height	18 µm
Height uniformity	
within a die	±2 µm
within a wafer	±3 µm
wafer to wafer	±4 µm
Bump flatness	±1.5 µm
Bump size	
LA, LB	294 µm × 164 µm
TEST, GND, VDD	60 µm × 60 µm
variation	±5 µm
Under bump metallization	sputtered TiW

8.1.1 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See Ref. 2 “General specification for 8” wafer on UV-tape with electronic fail die marking”.

8.1.2 Map file distribution

See Ref. 2 “General specification for 8” wafer on UV-tape with electronic fail die marking”.

9. Functional description

9.1 Memory organization

The EEPROM has a capacity of up to 1760 bit and is organized in blocks of 4 bytes each (1 block = 32 bits). A block is the smallest access unit.

The HITAG μ transponder IC is available with different memory sizes as shown in Table 5 “Memory organization HITAG m (128-bit)”, Table 6 “Memory organization HITAG μ Advanced (512 bit)” and Table 7 “Memory organization HITAG μ Advanced+ (1760 bit)”.

For permanent lock of blocks please refer to Section 14.9 “LOCK BLOCK”.

9.1.1 Memory organization HITAG μ transponder ICs

Table 5. Memory organization HITAG μ (128-bit)

Block address	Content	Password Access
FFh	User Config	bit3=0 R/W[2] bit3=1 RO[1]
FEh	PWD	
03h	ISO 11784/ISO 11785 128 bit TTF data	
02h		
01h		
00h		

[1] RO: Read without password, write with password

[2] R/W: Read and write without password

9.1.2 Memory organization HITAG µ Advanced

Table 6. Memory organization HITAG µ Advanced (512 bit)

Block address	Content	Password Access
FFh	User Config	
FEh	PWD	
0Fh 0Eh 0Dh 0Ch 0Bh 0Ah 09h 08h 07h 06h 05h 04h	User Memory	bit4=0 R/W[2] bit4=1 RO[1]
03h 02h 01h 00h	ISO 11784/ISO 11785 128-bit TTF data	bit3=0 R/W[2] bit3=1 RO[1]

[1] RO: Read without password, write with password

[2] R/W: Read and write without password

9.1.3 Memory organization HITAG µ Advanced +

Table 7. Memory organization HITAG µ Advanced+ (1760 bit)

Block address	Content	Password Access
FFh	User Config	
FEh	PWD	
36h 35h ... 14h 13h 12h 11h 10h	User Memory	bit6=0 bit5=0 R/W[2] bit6=0 bit5=1 RO[1] bit6=1 bit5=0 R/W(P)[3] bit6=1 bit5=1 R/W(P)[3]
0Fh 0Eh 0Dh 0Ch 0Bh 0Ah 09h 08h 07h 06h 05h 04h	User Memory	bit4=0 R/W[2] bit4=1 RO[1]
03h 02h 01h 00h	ISO 11784/ISO 11785 128-bit TTF data	bit3=0 R/W[2] bit3=1 RO[1]

[1] RO: Read without password, write with password

[2] R/W: Read and write without password

[3] R/W(P): Read and write with password

9.2 Memory configuration

The user configuration block consists of one configurable byte (Byte0) and three reserved bytes (Byte1 to Byte3)

The bits in the user configuration block enable a customized configuration of the HITAG µ transponder ICs. In TTF mode the user can choose Bi-phase or Manchester encoding and also the data rate for the return link (bit0 to bit2). In RTF mode data rate and coding are fixed with 4 kbit/s Manchester encoding.

Fitting to ISO 11785 standard the default values are set for 4 kbit/s Bi-Phase encoding. The next four bits (bit 3 to bit 6) are used for password settings.

Three areas (TTF area(128bit), lower 512 bits and upper memory) can be restricted to read/write access.

The user configuration block (User Config) is programmable by using WRITE SINGLE BLOCK command at address FFh. Bits 7 to 31 (Byte1 to Byte3) are reserved for further usage.

The user configuration block (block address FFh) and the password block (block address FEh) can be locked with the LOCK BLOCK command.

Attention:

- Pre-programmed default values are not locked !
- Configuration block has to be locked to make data unalterable!
- The lock of the blocks is permanently and therefore irreversible!

Table 8. User configuration block to Byte0

Byte0						Description
bit6	bit5	bit4	bit3	bit2	bit1 ... 0	Bit-no.
PWD (r/w) [2] Bit512… Max	PWD (w) [1] Bit512… Max	PWD (w) [1] Bit128… 511	PWD (w) [1] Bit0… 127	Encoding	Data rate	
				0… MCH 1… Bi-Ph.	’00’… 2kbit/s ’01’… 4kbit/s ’10’… 8kbit/s	Value/meaning

[1] PWD(w)=1: read without password and write with password

[2] PWD(r/w)=1: read and write with password

10. General requirements

The HITAG µ transponder ICs are compatible with ISO 11785. At the time a HITAG µ transponder IC is in the interrogator field it will respond according to ISO 11785.

A HITAG µ advanced/advanced+ can be identified as a transponder being in the data exchange mode (advanced mode) by the type information in the reserved bit field sent to the RWD.

- Bit 15 of the ISO 11784 frame shall be set to '1' indicating that this is an HITAG µ advanced/advanced+ in data exchange mode.
- Bit 16 of the ISO 11784 frame (additional data flag set to '1', indicating that the HITAG µ advanced/advanced+ in data exchange mode contains additional data in the user memory area.

To bring the HITAG µ transponder ICs into the data exchange mode, the RWD needs to send a valid request or a valid switch command within the defined listening window.

A HITAG µ transponder IC in data exchange mode only responds when requested by the RWD (RTF mode).

The identification code, all communication from reader to HITAG µ transponder ICs and vice versa and the CRC error detection bits (if applicable) are transmitted starting with LSB first.

In the case that multiple HITAG µ advanced/advanced+ in data exchange mode are in the interrogation field which cause collisions the RWD has to start the anticollision procedure as described in this document. Depending in which part of the ISO 11785 timing frame the collision is detected the RWD will start with the anticollision request.

The HITAG µ transponder IC in data exchange mode switches back to the standard ISO 11785 mode when it :

- is no longer in the interrogation field
- has terminated the data exchange mode operations and the interrogation field was switched off for at least 5 ms afterwards

11. HITAG µ transponder IC air interface

11.1 Downlink description

To transfer the HITAG µ transponder ICs into the data exchange mode, the RWD's interrogation field needs be switched off. After this off-period, the interrogation field is switched on again, and either the SOF at the start of a valid request or the special switch command needs to be sent to the HITAG µ transponder IC within the specified switch time window. The HITAG µ transponder IC switches itself into the data exchange mode upon reception of any of the switch commands. In this mode, the HITAG µ transponder IC respond when requested by the RWD (reader driven protocol).

The HITAG µ transponder IC in data exchange mode switches back to the ISO 11785 mode after the interrogation field has been switched off for at least 5 ms.

The steps necessary to transfer the HITAG µ transponder IC into the data exchange mode are shown in Figure 3. The downlink communication takes place in period C and D. The example in Figure 3 shows two data blocks (#1 and #2) being selected by the RWD, which then are transmitted by the HITAG µ transponder IC.

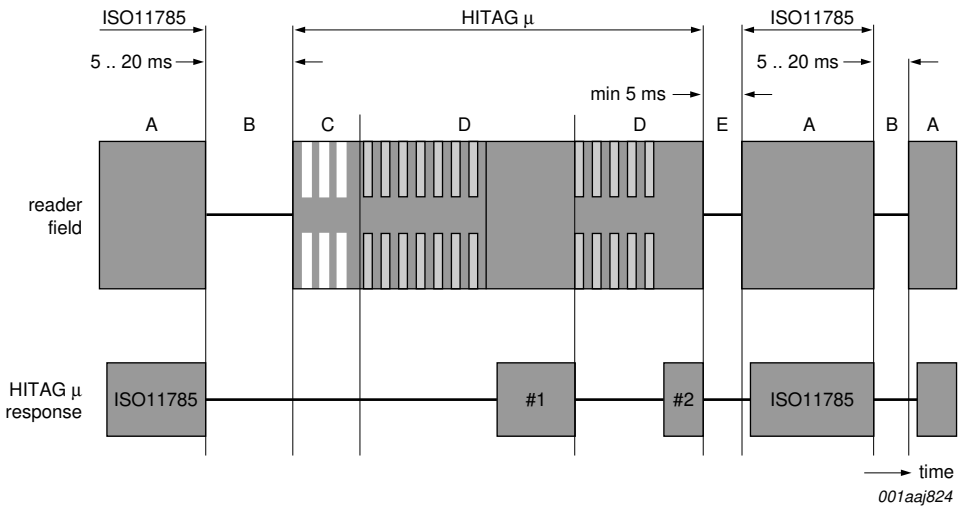

Fig 3. RF interface for HITAG µ

Table 9. RF interface for HITAG µ

Cycle A:	The RWD reads the ISO 11785 frame.
Cycle B:	The RWD switches off the interrogation field for at least 5 ms in order to reset the HITAG µ transponder IC.
Cycle C:	The RWD sends either the SOF at the start of a valid request or the SWITCH command to the HITAG µ transponder IC in order to put it into the data exchange mode. Any of these has to be issued within the switch window after reset - as defined in Section 11.2 “Mode switching protocol”
Cycle D:	Read/Write (for HITAG µ transponder ICs) or Inventory (HITAG µ advanced/advanced+ transponder ICs) operation in the data exchange mode.
Cycle E:	After all operations are finished or the HITAG µ transponder IC left the antenna field, the RWD switches off the field for at least 5 ms in order to poll for new incoming HITAG µ or HITAG µ advanced/advanced+.

11.2 Mode switching protocol

After powering the HITAG µ transponder IC switches to the data exchange mode after receiving one of the two possible switch commands from the RWD during the specified switch window (see Table 10 and Figure 4 for details).

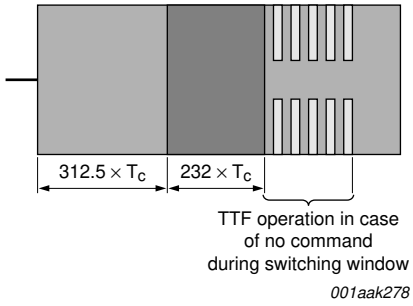

Fig 4. Switching window timing

Table 10. HITAG µ transponder IC air interface parameters [1]

Parameter	Description
Interrogation field modulation	Amplitude modulation (ASK), 90 - 100%
Encoding	Pulse Interval Encoding; Least Significant Bit (LSB) first
Bit rate	5.2 kbit/s typically
Mode switching	Either a specific 5 bit switch command or the detection of the SOF as part of a valid HITAG µ transponder IC command, transmitted after the interruption of the interrogation field for at least 5 ms
Mode switch timing	HITAG µ transponder IC settling time: 312.5 × T_C switch command window after HITAG µ transponder IC settling: 232.5 × T_C All within cycle C in Figure 3.
Mode switch command	00011 or SOF sequence

[1] T_C...Carrier period time ($1/134.2$ kHz = 7.45 µs nominal)

The RWD sends either the SOF at the start of a valid request or a special switch command to the HITAG µ (as shown in Figure 5) in order to transfer it into the data exchange mode.

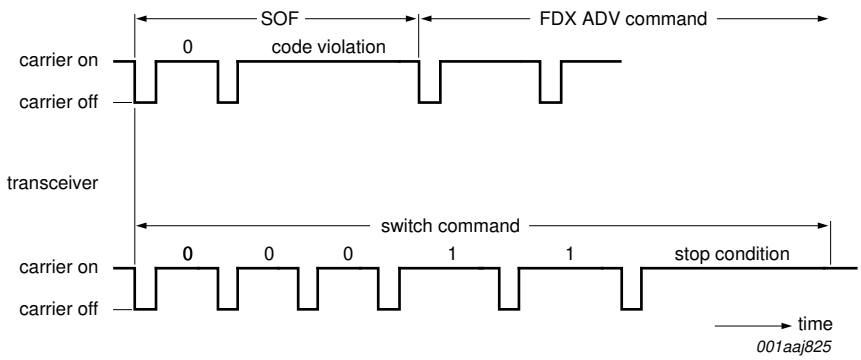

Fig 5. Reader downlink modulation for SWITCH command

11.2.1 SWITCH

Setting the transponder into data exchange mode (advanced mode) is done by sending SOF pattern or the switch command within the listening window (232.5 x T_C). The SWITCH command itself does not contain SOF and EOF.

Table 11. SWITCH Command

Command	Description
5	No. of bits
00011	

11.3 Downlink communication signal interface - RWD to HITAG µ transponder IC

11.3.1 Modulation parameters

Communications between RWD and HITAG µ transponder IC takes place using ASK modulation with a modulation index of m > 90%.

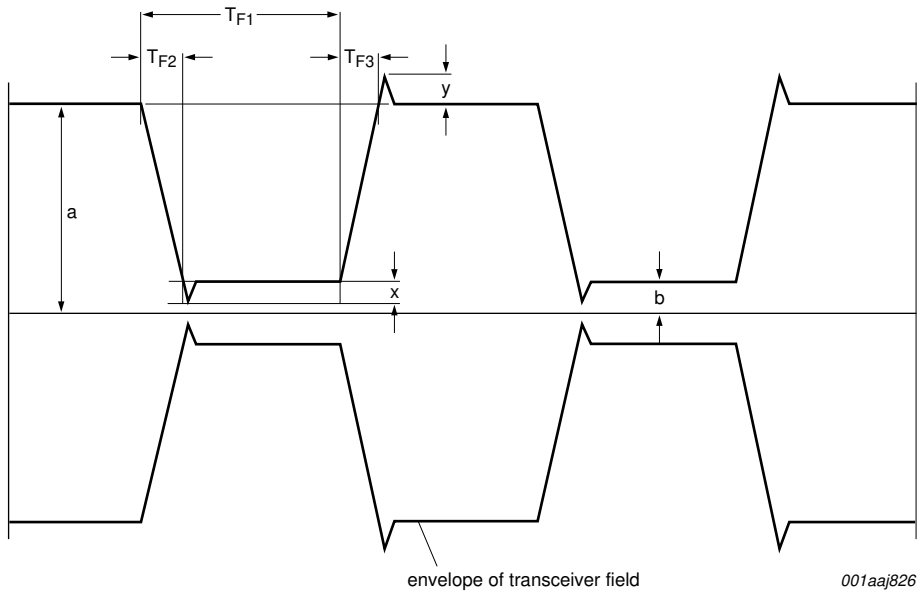

Fig 6. Modulation details of data transmission from RWD to HITAG µ transponder IC

Table 12. Modulation coding times[1][2]

Symbol	Min	Max
m = (a-b)/(a+b)	90%	100%
T_{F1}	4 × T_c	10 × T_c
T_{F2}	0	0.5 × T_{F1}
T_{F3}	0	0.5 × T_{Fd0}
x	0	0.05 × a
y	0	0.05 × a

[1] T_{F3} shall not exceed T_{Fd0} - T_{F1} - 3 × T_c

[2] $T_{C...}$Carrier period time ($1/134.2$ kHz = 7.45 µs nominal)

11.3.2 Data rate and data coding

The RWD to HITAG µ transponder IC communication uses Pulse Interval Encoding. The RWD creates pulses by switching the carrier off as described in Figure 7. The time between the falling edges of the pulses determines either the value of the data bit '0', the data bit '1', a code violation or a stop condition.

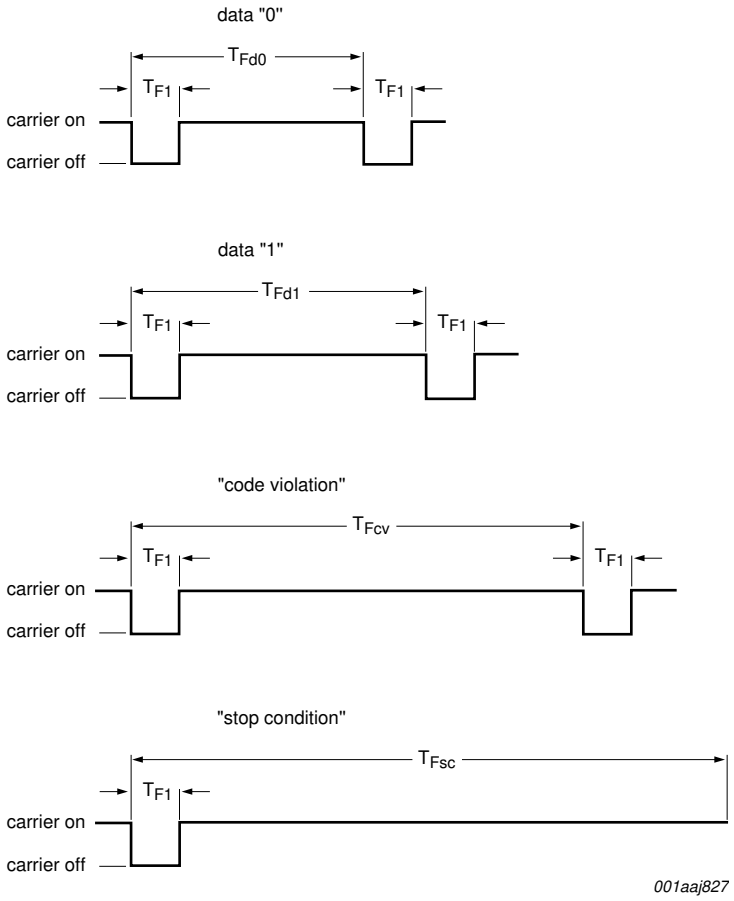

Fig 7. Reader to HITAG µ transponder IC: Pulse Interval Encoding

Assuming equal distributed data bits '0' and '1', the data rate is in the range of about 5.2 kbit/s.

Table 13. Data coding times [1]

Meaning	Symbol	Min	Max
Carrier off time	T_{F1}	$4 \times T_c$	$10 \times T_c$
Data "0" time	T_{Fd0}	$18 \times T_c$	$22 \times T_c$
Data "1" time	T_{Fd1}	$26 \times T_c$	$30 \times T_c$
Code violation time	T_{Fcv}	$34 \times T_c$	$38 \times T_c$
Stop condition time	T_{Fsc}	$\geq 42 \times T_c$	n/a

[1] $T_{C...}$ Carrier period time ($1/134.2$ kHz = 7.45 µs nominal)

11.3.3 RWD - Start of frame pattern

The RWD requests in the data exchange mode always a start with a SOF pattern for ease of synchronization. The SOF pattern consists of an encoded data bit ’0’ and a ’code violation’.

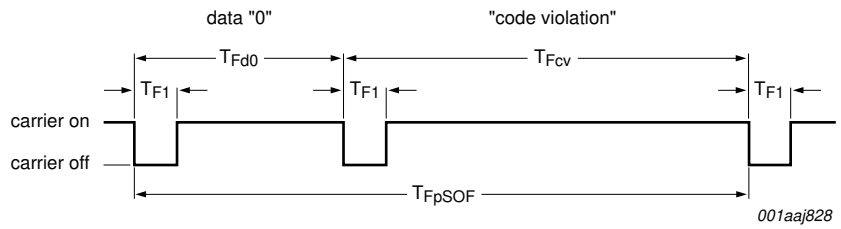

Fig 8. Start of frame pattern

The HITAG µ advanced/advanced+ is ready to receive a SOF from the RWD within 1.2 ms after having sent a response to the RWD.

The HITAG µ advanced/advanced+ is ready to receive a SOF or switch command from the RWD within 2.33 ms after the RWD has established the powering field.

11.3.4 RWD - End of frame pattern

For slot switching during a multi-slot anticollision sequence, the RWD request is an EOF pattern. The EOF pattern is represented by a RWD ’Stop condition’.

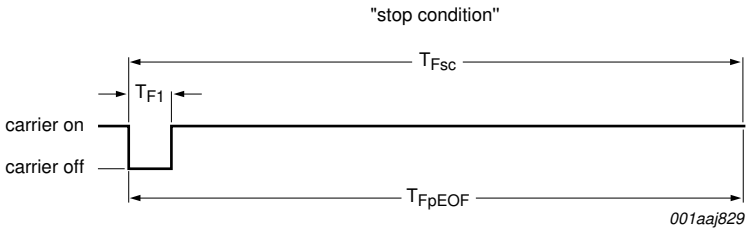

Fig 9. End of frame pattern

11.4 Communication signal interface - HITAG µ transponder IC to RWD

11.4.1 Data rate and data coding

The HITAG µ transponder IC accepts the following data rates and encoding schemes:

- $1/T_{Fd}$ Differential bi-phase coded data signal in the ISO 11785 mode, without SOF and EOF
- $1/T_{Fd}$ Manchester coded data signal on the response to the HITAG µ advanced/advanced+ commands in data exchange mode
- $1/(2 \times T_{Fd})$ dual pattern data coding when responding within the inventory process
- TTF mode (not ISO 11785 compliant): $1/(2 \times T_{Fd})$, $2/T_{Fd}$ Manchester or bi-phase coded

$T_{Fd} = 32 / f_c = 32 \times T_c$

Remark: The slower data rate used during the inventory process allows for improving the collision detection when several HITAG µ transponder ICs are present in the RWD field, especially if some HITAG µ transponder ICs are in the near field and others in the far field.

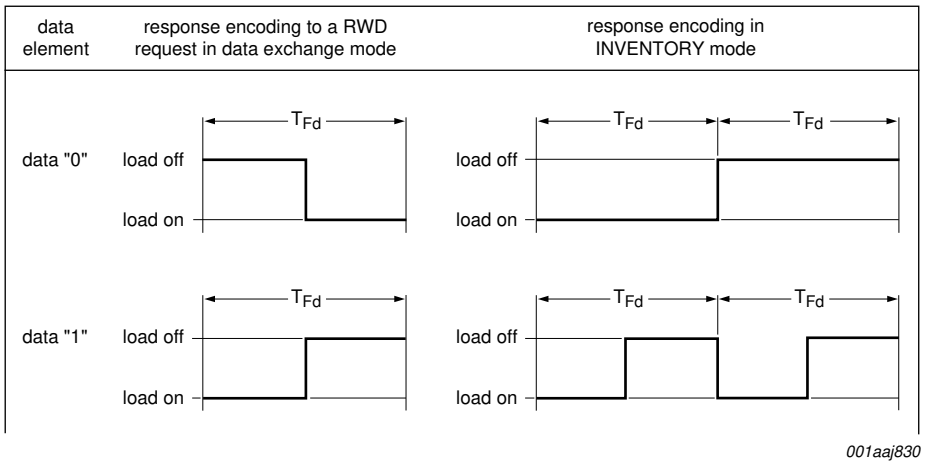

Fig 10. HITAG µ transponder IC - Load modulation coding

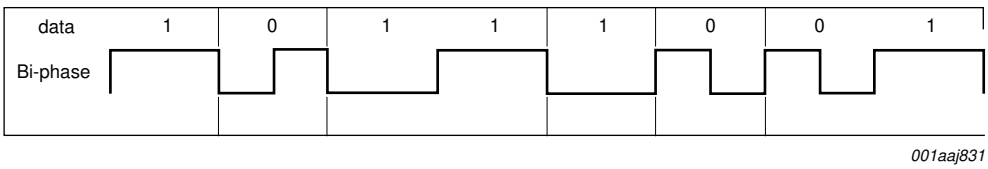

Fig 11. HITAG µ transponder IC - Differential Bi-Phase Modulation

Differential Bi-phase (or FM0 respectively) contains a transition in the center of bit conversion representing Data '0' and no one for Data '1'. At the beginning of every bit modulation a level transition must be performed.

11.4.2 Start of frame pattern

The HITAG µ transponder IC response - if not in ISO 11785 compliant mode - always starts with a SOF pattern. The SOF is a Manchester encoded bit sequence of ’110’.

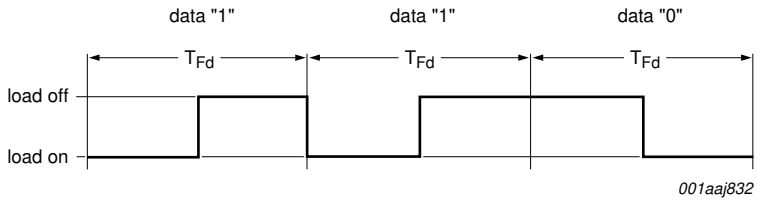

Fig 12. Start of fame pattern

11.4.3 End of frame pattern

A specific EOF pattern is neither used nor specified for the HITAG µ transponder IC response. An EOF is detected by the reader if there is no load modulation for more than two data bit periods (T_{Fd}).

12. General protocol timing specification

For requests where an EEPROM erase and/or programming operation is required, the transponder IC returns its response when it has completed the write/lock operation. This will be after 20 ms upon detection of the last falling edge of the interrogator request or after the interrogator has switched off the field.

12.1 Waiting time before transmitting a response after an EOF from the RWD

When the HITAG advanced/advanced+ in data exchange mode has detected an EOF of a valid RWD request or when this EOF is in the normal sequence of a valid RWD request, it waits for T_{Fp1} before starting to transmit its response to a RWD request or when switching to the next slot in an inventory process.

T_{Fp1} starts from the detection of the falling edge of the EOF received from the RWD.

Remark: The synchronization on the falling edge from the RWD to the EOF of the HITAG µ transponder ICs is necessary to ensure the required synchronization of the HITAG µ transponder IC responses.

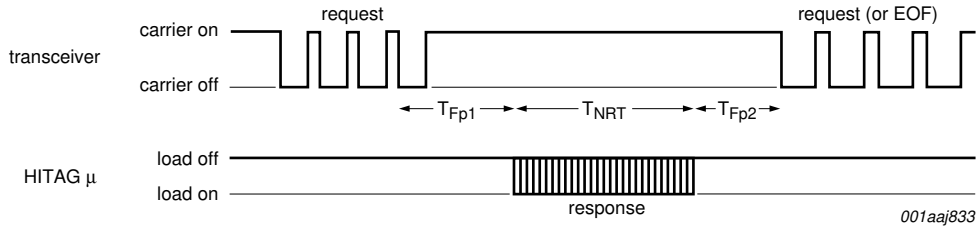

Fig 13. General protocol timing diagram

The minimum value of T_{Fp1} is $T_{Fp1min} = 204 \times T_C$

The typical value of T_{Fp1} is $T_{Fp1typ} = 209 \times T_C$

The maximum value of T_{Fp1} is $T_{Fp1max} = 213 \times T_C$

If the HITAG µ transponder IC detects a carrier modulation during this time (T_{Fp1}), it shall reset its T_{Fp1}-timer and wait for a further time (T_{Fp1}) before starting to transmit its response to a RWD request or to switch to the next slot when in an inventory process.

12.2 RWD waiting time before sending a subsequent request

- When the RWD has received a HITAG µ advanced/advanced+ response to a previous request other than inventory and quiet, it needs to wait T_{Fp2} before sending a subsequent request. T_{Fp2} starts from the time the last bit has been received from the HITAG µ advanced/advanced+.
- When the RWD has sent a quiet request, it needs to wait T_{Fp2} before sending a subsequent request. T_{Fp2} starts from the end of the quiet request's EOF (falling edge of EOF pulse + 42 × T_C). This results in awaiting time of (150 × T_C + 42 × T_C) before the next request.

The minimum value of T_{Fp2} is T_{Fp2min} = 150 × T_C ensures that the HITAG µ advanced/advanced+ ICs are ready to receive a subsequent request.

Remark: The RWD needs to wait at least 2.33 ms after it has activated the electromagnetic field before sending the first request, to ensure that the HITAG µ transponder ICs are ready to receive a request.

- When the RWD has sent an inventory request, it is in an inventory process.

12.3 RWD waiting time before switching to next inventory slot

An inventory process is started when the RWD sends an inventory request. For a detailed explanation of the inventory process refer to Section 14.3 and Section 14.4.

To switch to the next slot, the RWD sends an EOF after waiting a time period specified in the following sub-clauses.

12.3.1 RWD started to receive one or more HITAG µ transponder IC responses

During an inventory process, when the RWD has started to receive one or more HITAG µ advanced/advanced+ transponder IC responses (i.e. it has detected a HITAG µ advanced/advanced+ transponder IC SOF and/or a collision), it shall

- wait for the complete reception of the HITAG µ advanced/advanced+ transponder IC responses (i.e. when a last bit has been received or when the nominal response time T_{NRT} has elapsed),
- wait an additional time T_{Fp2} and then send an EOF to switch to the next slot, if a 16 slot anticollision request is processed, or send a subsequent request (which could be again an inventory request).

T_{Fp2} starts from the time the last bit has been received from the HITAG µ advanced/advanced+ transponder IC.

The minimum value of T_{Fp2} is T_{Fp2min} = 150 × T_C.

T_{NRT} is dependant on the anticollisions current mask value and on the setting of the CRCT flag.

12.3.2 RWD receives no HITAG µ transponder IC response

During an inventory process, when the RWD has received no HITAG µ advanced/advanced+ transponder IC response, it needs to wait T_{Fp3} before sending a subsequent EOF to switch to the next slot, if a 16 slot anticollision request is processed, or sending a subsequent request (which could be again an inventory request).

T_{Fp3} starts from the time the RWD has generated the falling edge of the last sent EOF.

The minimum value of T_{Fp3} is $T_{Fp3min} = T_{Fp1max} + T_{FpSOF}$.

T_{FpSOF} is the time duration for a HITAG µ advanced/advanced+ transponder to transmit an SOF to the reader.

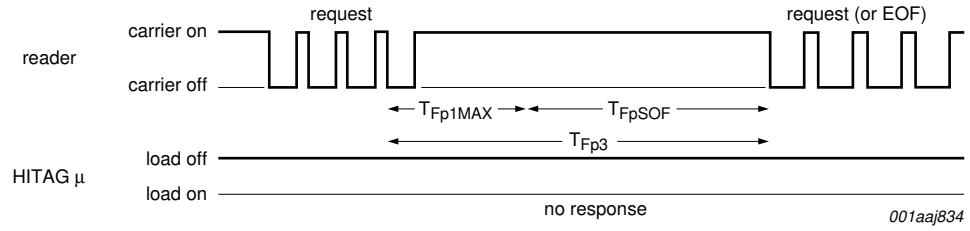

Fig 14. Protocol timing diagram without HITAG µ transponder IC response

Table 14. Overview timing parameters [1]

Symbol	Min	Max
T_{FpSOF}	$3 \times T_{Fd}$	$3 \times T_{Fd}$
T_{Fp1}	$204 \times T_C$	$213 \times T_C$
T_{Fp2}	$150 \times T_C$	-
T_{Fp3}	$T_{Fp1max} + T_{FpSOF}$	-

[1] $T_{C...}$Carrier period time ($1/_{134.2}$ kHz = 7.45 µs nominal)