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HUFA76407DK8T_F085

Dual N-Channel Logic Level UltraFET® Power MOSFET 60 V, 3.5 A, 105 mΩ

General Description

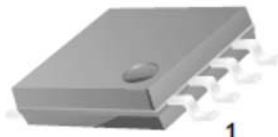
These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology achieves the lowest possible onresistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy

in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching convertors, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

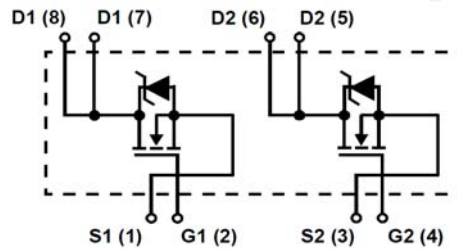


Features

- Ultra-Low On-Resistance $r_{DS(on)} = 0.090\Omega$ at $V_{GS} = 10\text{ V}$
- Ultra-Low On-Resistance $r_{DS(on)} = 0.105\Omega$ at $V_{GS} = 5\text{ V}$
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Transient Thermal Impedance Curve vs Board Mounting Area
- Switching Time vs R_{GS} Curves
- Qualified to AEC Q101
- RoHS Compliant



SO-8



MOSFET Maximum Ratings $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage (Note 1)	60	V
V_{DRG}	Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	60	V
V_{GS}	Gate to Source Voltage	± 16	V
I_D	Drain Current -Continuous ($T_A = 25\text{ }^\circ\text{C}$, $V_{GS} = 5\text{V}$) (Note 2)	3.5	A
	-Continuous ($T_A = 25\text{ }^\circ\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2) (Note 2)	3.8	
	-Continuous ($T_A = 100\text{ }^\circ\text{C}$, $V_{GS} = 5\text{V}$) (Note 3)	1	
	-Continuous ($T_A = 100\text{ }^\circ\text{C}$, $V_{GS} = 4.5\text{V}$) (Figure 2) (Note 3)	1	
I_{DM}	Drain Current -Pulsed	Figure 4	
UIS	Pulsed Avalanche Rating	Figures 6, 17, 18	
P_D	Power Dissipation (Note 2)	2.5	W
	Derate Above $25\text{ }^\circ\text{C}$	20	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Temperature for Soldering - Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
T_{pkg}	Temperature for Soldering - Package Body for 10s, See Techbrief TB334	260	$^\circ\text{C}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
76407DK8	HUFA76407DK8T_F085	SO-8	330mm	12mm	2500 units

Notes:

1. $T_J = 25\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$.
2. $50\text{ }^\circ\text{C/W}$ measured using FR-4 board with 0.76 in^2 (490.3 mm^2) copper pad at 1second.
3. $228\text{ }^\circ\text{C/W}$ measured using FR-4 board with 0.006 in^2 (3.87 mm^2) copper pad at 1000 seconds.
4. A suffix as "...F085P" has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0 \text{ V}$	(Figure 12)	60	-	-	V
			$T_A = -40^\circ\text{C}$ (Figure 12)	55	-	-	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 55 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	1	μA
			$T_A = 150^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 16 \text{ V}$	-	-	± 100	nA	

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$ (Figure 11)	1	-	3	V
$r_{DS(on)}$	Static Drain to Source On Resistance	$I_D = 3.8 \text{ A}$, $V_{GS} = 10 \text{ V}$ (Figure 9,10)	-	0.075	0.090	Ω
		$I_D = 1.0 \text{ A}$, $V_{GS} = 5 \text{ V}$ (Figure 9)	-	0.088	0.105	
		$I_D = 1.0 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ (Figure 9)	-	0.092	0.110	

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient	0.76in ² (490.3mm ²) Pad (Note 2)	-	-	50	$^\circ\text{C/W}$
		0.027in ² (17.4mm ²) Pad (Figure 23)	-	-	191	
		0.006in ² (3.87mm ²) Pad (Figure 23)	-	-	228	

Switching Characteristics ($V_{GS}=4.5\text{V}$)

t_{on}	Turn-On Time	$V_{DD} = 30 \text{ V}$, $I_D = 1.0 \text{ A}$, $V_{GS} = 4.5 \text{ V}$, $R_{GS} = 27 \Omega$ (Figure 15, 21, 22)	-	-	57	ns
$t_{d(on)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	30	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	25	-	ns
t_f	Fall Time		-	25	-	ns
t_{off}	Turn-Off Time		-	-	75	ns

Switching Characteristics ($V_{GS}=10\text{V}$)

t_{on}	Turn-On Time	$V_{DD} = 30 \text{ V}$, $I_D = 3.8 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GS} = 30 \Omega$ (Figure 16, 21, 22)	-	-	24	ns
$t_{d(on)}$	Turn-On Delay Time		-	5	-	ns
t_r	Rise Time		-	11	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	46	-	ns
t_f	Fall Time		-	31	-	ns
t_{off}	Turn-Off Time		-	-	116	ns

Gate Charge Characteristics

$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0$ to 10 V	$V_{DD} = 30 \text{ V}$, $I_D = 1.0 \text{ A}$, $I_{g(REF)} = 1.0 \text{ mA}$, (Figure 14, 19, 20)	-	9.4	11.2	nC
$Q_{g(5)}$	Gate Charge at 5V	$V_{GS} = 0$ to 5 V		-	5.3	6.4	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0$ to 1 V		-	0.42	0.5	nC
Q_{gs}	Gate to Source Charge			-	1.05	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	2.4	-	nC

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$,	-	330	-	pF
C_{oss}	Output Capacitance	$f = 1 \text{ MHz}$,	-	100	-	pF
C_{rss}	Reverse Transfer Capacitance	(Figure 13)	-	18	-	pF

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$I_{SD} = 3.8 \text{ A}$	-	-	1.25	V
		$I_{SD} = 1.0 \text{ A}$	-	-	1.00	
t_{rr}	Reverse Recovery Time	$I_F = 1.0 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	-	48	ns
Q_{rr}	Reverse Recovery Charge		-	-	89	nC

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

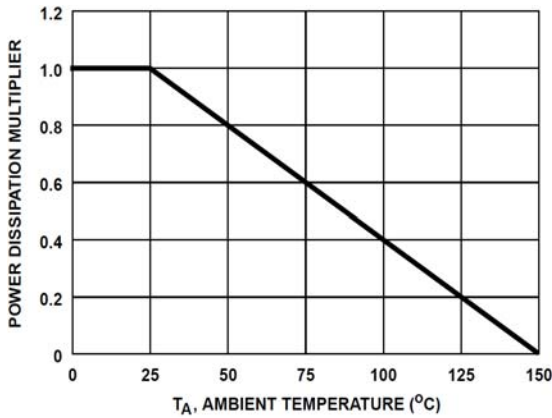


Figure 1. NORMALIZED POWER DISSIPATION vs. AMBIENT TEMPERATURE

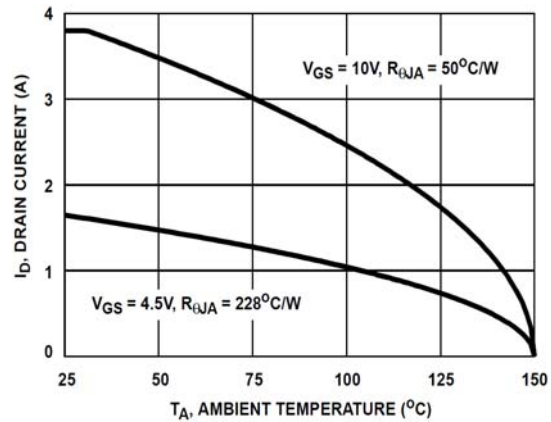


Figure 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs. AMBIENT TEMPERATURE

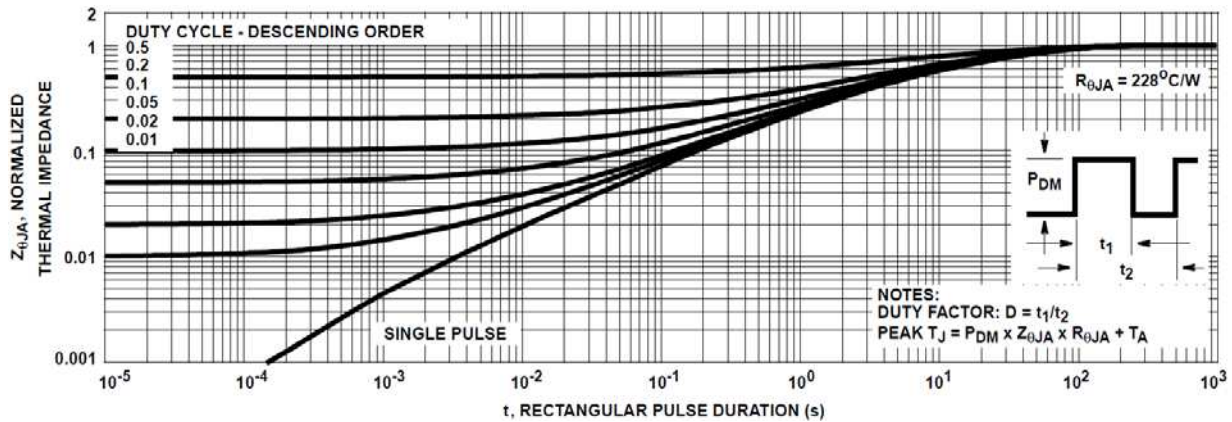


Figure 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

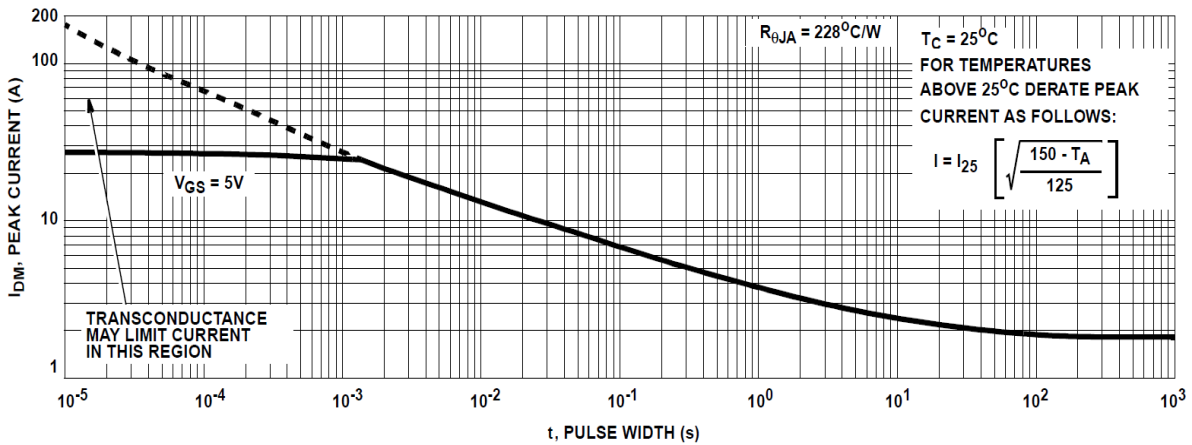


Figure 4. PEAK CURRENT CAPABILITY

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

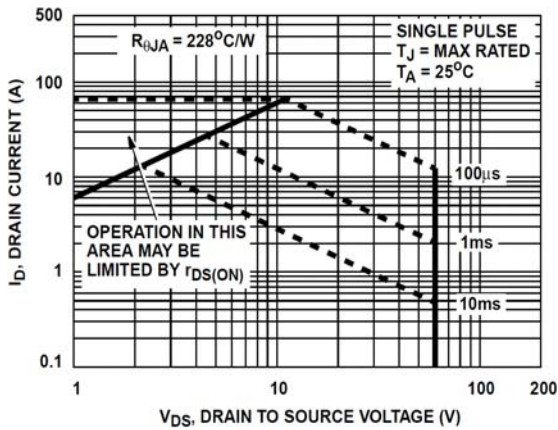


Figure 5. FORWARD BIAS SAFE OPERATING AREA

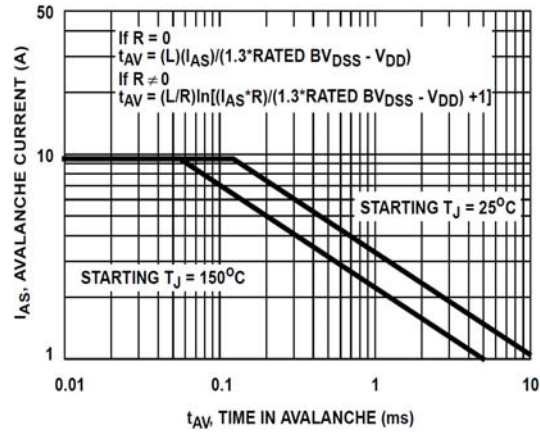


Figure 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

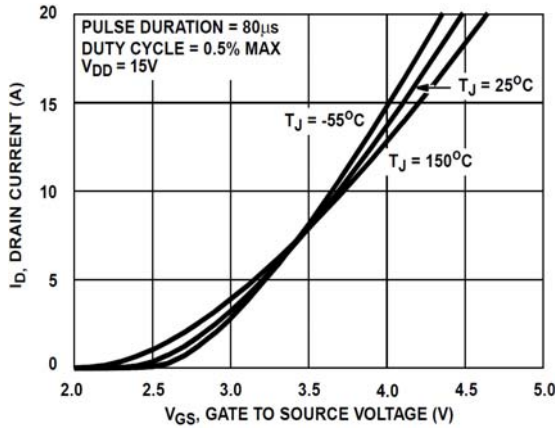


Figure 7. TRANSFER CHARACTERISTICS

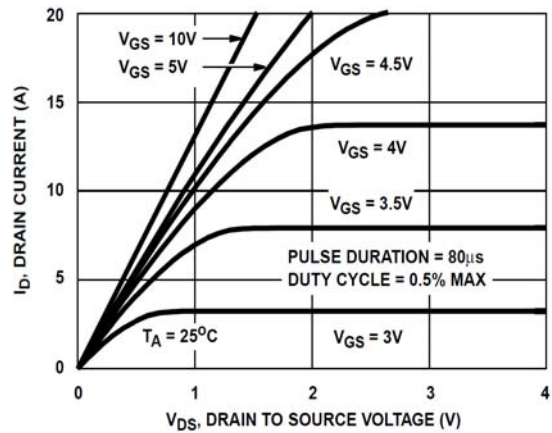


Figure 8. SATURATION CHARACTERISTICS

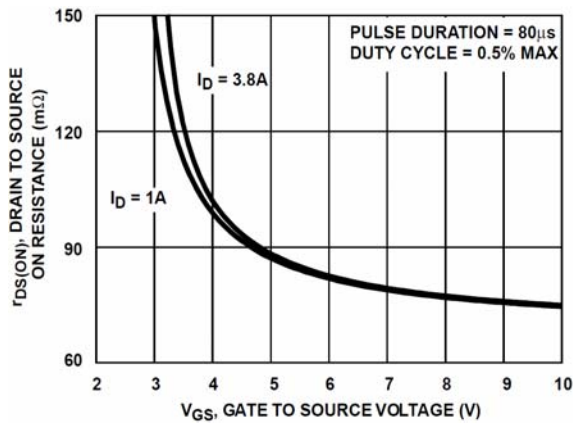


Figure 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

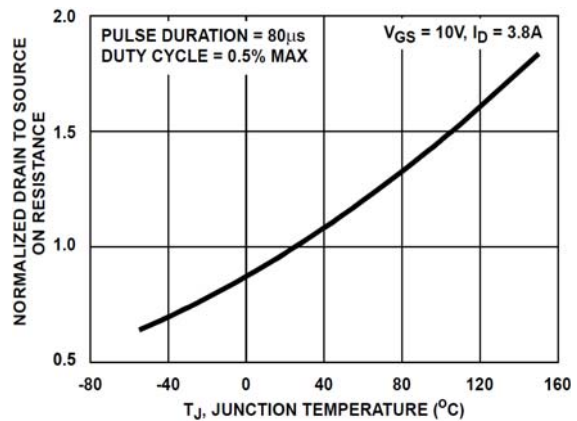


Figure 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

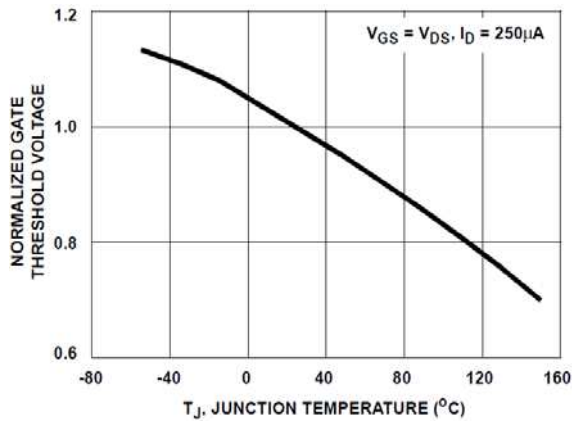


Figure 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

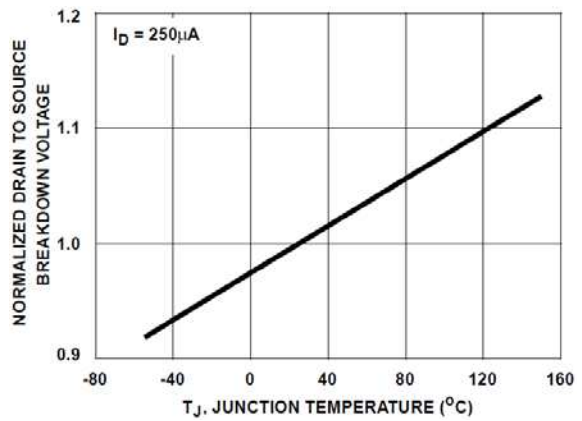


Figure 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

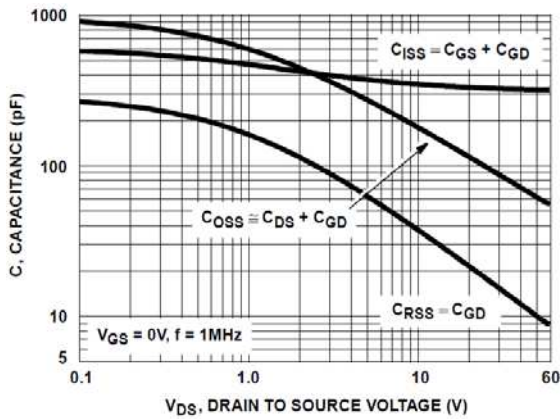


Figure 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

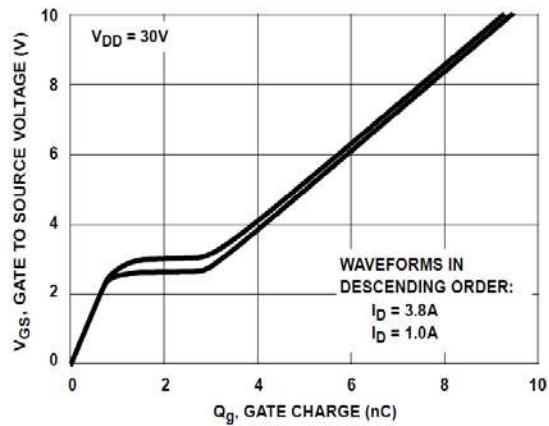


Figure 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

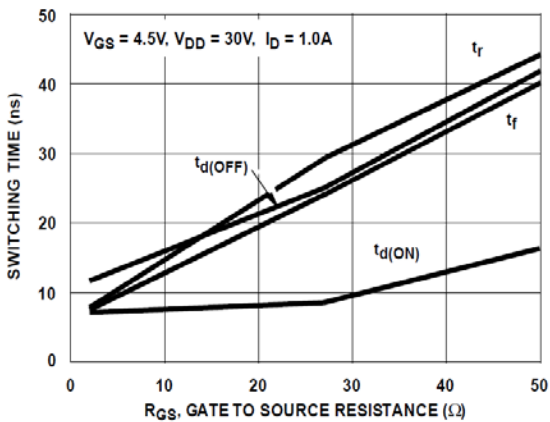


Figure 15. SWITCHING TIME vs GATE RESISTANCE

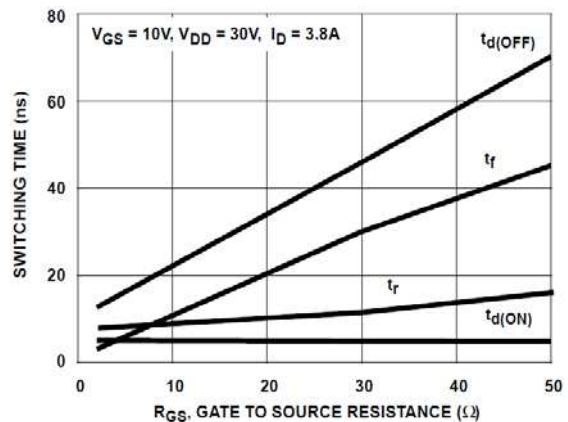
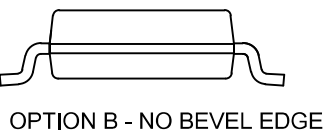
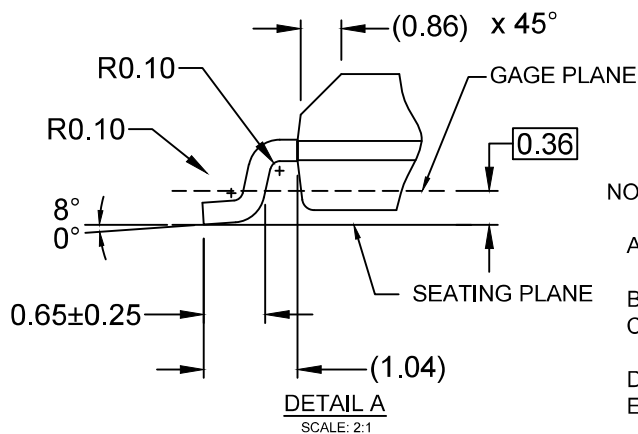
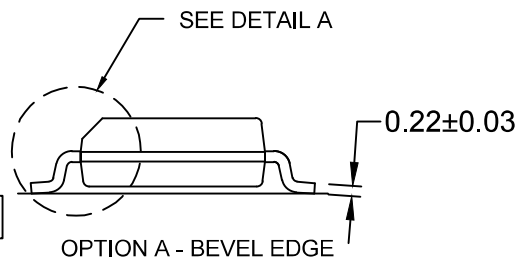
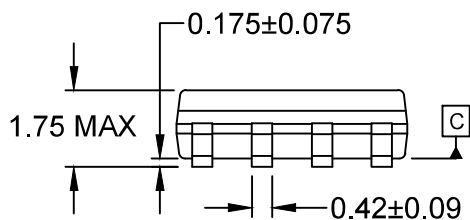
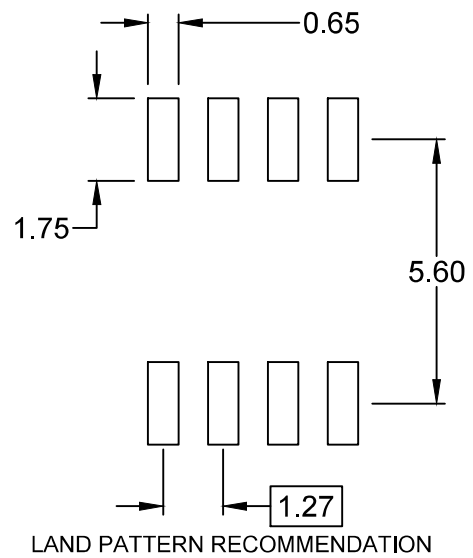
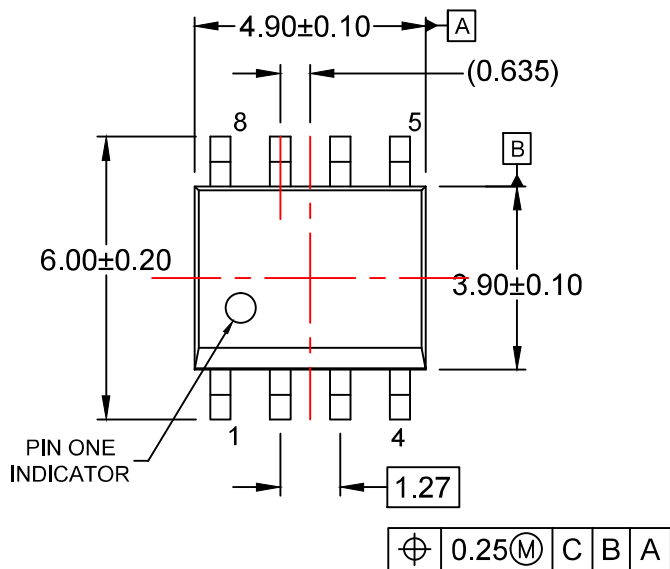


Figure 16. SWITCHING TIME vs GATE RESISTANCE



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
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- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
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