

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China









Data Sheet December 2001

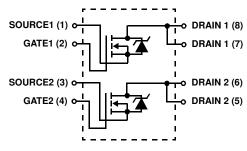
3.5A, 60V, 0.105 Ohm, Dual N-Channel, Logic Level UltraFET® Power MOSFET

Packaging

JEDEC MS-012AA



Symbol





Features

- · Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.090\Omega$, $V_{GS} = 10V$
 - $r_{DS(ON)} = 0.105\Omega$, $V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - SPICE and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- · Peak Current vs Pulse Width Curve
- · UIS Rating Curve
- Transient Thermal Impedance Curve vs Board Mounting Area
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA76407DK8	MS-012AA	76407DK8

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUFA76407DK8T.

Absolute Maximum Ratings T_A = 25°C, Unless Otherwise Specified

	HUFA76407DK8	UNITS
Drain to Source Voltage (Note 1)	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	60	V
Gate to Source Voltage	±16	V
Drain Current		
Continuous ($T_A = 25^{\circ}C$, $V_{GS} = 5V$) (Note 2)	3.5	Α
Continuous ($T_A = 25^{\circ}$ C, $V_{GS} = 10$ V) (Figure 2) (Note 2)	3.8	Α
Continuous ($T_A = 100^{\circ}$ C, $V_{GS} = 5V$) (Note 3)	1.0	Α
Continuous ($T_A = 100^{\circ}$ C, $V_{GS} = 4.5$ V) (Figure 2) (Note 3)	1.0	Α
Pulsed Drain Current	Figure 4	
Pulsed Avalanche RatingUIS	Figures 6, 17, 18	
Power Dissipation (Note 2)	2.5	W
Derate Above 25°C	20	mW/ ^o C
Operating and Storage Temperature	-55 to 150	°C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10sT _I	300	°C
Package Body for 10s, See Techbrief TB334	260	°C

NOTES: 1. $T_J = 25^{\circ}C$ to $125^{\circ}C$.

- 2. 50°C/W measured using FR-4 board with 0.76 in² (490.3 mm²) copper pad at 1 second.
- 3. 228°C/W measured using FR-4 board with 0.006 in² (3.87 mm²) copper pad at 1000 seconds.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUFA76407DK8

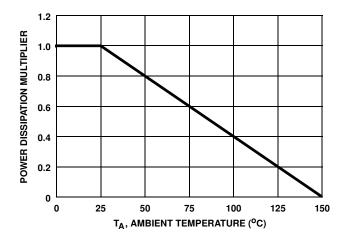
Electrical Specifications T_A = 25°C, Unless Otherwise Specified

Description	PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
To = 250μA, VGS = 0V	OFF STATE SPECIFICATIONS					+	ļ.	-
Vos = 55V, Vos = 0V	Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)		60	-	-	V
VDS = 50V, VGS = 0V, TA = 150°C			$I_D = 250\mu A$, $V_{GS} = 0V$, $T_A = -40^{\circ}C$ (Figure 12)		55	-	-	V
Gate to Source Leakage Current IGSS VGS = ±16V	Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55V, V _{GS} = 0V	I	-	-	1	μΑ
ON STATE SPECIFICATIONS VGS(TH) VGS = VDS, ID = 250µA (Figure 11) 1 - 3 V Drain to Source On Resistance FDS(NN) ID = 3.8A, VGS = 10V (Figure 9) - 0.075 0.090 Ω THERMAL SPECIFICATIONS THERMAL SPECIFICATIONS Thermal Resistance Junction to Ambient RBJA Pad Area = 0.76 in² (490.3 mm²) (Note 2) - - 5.0 °C/W Ambient Pad Area = 0.026 in² (490.3 mm²) (Note 2) - - 5.0 °C/W Ambient Pad Area = 0.027 in² (17.4 mm²) (Figure 23) - - 5.0 °C/W Ambient Ion No. VDD = 30V. Ip = 1.00. (Figure 23) - - 1.0 VC/W SWITCHING SPECIFICATIONS (VGS = 4.5V) Turn-On Time Ion No. VDD = 30V. Ip = 3.0A - - 5.7 ns SWITCHING SPECIFICATIONS (VGS = 1.5V) VDF = 30V. Ip = 3.8A - - - 5.7 ns SWITCHING SPECIFICATIONS (VGS = 10V) VGS = 10V. - -			$V_{DS} = 50V, V_{GS} = 0V$	/, T _A = 150 ^o C	-	-	250	μΑ
ON STATE SPECIFICATIONS V _{GS} (TH) V _{GS} = V _{DS} , I _D = 250µA (Figure 11) 1 - 3 V Drain to Source On Resistance V _{GS} = V _{DS} , I _D = 250µA (Figure 9, 10) 1 - 3 V Drain to Source On Resistance In John (V _{GS} = 10V (Figure 9) - 0.075 0.090 Ω THERMAL SPECIFICATIONS THERMAL SPECIFI	Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V		-	-	±100	nA
Day Da	ON STATE SPECIFICATIONS							
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate to Source Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250$	μA (Figure 11)	1	-	3	V
Thermal Resistance Junction to Ambient Pad Area = 0.76 in² (490.3 mm²) (Note 2) - 0.092 0.110 Ω	Drain to Source On Resistance		I _D = 3.8A, V _{GS} = 10V	' (Figures 9, 10)	-	0.075	0.090	Ω
Pad Area = 0.76 in² (490.3 mm²) (Note 2)		, ,	I _D = 1.0A, V _{GS} = 5V			0.088	0.105	Ω
Pad Area = 0.76 in² (490.3 mm²) (Note 2)			$I_D = 1.0A, V_{GS} = 4.5$	V (Figure 9)	-	0.092	0.110	Ω
Pad Area = 0.027 in² (17.4 mm²) (Figure 23) - - 191 0°C/W Pad Area = 0.006 in² (3.87 mm²) (Figure 23) - - 228 0°C/W SWITCHING SPECIFICATIONS (VGS = 4.5V) Turn-On Time	THERMAL SPECIFICATIONS					I	I.	.1
Pad Area = 0.02 in (Figure 23) - - 228 OC/W	Thermal Resistance Junction to	$R_{ heta JA}$	Pad Area = 0.76 in ² (490.3 mm ²) (Note 2)	-	-	50	oC/W
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V) Turn-On Time t _{ON} V _{DD} = 30V, I _D = 1.0A - 57 ns Turn-On Delay Time t _d (ON) (Figures 15, 21, 22) - 8 - ns Rise Time t _f - 25 - ns Turn-Off Delay Time t _f - 25 - ns Fall Time t _f 75 ns SWITCHING SPECIFICATIONS (V _{GS} = 10V) Turn-Off Time t _{OF} 75 ns SWITCHING SPECIFICATIONS (V _{GS} = 10V) Turn-On Delay Time t _{OF} 75 ns Turn-On Delay Time t _O (ON) V _{DD} = 30V, I _D = 3.8A 24 ns Turn-Off Delay Time t _O (ON) V _{GS} = 30Ω 24 ns Rise Time t _f (Figures 16, 21, 22) 111 - ns Turn-Off Delay Time t _O (OF) R _{GS} = 30Ω 116 ns Turn-Off Time t _O (F) 116 ns GATE CHARGE SPECIFICATIONS 116 ns Gate Charge Q _G (TH)	Ambient		Pad Area = 0.027 in ²	(17.4 mm ²) (Figure 23)	-	-	191	oC/W
Turn-On Time toN VDD = 30V, ID = 1.0A VGS = 4.5V, RGS = 27Ω Figures 15, 21, 22 Figures 16, 21, 22 Figures 14, 19, 20 F			, , , , , , , , , , , , , , , , , , , ,		-	-	228	oC/W
Turn-On Delay Time	SWITCHING SPECIFICATIONS (VGS	= 4.5V)						
Figures 15, 21, 22	Turn-On Time	t _{ON}			-	-	57	ns
Fise Time	Turn-On Delay Time	t _{d(ON)}	$V_{GS} = 4.5V, R_{GS} = 27\Omega$		-	8	-	ns
Fall Time	Rise Time				-	30	-	ns
Fall Time t _f t _{OFF} Turn-Off Time t _{OFF} Turn-Off Time t _{OFF} Turn-Off Time t _{ON} V _{DD} = 30V, I _D = 3.8A V _{GS} = 10V, I _D = 3.8A V _{GS} = 10V, I _D = 3.8A V _{GS} = 30Ω V _{DS} = 30Ω V _{DD} = 30V V _D = 1.0A V _D =	Turn-Off Delay Time	t _{d(OFF)}			-	25	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Fall Time				-	25	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-Off Time	tOFF	1		-	-	75	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	SWITCHING SPECIFICATIONS (VGS	= 10V)				1		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-On Time	ton	$V_{GS} = 10V$, $R_{GS} = 30\Omega$		-	-	24	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-On Delay Time	t _d (ON)			-	5	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Rise Time	t _r			-	11	-	ns
Turn-Off Time t_{OFF} $-$ 116 ns GATE CHARGE SPECIFICATIONS Total Gate Charge $Q_{g(TOT)}$ $V_{GS} = 0V \text{ to } 10V$ $V_{DD} = 30V$, V_{D	Turn-Off Delay Time	t _d (OFF)			-	46	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Fall Time	t _f		1		31	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-Off Time	t _{OFF}	1		-	-	116	ns
Gate Charge at 5V $Q_{g(5)} V_{GS} = 0V \text{ to } 5V$ Threshold Gate Charge $Q_{g(TH)} V_{GS} = 0V \text{ to } 1V$ Gate to Source Gate Charge $Q_{gs} Q_{gd} P_{gs} = 0V \text{ to } 1V$ Gate to Drain "Miller" Charge $Q_{gd} P_{gs} = 0V \text{ to } 1V$ $Q_{g(TH)} Q_{gs} P_{gs} = 0V \text{ to } 1V$ $Q_{g(TH)} Q_{gs} P_{gs} = 0V \text{ to } 1V$ $Q_{g(TH)} Q_{gs} P_{gs} = 0V \text{ to } 1V$ $Q_{g(TH)} Q_{gs} P_{gs} = 0V \text{ to } 1V$ $Q_{g(TH)} Q_{gs} P_{gs} = 1.0 \text{ and } 10V$ $P_{g(TH)} P_{g(TH)} P_{gs} = 1.0 \text{ and } 10V$ $P_{g(TH)} P_{g(TH)} P_{gs} = 1.0 \text{ and } 10V$ $P_{g(TH)} P_{g(TH)} P_{gs} = 1.0 \text{ and } 10V$ $P_{g(TH)} P_{g(TH)} P_{gs} = 1.0 \text{ and } 10V$ $P_{g(TH)} P_{g(TH)} P_{gs} = 1.0 \text{ and } 10V$ $P_{g(TH)} P_{g(TH)} P_{gs} = 1.0 \text{ and } 10V$ $P_{g(TH)} P_{g(TH)} P_{g$	GATE CHARGE SPECIFICATIONS	1				Ш	II.	1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V		-	9.4	11.2	nC
Threshold Gate Charge $Q_{g(TH)}$ $V_{GS} = 0V \text{ to } 1V$ $(Figures 14, 19, 20)$ $- 0.42 0.5 nC$ Gate to Source Gate Charge Q_{gS} $- 1.05 - nC$ Gate to Drain "Miller" Charge Q_{gd} $- 2.4 - nC$ $- 2.4 - nC$ $$	Gate Charge at 5V		$V_{GS} = 0V \text{ to } 5V$	I _D = 1.0A,	-	5.3	6.4	nC
Gate to Source Gate Charge Q_{gs} $-$ 1.05 $-$ nC Gate to Drain "Miller" Charge Q_{gd} $-$ 2.4 $-$ nC CAPACITANCE SPECIFICATIONS Input Capacitance C_{ISS} $V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$ (Figure 13) $F = 100 - F$	Threshold Gate Charge		$I_{g(REF)} = I.UMA$	-	0.42	0.5	nC	
Gate to Drain "Miller" Charge Q_{gd} - 2.4 - nC CAPACITANCE SPECIFICATIONS Input Capacitance C_{ISS} $V_{DS} = 25V, V_{GS} = 0V,$ - 330 - pF Output Capacitance C_{OSS} $f = 1MHz$ (Figure 13)	Gate to Source Gate Charge				-	1.05	-	nC
Input Capacitance C_{ISS} $V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$ (Figure 13) $ pF$	Gate to Drain "Miller" Charge	_			-	2.4	-	nC
Output Capacitance Coss f = 1MHz (Figure 13)	CAPACITANCE SPECIFICATIONS				1	1	ı	-
Output Capacitance C _{OSS} f = 1MHz (Figure 13)	Input Capacitance	C _{ISS}		/,	-	330	-	pF
(Tiguic 10)	Output Capacitance				-	100	-	pF
	Reverse Transfer Capacitance				-	18	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I _{SD} = 3.8A		-	1.25	V
		I _{SD} = 1.0A	-	-	1.00	V
Reverse Recovery Time	t _{rr}	$I_{SD} = 1.0A$, $dI_{SD}/dt = 100A/\mu s$	-	-	48	ns
Reverse Recovered Charge	Q _{RR}	$I_{SD} = 1.0A$, $dI_{SD}/dt = 100A/\mu s$		-	89	nC

Typical Performance Curves



V_{GS} = 10V, R_{θJA} = 50°C/W

V_{GS} = 10V, R_{θJA} = 50°C/W

V_{GS} = 4.5V, R_{θJA} = 228°C/W

0
25 50 75 100 125 150

T_A, AMBIENT TEMPERATURE (°C)

FIGURE 1. NORMALIZED POWER DISSIPATION VS AMBIENT TEMPERATURE

FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

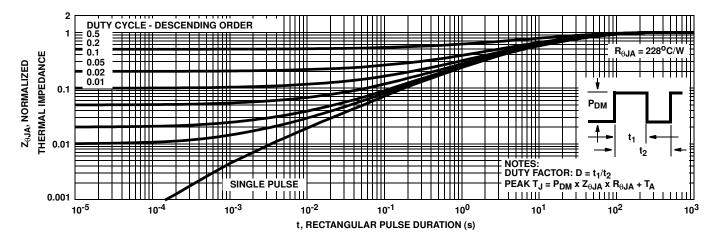


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

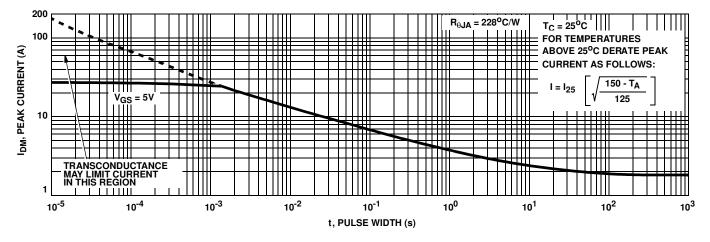


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

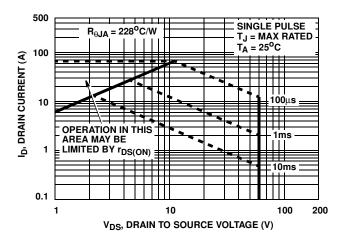


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

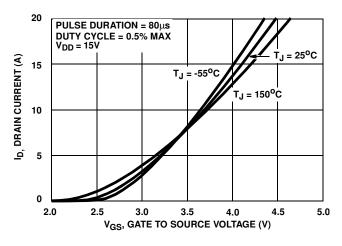


FIGURE 7. TRANSFER CHARACTERISTICS

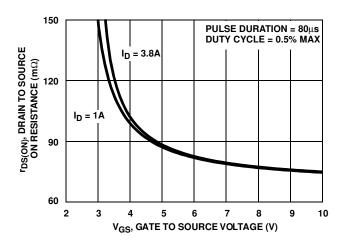
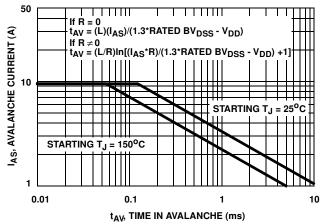


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

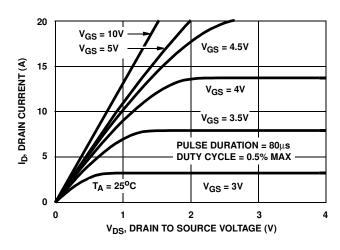


FIGURE 8. SATURATION CHARACTERISTICS

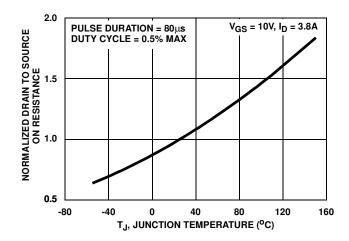


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE VS JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

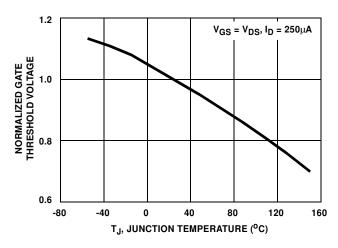


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

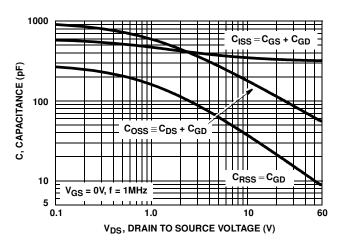


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

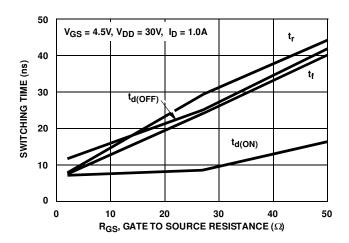


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

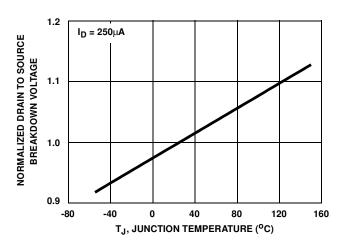
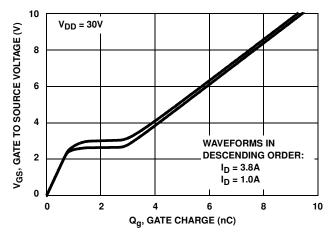


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

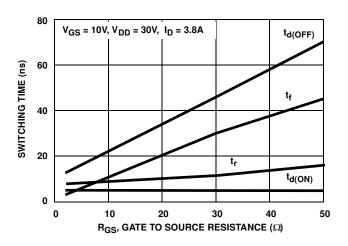


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

©2001 Fairchild Semiconductor Corporation

Test Circuits and Waveforms

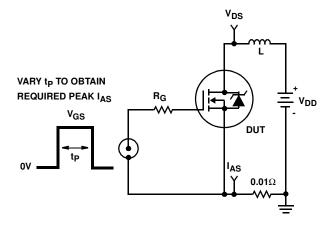


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

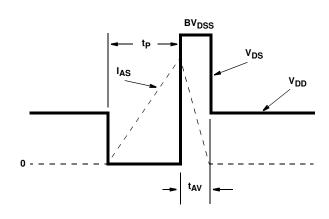


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

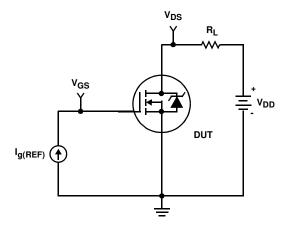


FIGURE 19. GATE CHARGE TEST CIRCUIT

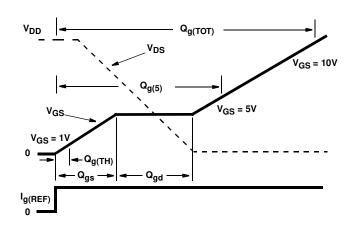


FIGURE 20. GATE CHARGE WAVEFORMS

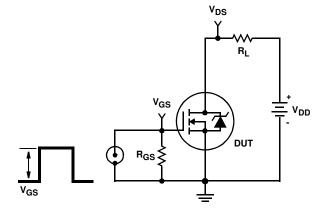


FIGURE 21. SWITCHING TIME TEST CIRCUIT

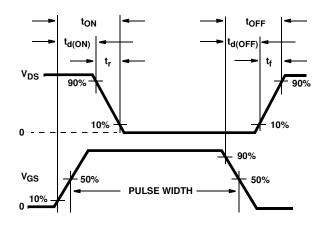


FIGURE 22. SWITCHING TIME WAVEFORM

©2001 Fairchild Semiconductor Corporation

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A (^{o}C), and thermal resistance $R_{\theta JA}$ ($^{o}C/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$_{DM} = \frac{(T_{JM} - T_{A})}{R_{0,JA}}$$
 (EQ. 1)

In using surface mount devices such as the SOP-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- 6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 23 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM} .

Thermal resistances corresponding to other copper areas can be obtained from Figure 23 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a cofficient added to a constant. The area, in square

inches is the top copper area including the gate and source pads.

$$R_{\theta, JA} = 103.2 - 24.3 \times \ln(Area)$$
 (EQ. 2)

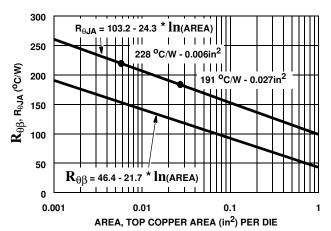


FIGURE 23. THERMAL RESISTANCE vs MOUNTING PAD AREA

While Equation 2 describes the thermal resistance of a single die, several of the new UltraFETs are offered with two die in the SOP-8 package. The dual die SOP-8 package introduces an additional thermal component, thermal coupling resistance, $R_{\theta\beta}$. Equation 3 describes $R_{\theta\beta}$ as a function of the top copper mounting pad area.

$$R_{\theta\beta} = 46.4 - 21.7 \times \ln(\text{Area})$$
 (EQ. 3)

The thermal coupling resistance vs. copper area is also graphically depicted in Figure 23. It is important to note the thermal resistance $(R_{\theta J}A)$ and thermal coupling resistance $(R_{\theta \beta})$ are equivalent for both die. For example at 0.1 square inches of copper:

$$R_{\theta, JA1} = R_{\theta, JA2} = 159^{\circ}C/W$$

$$R_{\theta\beta1}=R_{\theta\beta2}=97^{\text{O}}\text{C/W}$$

 T_{J1} and T_{J2} define the junction temerature of the respective die. Similarly, P_1 and P_2 define the power dissipated in each die. The steady state junction temperature can be calculated using Equation 4 for die 1 and Equation 5 for die 2.

Example: To calculate the junction temperature of each die when die 2 is dissipating 0.5 Watts and die 1 is dissipating 0 Watts. The ambient temperature is 70° C and the package is mounted to a top copper area of 0.1 square inches per die. Use Equation 4 to calulate T_{J1} and and Equation 5 to calulate T_{J2} .

$$\begin{split} & \text{T}_{\text{J1}} = \text{P}_{1} \text{R}_{\theta \text{JA}} + \text{P}_{2} \text{R}_{\theta \beta} + \text{T}_{\text{A}} & \text{(EQ. 4)} \\ & \text{T}_{\text{J1}} = (0 \text{ Watts})(159^{\text{O}}\text{C/W}) + (0.5 \text{ Watts})(97^{\text{O}}\text{C/W}) + 70^{\text{O}}\text{C} \end{split}$$

 $T_{J1} = 119^{\circ}C$

HUFA76407DK8

$$\begin{split} & \text{T}_{J2} = \text{P}_2 \text{R}_{\theta J \text{A}} + \text{P}_1 \text{R}_{\theta \beta} + \text{T}_{\text{A}} \\ & \text{T}_{J2} = (0.5 \text{ Watts}) (159^{\text{O}}\text{C/W}) + (0 \text{ Watts}) (97^{\text{O}}\text{C/W}) + 70^{\text{o}}\text{C} \\ & \text{T}_{J2} = 150^{\text{O}}\text{C} \end{split}$$

The transient thermal impedance $(Z_{\theta JA})$ is also effected by varied top copper board area. Figure 24 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the

graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

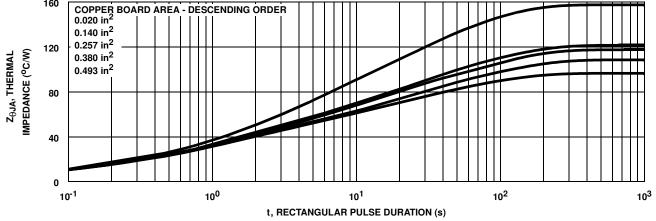


FIGURE 24. THERMAL RESISTANCE vs MOUNTING PAD AREA

PSPICE Electrical Model

.SUBCKT HUFA76407DK8 2 1 3; REV 28 May 1999

CA 12 8 4.55e-10 CB 15 14 5.20e-10 CIN 6 8 3.11e-10

DBODY 7 5 DBODYMOD LDRAIN DBREAK 5 11 DBREAKMOD **DPLCAP** DRAIN **DPLCAP 10 5 DPLCAPMOD** 10 **RLDRAIN** RSLC1 EBREAK 11 7 17 18 67.8 DRRFAK 51 EDS 14 8 5 8 1 RSLC2 EGS 13 8 6 8 1 ESG 6 10 6 8 1 **ESLC** 11 EVTHRES 6 21 19 8 1 EVTEMP 20 6 18 22 1 50 17 18 **▲** DBODY **≥**RDRAIN 8 **EBREAK ESG** IT 8 17 1 **EVTHRES** 16 21 1<u>9</u> 8 **MWEAK** LDRAIN 2 5 1.0e-9 **EVTEMP LGATE** LGATE 1 9 1.5e-9 **RGATE** GATE 18 22 6 LSOURCE 3 7 4.86e-10 -MMED 9 20 **←** MSTR **RLGATE** MMED 16 6 8 8 MMEDMOD MSTRO 16 6 8 8 MSTROMOD **LSOURCE** CIN SOURCE MWEAK 16 21 8 8 MWEAKMOD 8 **RSOURCE** RBREAK 17 18 RBREAKMOD 1 **RLSOURCE** RDRAIN 50 16 RDRAINMOD 3.00e-2 RGATE 9 20 3.37 S1A S2A **RBREAK** RLDRAIN 2 5 10 15 13 8 14 13 18 RLGATE 1 9 15 **RLSOURCE 3 7 4.86 RVTEMP** S₁B o S2B RSLC1 5 51 RSLCMOD 1e-6 13 RSLC2 5 50 1e3 CB 19 CA 14 IT RSOURCE 8 7 RSOURCEMOD 3.80e-2 RVTHRES 22 8 RVTHRESMOD 1 **VBAT** <u>5</u> 8 **EGS EDS RVTEMP 18 19 RVTEMPMOD 1** 8 S1A 6 12 13 8 S1AMOD S1B 13 12 13 8 S1BMOD **RVTHRES** S2A 6 15 14 13 S2AMOD S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*105),2))}

```
.MODEL DBODYMOD D (IS = 3.17e-13 RS = 2.21e-2 TRS1 = 6.25e-4 TRS2 = -1.11e-6 CJO = 6.82e-10 TT = 7.98e-8 M = 0.65)
.MODEL DBREAKMOD D (RS = 3.36e- 1TRS1 = 1.25e- 4TRS2 = 1.34e-6)
MODEL DPLCAPMOD D (CJO = 2.91e-1 0IS = 1e-3 0M = 0.85)
.MODEL MMEDMOD NMOS (VTO = 2.00 KP = 1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.37)
.MODEL MSTROMOD NMOS (VTO = 2.33 KP = 19 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
MODEL MWEAKMOD NMOS (VTO = 1.71 KP = 0.02 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 33.7 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.06e- 3TC2 = 0)
MODEL RDRAINMOD RES (TC1 = 1.23e-2 TC2 = 2.58e-5)
.MODEL RSLCMOD RES (TC1 = 1.0e-3 TC2 = 1.0e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.19e-3 TC2 = -4.97e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.11e- 3TC2 = 0)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.0 VOFF= -2.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.5 VOFF= -7.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.0 VOFF= 0)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0 VOFF= -1.0)
```

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options:** IEEE Power Electronics Specialist Conference Records. 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
REV 28May 1999
template HUFA76407dk8 n2,n1,n3
electrical n2,n1,n3
var i iscl
d..model dbodymod = (is = 3.17e-13, cjo = 6.82e-10, tt = 7.98e-8, m = 0.65)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 2.91e-10, is = 1e-30, m = 0.85)
m..model mmedmod = (type=_n, vto = 2.00, kp = 1, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.33, kp = 19, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.71, kp = 0.02, is = 1e-30, tox = 1)
                                                                                                                                LDRAIN
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -7, voff = -2.5)
                                                                                  DPLCAP
                                                                                            5
                                                                                                                                          DRAIN
sw vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.5, voff = -7)
                                                                              10
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.0, voff = 0)
                                                                                                                               RLDRAIN
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0, voff = -1)
                                                                                               RSLC1
                                                                                                          RDBREAK
c.ca n12 n8 = 4.55e-10
                                                                               RSLC2 §
                                                                                                                   72
c.cb n15 n14 = 5.20e-10
                                                                                                                               RDBODY
                                                                                                ISCL
c.cin n6 n8 = 3.11e-10
                                                                                                            DBREAK _
d.dbody n7 n71 = model=dbodymod
                                                                                              RDRAIN
d.dbreak n72 n11 = model=dbreakmod
                                                                            6
8
                                                                      ESG
                                                                                                                    11
d.dplcap n10 n5 = model=dplcapmod
                                                                                  EVTHRES
                                                                                                  16
                                                                                              21
                                                                                     1<u>9</u>
i.it n8 n17 = 1
                                                                                                              MWEAK
                                                  LGATE
                                                                    EVTEMP
                                                                                                                               DBODY
                                                            RGATE
                                          GATE
                                                                               6
                                                                                                               EBREAK
I.ldrain n2 n5 = 1e-9
                                                                                                    MMED
                                                           9
                                                                   20
I.lgate n1 n9 = 1.5e-9
                                                                                             MSTR
                                                  RLGATE
I.Isource n3 n7 = 4.86e-10
                                                                                                                               LSOURCE
                                                                                        CIN
                                                                                                                                          SOURCE
                                                                                                  8
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
                                                                                                             RSOURCE
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
                                                                                                                              RLSOURCE
                                                                     S1A
                                                                               OS2A
res.rbreak n17 n18 = 1, tc1 = 1.06e-3, tc2 = 0
                                                                                                                  RBREAK
                                                                         13
8
res.rdbody n71 n5 = 2.21e-2, tc1 = -6.25e-4, tc2 = -1.11e-6
                                                                                                              17
res.rdbreak n72 n5 = 3.36e-1, tc1 = 1.25e-4, tc2 = 1.34e-6
                                                                                                                             RVTEMP
res.rdrain n50 n16 = 3.00e-2, tc1 = 1.23e-2, tc2 = 2.58e-5
                                                                               o S2B
res.rgate n9 n20 = 3.37
                                                                                        CB
                                                              CA
res.rldrain n2 n5 = 10
                                                                                                            ΙT
res.rlgate n1 n9 = 15
                                                                                                                               VBAT
res.rlsource n3 n7 = 4.86
                                                                        EGS
                                                                                     EDS
res.rslc1 n5 n51 = 1e-6, tc1 = 1e-3, tc2 = 1e-6
                                                                                                          8
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 3.80e-2, tc1 = 0, tc2 = 0
                                                                                                                 RVTHRES
res.rvtemp n18 n19 = 1, tc1 = -1.11e-3, tc2 = 0
res.rvthres n22 n8 = 1, tc1 = -2.19e-3, tc2 = -4.97e-6
spe.ebreak n11 n7 n17 n18 = 67.8
\frac{1}{100} spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw vcsp.s2b n13 n15 n14 n13 = model=s2bmod
v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51, n'50) = ((v(n5, n51)/(1e-9+abs(v(n5, n51))))^*((abs(v(n5, n51)*1e6/105))^{**} 2))
```

SPICE Thermal Model JUNCTION th REV 1June 1999 HUFA76407DK8 Copper Area = 0.02 in^2 CTHERM1 th 8 8.5e-4 RTHERM1 CTHERM1 CTHERM2 8 7 1.8e-3 CTHERM3 7 6 5.0e-3 8 CTHERM4 6 5 1.3e-2 CTHERM5 5 4 4.0e-2 RTHERM2 CTHERM2 CTHERM6 4 3 9.0e-2 CTHERM7 3 2 4.0e-1 CTHERM8 2 tl 1.4 7 RTHERM1 th 8 3.5e-2 RTHERM3 CTHERM3 RTHERM2 8 7 6.0e-1 RTHERM3 7 6 2 6 RTHERM4 6 5 8 RTHERM5 5 4 18 RTHERM6 4 3 39 RTHERM4 CTHERM4 RTHERM7 3 2 42 RTHERM8 2 tl 48 5 SABER Thermal Model RTHERM5 CTHERM5 Copper Area = 0.02 in^2 4 template thermal model th tl thermal cth, tl RTHERM6 CTHERM6 ctherm.ctherm1 th 8 = 8.5e-4 ctherm.ctherm287 = 1.8e-33 ctherm.ctherm376 = 5.0e-3ctherm.ctherm4 65 = 1.3e-2RTHERM7 CTHERM7 ctherm.ctherm5 5 4 = 4.0e-2ctherm.ctherm6 43 = 9.0e-22 ctherm.ctherm7 3 2 = 4.0e-1ctherm.ctherm8 2 tl = 1.4 RTHERM8 CTHERM8 rtherm.rtherm1 th 8 = 3.5e-2 rtherm.rtherm2 8 7 = 6.0e-1 rtherm.rtherm376 = 2rtherm.rtherm4 6 5 = 8**AMBIENT** tl rtherm.rtherm554 = 18rtherm.rtherm6 4 3 = 39 rtherm.rtherm732 = 42rtherm.rtherm8 2 tl = 48

TABLE 1. THERMAL MODELS

COMPONENT	0.02 in ²	0.14 in ²	0.257 in ²	0.38 in ²	0.493 in ²
CTHERM6	9.0e-2	1.3e-1	1.5e-1	1.5e-1	1.5e-1
CTHERM7	4.0e-1	6.0e-1	4.5e-1	6.5e-1	7.5e-1
CTHERM8	1.4	2.5	2.2	3	3
RTHERM6	39	26	20	20	20
RTHERM7	42	32	31	29	23
RTHERM8	48	35	38	31	25

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FAST ® SMART START™ VCX^{TM} ACEx™ OPTOLOGIC™ STAR*POWER™ FASTr™ Bottomless™ OPTOPLANAR™ Stealth™ CoolFET™ FRFET™ PACMANTM SuperSOT™-3 CROSSVOLT™ GlobalOptoisolator™ POP™ SuperSOT™-6 DenseTrench™ GTO™ Power247™ $\mathsf{HiSeC^{\mathsf{TM}}}$ SuperSOT™-8 DOME™ PowerTrench® SyncFET™ ISOPLANAR™ EcoSPARK™ QFET™ TinyLogic™ E²CMOSTM LittleFET™ OSTM EnSigna™ MicroFET™ TruTranslation™ QT Optoelectronics™ MicroPak™ UHC™ FACT™ Quiet Series™ UltraFET® FACT Quiet Series™ MICROWIRE™ SILENT SWITCHER®

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H4