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Low Charge Injection 32-Channel High Voltage Analog Switch

Features

- 32-Channel high voltage analog switch
- 2:1 Multiplexer / Demultiplexer
- 3.3V or 5.0V CMOS input logic level
- 20MHz data shift clock frequency
- HVCMOS technology for high performance
- Very low quiescent power dissipation -10µA
- Low parasitic capacitance
- DC to 50MHz analog signal frequency
- -60dB typical OFF-isolation at 5.0MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages

Applications

- Medical ultrasound imaging
- NDT metal flaw detection
- Piezoelectric transducer drivers
- Inkjet printer heads
- Optical MEMS modules

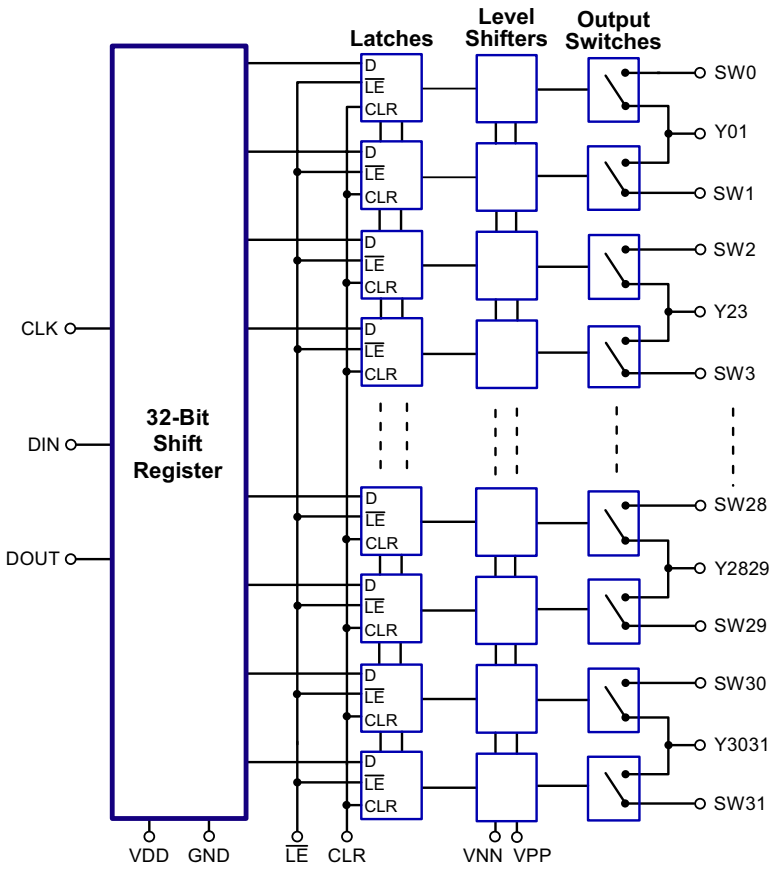
General Description

The Supertex HV2801 is a low charge injection 32-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers.

Input data are shifted into a 32-bit shift register that can then be retained in a 32-bit latch. To reduce any possible clock feed through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN}: +40V/-160V, +100V/-100V, and +160V/-40V.

Block Diagram

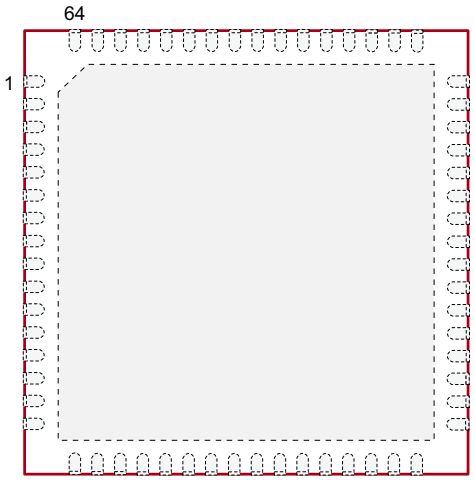


Ordering Information

Part Number	Package Option	Packing
HV2801K6-G	64-Lead QFN (9x9)	260/Tray

-G indicates package is RoHS compliant ('Green')

Pin Configuration



64-Lead QFN (K6)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic supply	-0.5V to +6.5V
V_{PP}-V_{NN} differential supply	220V
V_{PP} positive supply	-0.5V to V_{NN} +200V
V_{NN} negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	1.5W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or

64-Lead QFN (K6)

Typical Thermal Resistance

Package	θ_{ja}
64-Lead QFN	21°C/W

Recommended Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	+40V to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0V to 0.1V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1.0msec.*

DC Electrical Characteristics *(Over recommended operating conditions unless otherwise specified)*

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I_{SIG} = 5.0mA	V_{PP} = +40V, V_{NN} = -160V
		-	25	-	22	27	-	32		I_{SIG} = 200mA	
		-	25	-	22	27	-	30		I_{SIG} = 5.0mA	V_{PP} = +100V, V_{NN} = -100V
		-	18	-	18	24	-	27		I_{SIG} = 200mA	
		-	23	-	20	25	-	30		I_{SIG} = 5.0mA	V_{PP} = +160V, V_{NN} = -40V
		-	22	-	16	25	-	27		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +100V, V_{NN} = -100V	
R_{ONL}	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V_{SIG} = V_{PP} -10V, I_{SIG} = 1A	
I_{SOL}	Switch OFF-leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V, V_{NN} +10V	
V_{OS}	DC offset switch OFF	-	300	-	100	300	-	300	mV	100kΩ load	
	DC offset switch ON	-	500	-	100	500	-	500			
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches OFF	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-			
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches ON, I_{SW} = 5.0mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-			
I_{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%	
f_{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	16	-	-	20	-	22	mA	V_{PP}= +40V, V_{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	14	-	-	14	-	14		V_{PP}= +100V, V_{NN} = -100V	
		-	14	-	-	14	-	14		V_{PP}= +160V, V_{NN} = -40V	
I_{NN}	Average V_{NN} supply current	-	16	-	-	20	-	22	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	14	-	-	14	-	14		V_{PP}= +100V, V_{NN} = -100V	
		-	14	-	-	14	-	14		V_{PP}= +160V, V_{NN} = -40V	
I_{DD}	Average V_{DD} supply current	-	8.0	-	-	8.0	-	8.0	mA	f_{CLK} = 5.0MHz, V_{DD} = 5.0V	
I_{DDQ}	Quiescent V_{DD} supply current	-	10	-	-	10	-	10	µA	All logic inputs are static	
I_{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} -0.7V	
I_{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

** See Test Circuits on page 5*

AC Electrical Characteristics *(Over recommended operating conditions unless otherwise specified)*

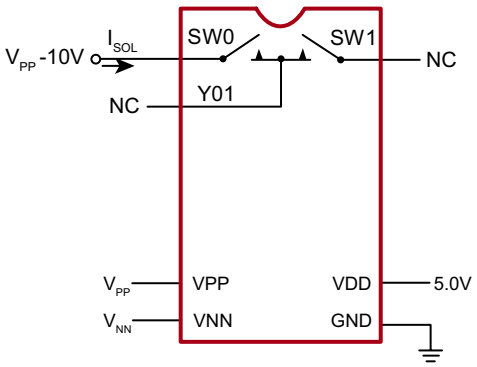
Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	V_{DD} = 3.0V
		12	-	-	12	-	12	-		V_{DD} = 5.0V
t_{DO}	Clock delay time to data out	8.0	40	8.0	19	40	8.0	40	ns	V_{DD} = 3.0V
		8.0	30	8.0	15	30	8.0	30		V_{DD} = 5.0V
t_{WCLR}	Time width of CLR	55	-	55	-	-	55	-	ns	---
t_{SU}	Set up time data to clock	21	-	21	-	-	21	-	ns	V_{DD} = 3.0V
		7.0	-	7.0	-	-	7.0	-		V_{DD} = 5.0V
t_H	Hold time data from clock	5.0	-	5.0	-	-	5.0	-	ns	V_{DD} = 3.0V
		7.0	-	7.0	-	-	7.0	-		V_{DD} = 5.0V
f_{CLK}	Clock frequency	-	8	-	-	8	-	8	MHz	V_{DD} = 3.0V
		-	20	-	-	20	-	20		V_{DD} = 5.0V
t_R, t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
t_{ON}	Turn ON time	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = V_{PP} -10V, R_{LOAD} = 10kΩ
t_{OFF}	Turn OFF time	-	5.0	-	-	5.0	-	5.0		
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	V_{PP} = +40V, V_{NN} = -160V
		-	20	-	-	20	-	20		V_{PP} = +100V, V_{NN} = -100V
		-	20	-	-	20	-	20		V_{PP} = +160V, V_{NN} = -40V
K_O	OFF isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0kΩ//15pF load
		-58	-	-58	-60	-	-58	-		f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	OFF capacitance SW to GND	-	14	-	9.0	14	-	14	pF	V_{SIG} = 0, f = 1.0MHz, both SW OFF
	OFF capacitance Y to GND	-	28	-	18	28	-	28		
$C_{SG(ON)}$	ON capacitance SW to GND	-	33	-	23	33	-	33	pF	V_{SIG} = 0, f = 1.0MHz, one SW ON, one SW OFF
	ON capacitance Y to GND	-	33	-	23	33	-	33		
$+V_{SPK}$	Output voltage spike SW	-	-	-	-	+150	-	-	mV	V_{PP} = +40V, V_{NN} = -160V R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	-150	-	-		
$+V_{SPK}$		-	-	-	-	+150	-	-		V_{PP} = +100V, V_{NN} = -100V R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	-150	-	-		
$+V_{SPK}$		-	-	-	-	+150	-	-		V_{PP} = +160V, V_{NN} = -40V R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	-150	-	-		

** See Test Circuits on page 5*

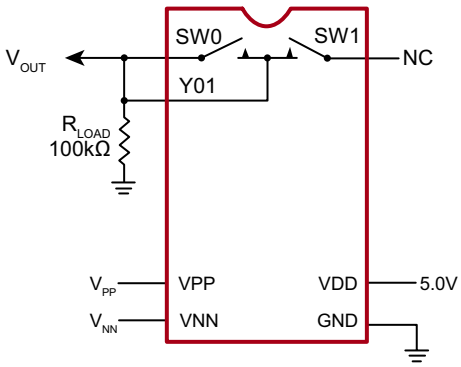
AC Electrical Characteristics *(Over recommended operating conditions unless otherwise specified)*

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
$+V_{SPK}$	Output voltage spike Y	-	-	-	-	+150	-	-	mV	V_{PP} = +40V, V_{NN} = -160V R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	-150	-	-		
$+V_{SPK}$		-	-	-	-	+150	-	-		V_{PP} = +100V, V_{NN} = -100V R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	-150	-	-		
$+V_{SPK}$		-	-	-	-	+150	-	-		V_{PP} = +160V, V_{NN} = -40V R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	-150	-	-		
QC	Charge injection	-	-	-	820	-	-	-	pC	V_{PP} = +40V, V_{NN} = -160V
		-	-	-	600	-	-	-		V_{PP} = +100V, V_{NN} = -100V
		-	-	-	350	-	-	-		V_{PP} = +160V, V_{NN} = -40V

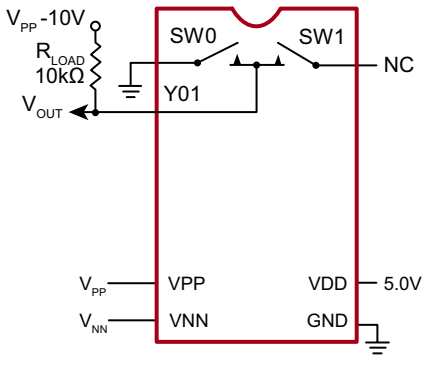
Test Circuits



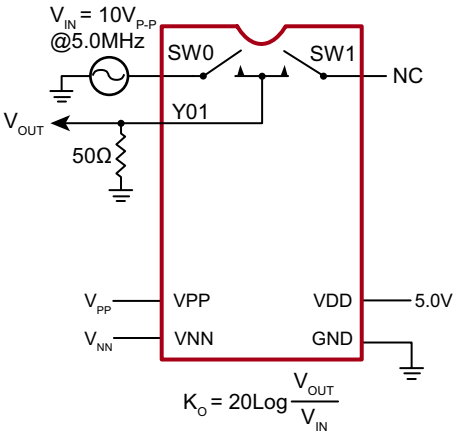
Switch OFF Leakage



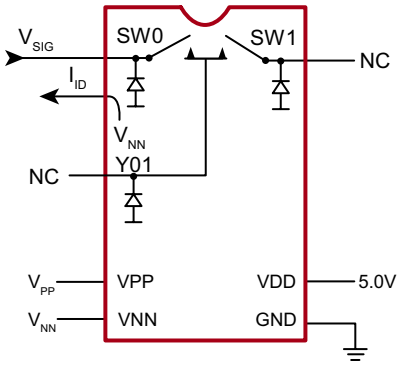
DC Offset ON/OFF



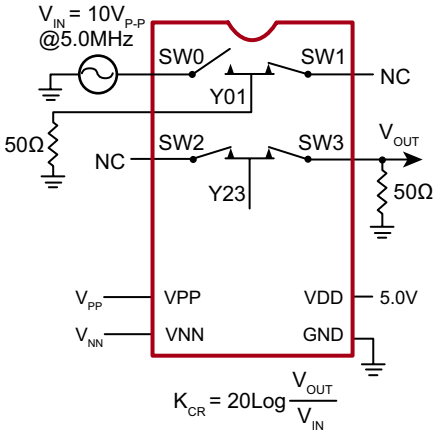
T_{ON}/T_{OFF} Test Circuit



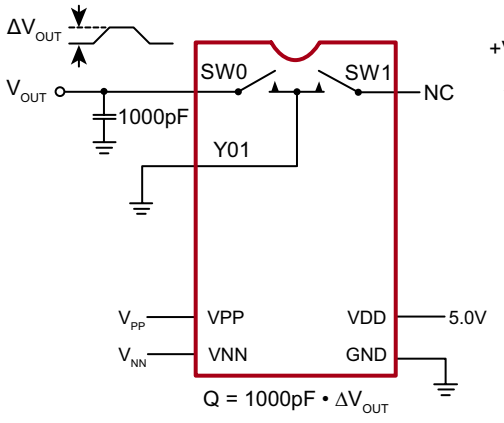
OFF Isolation



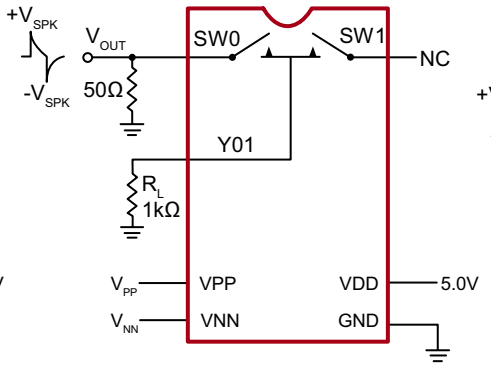
Isolation Diode Current



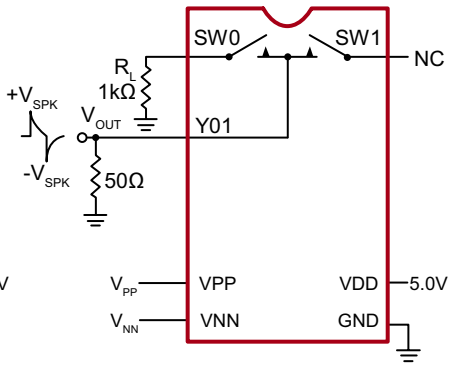
Crosstalk



Charge Injection



Output Voltage Spike SW



Output Voltage Spike Y

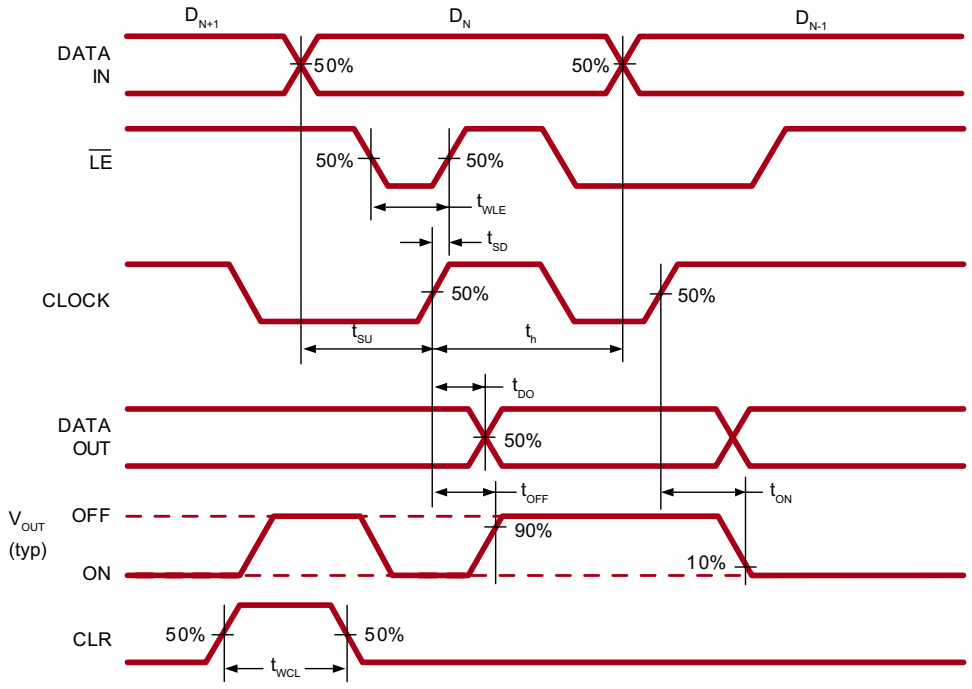
Truth Table

D0	D1	...	D15	D16	...	D31	$\overline{LE}$	CLR	SW0	SW1	...	SW15	SW16	...	SW31
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		L	-		-	L	L	-	-		OFF	-		-
-	-		H	-		-	L	L	-	-		ON	-		-
-	-	...	-	L	...	-	L	L	-	-	...	-	OFF	...	-
-	-		-	H		-	L	L	-	-		-	ON		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Notes:

1. *The 32 switches operate independently.*
2. *Serial data is clocked in on the L to H transition of the CLK.*
3. *All 32 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.*
4. *D_{OUT} is high when data in the register 31 is high.*
5. *Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.*
6. *The CLR clear input overrides all other inputs.*

Logic Timing Waveforms



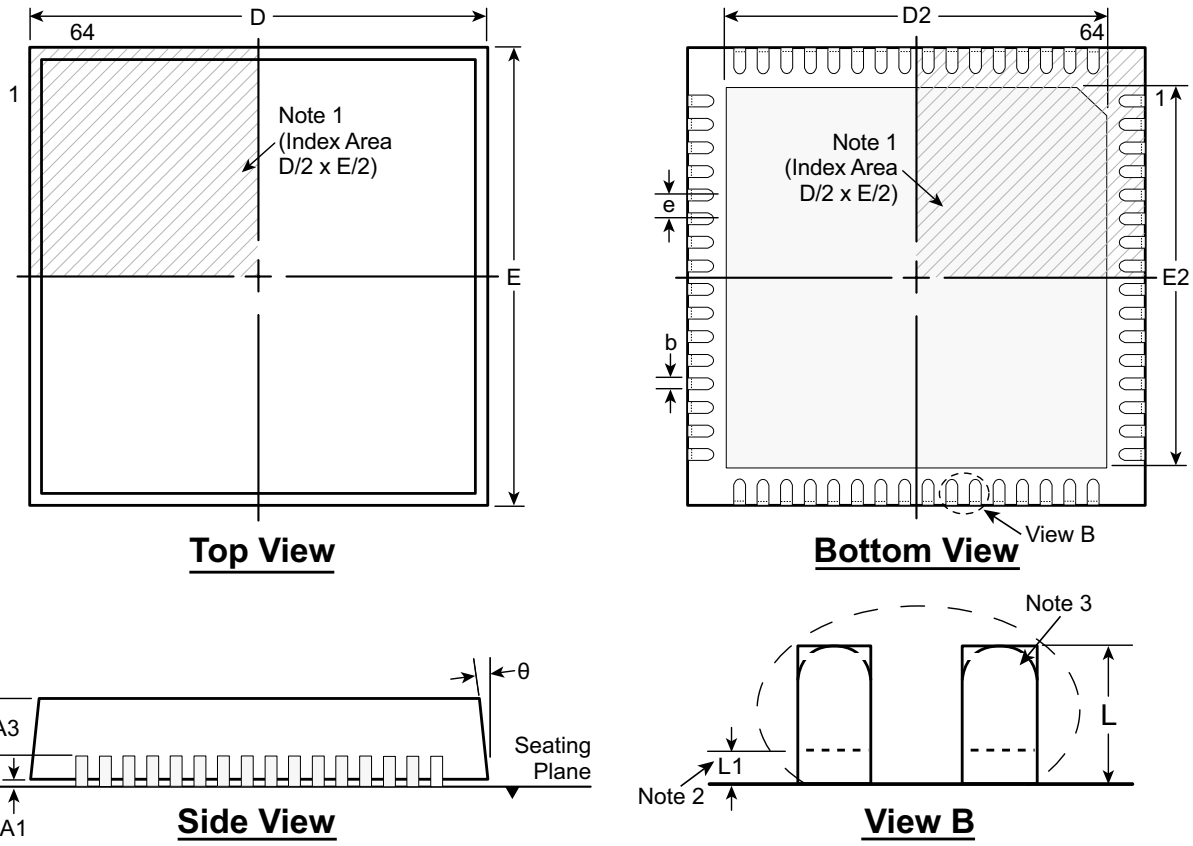
Pin Function

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	SW30	17	SW2	33	Y1213	49	SW19
2	Y3031	18	Y23	34	SW13	50	SW20
3	SW31	19	SW3	35	VPP	51	Y2021
4	NC	20	SW4	36	NC	52	SW21
5	CLR	21	Y45	37	VNN	53	SW22
6	NC	22	SW5	38	SW14	54	Y2223
7	$\overline{\text{LE}}$	23	SW6	39	Y1415	55	SW23
8	CLK	24	Y67	40	SW15	56	SW24
9	VDD	25	SW7	41	SW16	57	Y2425
10	DIN	26	SW8	42	Y1617	58	SW25
11	GND	27	Y89	43	SW17	59	SW26
12	DOUT	28	SW9	44	VNN	60	Y2627
13	NC	29	SW10	45	NC	61	SW27
14	SW0	30	Y1011	46	VPP	62	SW28
15	Y01	31	SW11	47	SW18	63	Y2829
16	SW1	32	SW12	48	Y1819	64	SW29

VSUB (Thermal Pad)	The central thermal pad on the bottom of package must be connected to VNN externally

64-Lead QFN Package Outline (K6)

9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch



Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.20	8.90	7.60	8.90	7.60	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	9.00	7.70	9.00	7.70		0.40	-	-
	MAX	1.00	0.05		0.30	9.10	7.80	9.10	7.80		0.50	0.15	14°

Drawings are not to scale.
Supertex Doc.#: *DSPD-64QFNK69X9P050, Version B020112*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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