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HV2803/HV2903/HV2904

No High-Voltage Bias, Low Harmonic Distortion, 32-Channel, High-Voltage Analog Switch

Features

- 32-Channel, High-Voltage Analog Switch
- No High-Voltage Supplies Required
- 32-Channel, Single-Pole, Single-Throw (SPST) Individual Switching or Bank Switching
- 3.3V CMOS Input Logic Level
- 66 MHz Data Shift Clock Frequency
- Silicon-on-Insulator (SOI) High-Voltage Technology for High Performance
- Standby mode for Low-Power Dissipation
- Low-Parasitic Capacitance
- DC to 50 MHz Analog Small-Signal Frequency
- 200 kHz to 50 MHz Large-Signal Frequency
- -70 dB Typical Off Isolation at 5.0 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Integrated Bleed Resistors on the Outputs (both sides for HV2903, one side for HV2904)

Applications

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT) Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Heads
- Optical MEMS Modules

General Description

The HV2803/HV2903/HV2904 devices are low harmonic distortion, low charge injection, 32-channel, high-voltage analog switches without high-voltage supplies. They are intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers.

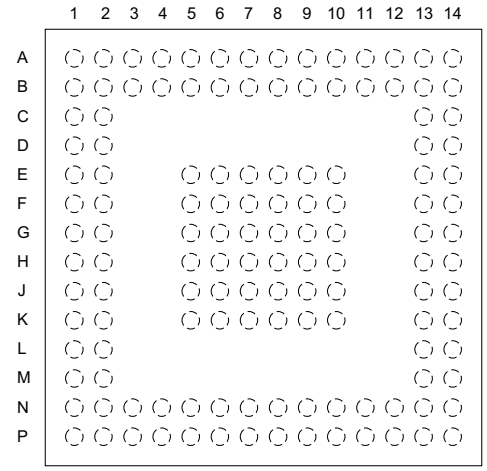
The HV2903 device has integrated bleed resistors at both sides of the switches; the HV2904 device has bleed resistors at one side only, while the HV2803 device has no bleed resistors. The bleed resistor eliminates voltage build-up on capacitive loads, such as piezoelectric transducers.

The HV2803/HV2903/HV2904 devices have two modes of operation determined by the MODE pin input. MODE input high enables an individual Switching mode of 32-channel SPST switches and MODE input low enables a Bank Switching mode of 16-Pole Double-Throw (16PDT) switches to support bank switching for probe selection.

The devices require only ±6V or ±5V low-voltage supplies and no high-voltage supplies. However, all of the analog switches can transmit ±100V high-voltage pulses.

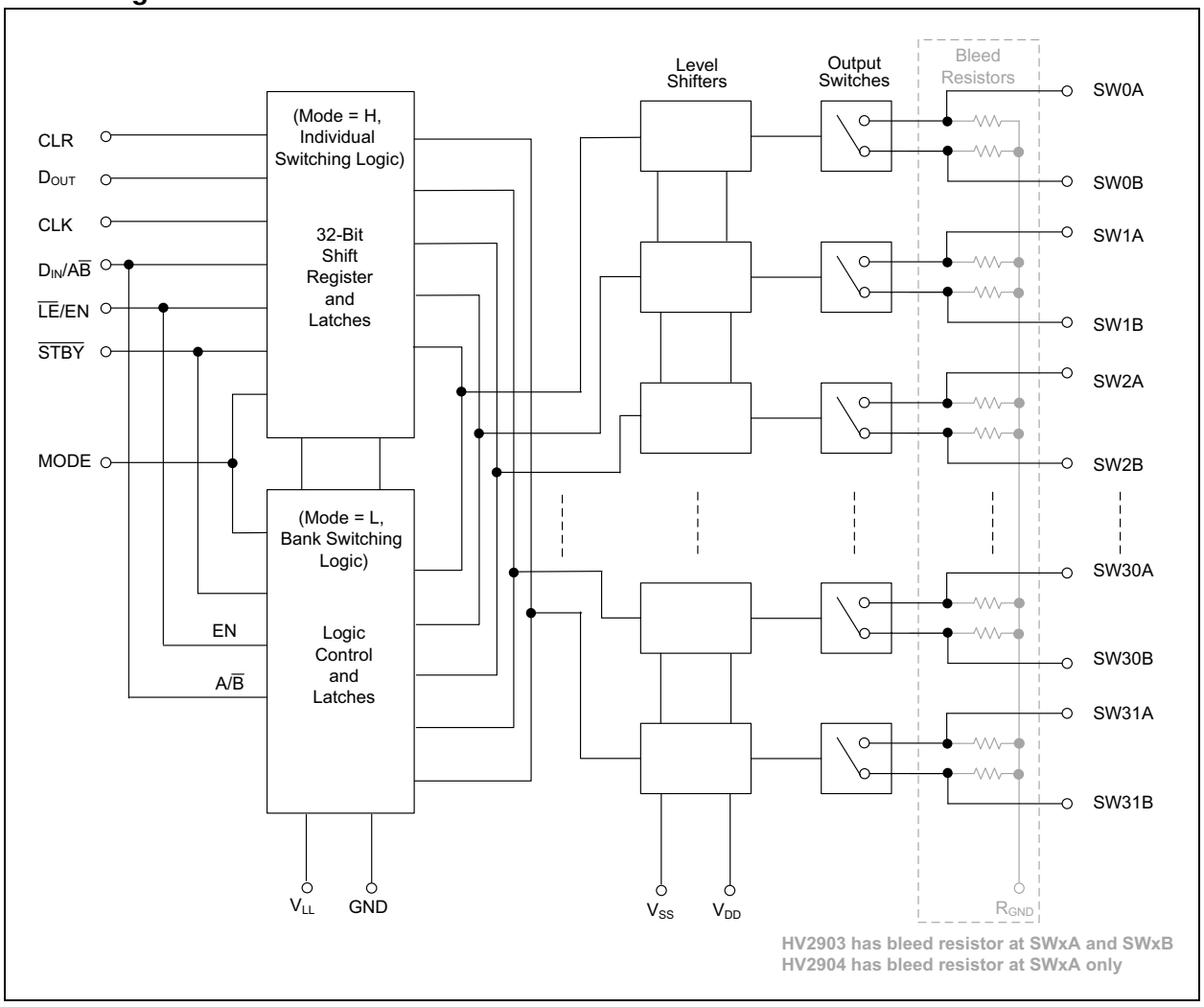
Package Type

HV2803/HV2903/HV2904
12 x 12 x 1.20 mm TFBGA
(Top View*)



* See **Section 2.0 "Package Pin Configuration and Function Description"**.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply Voltage (V_{LL})..... -0.5V to +6.6V
Positive Supply Voltage (V_{DD})..... -0.5V to +6.6V
Negative Supply Voltage (V_{SS}) ..... +0.5V to -6.6V
Logic Input Voltage (V_{IN})..... -0.5V to V_{LL} + 0.3V
DGND to GND ..... -0.3V to +0.3V
Analog Signal Range (V_{SIG})..... -110V to +110V
Peak Analog Signal Current/Channel (I_{PK})..... 3A

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1,2,3)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{LL}	3	—	3.6	V	
Positive Supply Voltage	V_{DD}	4.5	—	6.3	V	
Negative Supply Voltage	V_{SS}	-6.3	—	-4.5	V	
High-Level Input Voltage	V_{IH}	0.9 V_{LL}	—	V_{LL}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.1 V_{LL}	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	-100	—	100	V	

Note 1: Power-up sequence is V_{SS}, V_{DD} and then V_{LL}. Power-down sequence is the reverse of power-up.
2: V_{SIG} must be $V_{SS} \le V_{SIG} \le V_{DD}$ or floating during power-up/down transition.
3: Rise and fall times of power supplies, V_{LL}, V_{DD} and V_{SS} should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = 6.0V, V_{SS} = -6.0V, V_{LL} = 3.3V, T_{AMB} = +25°C. **Boldface** specifications apply over the full operating temperature range.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Small-Signal Switch On-Resistance	R_{ONS}	—	10	**15**	Ω	I_{SIG} = 5 mA
		—	10.4	—	Ω	V_{DD} = +5V, V_{SS} = -5V, I_{SIG} = 5 mA (**Note 1**)
		—	10	**15**	Ω	I_{SIG} = 200 mA
Small-Signal Switch On-Resistance Matching	ΔR_{ONS}	—	5	**20**	%	I_{SIG} = 5 mA
Large-Signal Switch On-Resistance	R_{ONL}	—	9	—	Ω	V_{SIG} = 90V, I_{SIG} = 1A (**Note 1**)
Value of Output Bleed Resistor (**HV2903**/**HV2904** only)	R_{INT}	20	35	50	kΩ	Output switch to R_{GND}, I_{RINT} = 0.1 mA
Switch Off Leakage per SW	I_{SOL}	—	—	**3**	µA	At 49 µs with V_{SIG} = +100V, 50 µs pulse (see Figure 3-1)
		—	—	**3**	µA	At 49 µs with V_{SIG} = -100V, 50 µs pulse (see Figure 3-1)

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, V_{DD} = 6.0V, V_{SS} = -6.0V, V_{LL} = 3.3V, T_{AMB} = +25°C. **Boldface** specifications apply over the full operating temperature range.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
HV2803						
Switch Off Bias per SW	I_{SOB}	—	—	**3**	µA	V_{SIG} = +100V, 400 µs pulse (see Figure 3-2)
		—	—	**4**	mA	V_{SIG} = -100V, 12 µs pulse (see Figure 3-2) **(Note 1)**
HV2903						
Switch Off Bias per SW	I_{SOB}	—	—	**3**	µA	V_{SIG} = +100V, 400 µs pulse (see Figure 3-2)
		—	—	**8**	mA	V_{SIG} = -100V, 12 µs pulse (see Figure 3-2) **(Note 1)**
HV2904						
Switch Off Bias per SWA (with bleed resistor)	I_{SOB}	—	—	**3**	µA	V_{SIG} = +100V, 400 µs pulse (see Figure 3-2)
		—	—	**8**	mA	V_{SIG} = -100V, 12 µs pulse (see Figure 3-2) **(Note 1)**
Switch Off Bias per SWB (without bleed resistor)		—	—	**3**	µA	V_{SIG} = +100V, 400 µs pulse (see Figure 3-2)
		—	—	**4**	mA	V_{SIG} = -100V, 12 µs pulse (see Figure 3-2) **(Note 1)**
Switch Off DC Offset	V_{OS}	—	1	**10**	mV	R_{LOAD} = 25 kΩ (HV2803), 50 kΩ (HV2904) No load (HV2903) (see Figure 3-3)
Switch On DC offset		—	1	**10**		
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	**7**	mA	All switches off
Quiescent V_{SS} Supply Current	I_{SSQ}	—	—	**5**	mA	
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	**8**	mA	All switches on, V_{SW} = 1V
Quiescent V_{SS} Supply Current	I_{SSQ}	—	—	**8**	mA	
Quiescent V_{LL} Supply Current	I_{LLQ}	—	1	**10**	µA	All logic inputs are static
Standby V_{DD} Supply Current	I_{DDS}	—	63	**150**	µA	$\overline{STBY}$ = 0V
Standby V_{SS} Supply Current	I_{SSS}	—	13	**100**	µA	
Standby V_{LL} Supply Current	I_{LLS}	—	—	**2**	µA	$\overline{STBY}$ = 0V
Switch Output Peak Current	I_{SW}	**2**	3	—	A	V_{SIG} duty cycle < 0.1% **(Note 1)**
Output Switching Frequency	f_{SW}	—	—	**50**	kHz	Duty cycle = 50% **(Note 1)**
Average V_{DD} Supply Current	I_{DD}	—	11	**25**	mA	All output switches are turning on and off at 50 kHz with no load, V_{SIG} = 0V
Average V_{SS} Supply Current	I_{SS}	—	9	**20**	mA	
Average V_{LL} Supply Current	I_{LL}	—	3	**6**	mA	f_{CLK} = 5.0 MHz
Data Out Source Current	I_{SOR}	**10**	—	—	mA	V_{OUT} = V_{LL} – 0.7V
Data Out Sink Current	I_{SINK}	**10**	—	—	mA	V_{OUT} = 0.7V
Logic Input Capacitance	C_{IN}	—	8	—	pF	**(Note 2)**

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = 6.0V, V_{SS} = -6.0V, V_{LL} = 3.3V, T_{AMB} = +25°C. **Boldface** specifications apply over the full operating temperature range.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Setup Time before $\overline{LE}$/EN Rises	t_{SD}	**25**	—	—	ns	**(Note 1)**
Time Width of $\overline{LE}$/EN	t_{WLE}	**12**	—	—	ns	**(Note 1)**
Clock Delay Time to Data Out	t_{DO}	—	—	**13.5**	ns	
Time Width of CLR	t_{WCLR}	**55**	—	—	ns	**(Note 1)**
Setup Time Data to Clock	t_{SU}	**1.5**	—	—	ns	**(Note 1)**
Hold Time Data from Clock	t_H	**1.5**	—	—	ns	**(Note 1)**
Clock Frequency	f_{CLK}	—	—	**66**	MHz	50% duty cycle, $f_{DIN} = (1/2)f_{CLK}$, C_{DOUT} = 20 pF **(Note 1)**
Clock Rise and Fall Times	t_R, t_F	—	—	**50**	ns	
Turn-On Time	t_{ON}	—	—	**5**	µs	V_{SIG} = 5V, R_{LOAD} = 550Ω (see Figure 3-4)
Turn-Off Time	t_{OFF}	—	—	**5**		
Input Large-Signal Pulse Width	t_{PW}	—	—	**2.5**	µs	V_{PULSE} = 0V to ±100V, Measured at 90% amplitude (see Figure 3-5) **(Note 1)**
Wake-up Time from Standby to Digital Logic Normal Operation	t_{WU}	—	—	**10**	µs	Bank Switching mode (MODE = L)
		—	—	**10**	µs	Individual Switching mode (MODE = H) **(Note 1)**
Maximum V_{SIG} Slew Rate	dv/dt	—	—	20	V/ns	**(Note 1)**
Analog Small-Signal Frequency	f_{BWS}	—	50	—	MHz	**(Note 1)**
Off Isolation	K_O	—	-57	-51	dB	f = 5.0 MHz,1.0 kΩ/15 pF load (see Figure 3-6) **(Note 1)**
		—	-70	-65		f = 5.0 MHz, 50Ω load (see Figure 3-6) **(Note 1)**
Switch Crosstalk	K_{CR}	—	-70	-60	dB	f = 5.0 MHz, 50Ω load (see Figure 3-7) **(Note 1)**
Off Capacitance SW to GND	$C_{SG(OFF)}$	—	9	—	pF	V_{SIG} = 50 mV@1 MHz, no load **(Note 1)**
On Capacitance SW to GND	$C_{SG(ON)}$	—	27	—		
Output Voltage Spike at SWA, SWB	$+V_{SPK}$	—	—	100	mV	R_{LOAD} = 50Ω. (see Figure 3-8) **(Note 1)**
	$-V_{SPK}$	-150	—	—		
Charge Injection	QC	—	200	—	pC	See Figure 3-9 **(Note 1)**
Second Harmonic Distortion	HD2	—	-68	-60	dBc	V_{SIG} = 1.5 V_{PP} @ 5 MHz, 50Ω load **(Note 1)**
		—	-65	-60	dBc	V_{SIG} = 1.5 V_{PP} @ 5 MHz, 1 kΩ/15 pF load **(Note 1)**

Note 1: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATION

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Range						
Operating Temperature Range	T_A	0	—	+70	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+125	°C	
Package Thermal Resistance						
Thermal Resistance, 132-Ball TFBGA	θ_{JA}	—	22	—	°C/W	

1.1 Logic Timing and Truth Table

Figure 1-1 shows the timing of the AC characteristic parameters graphically.

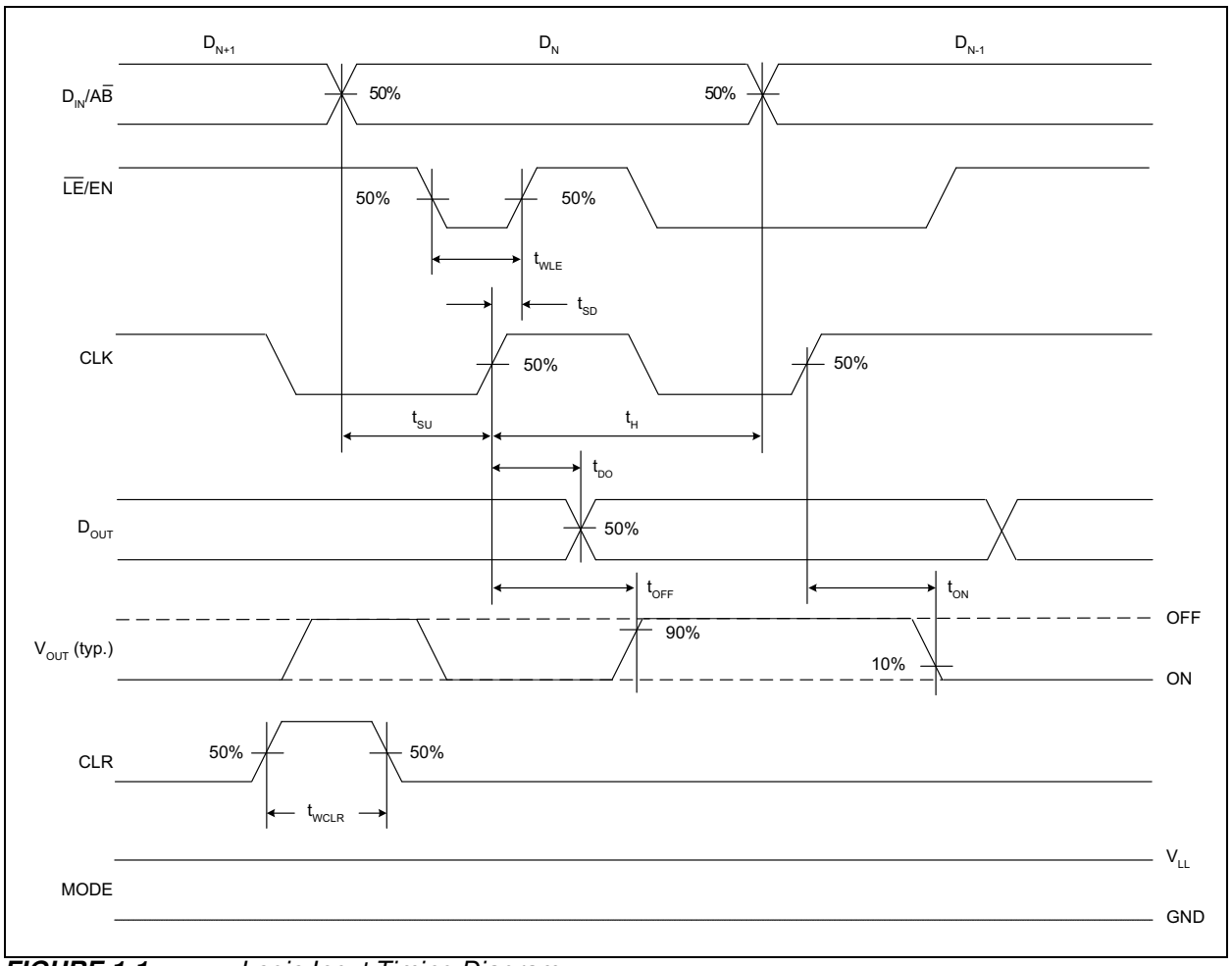


FIGURE 1-1: *Logic Input Timing Diagram.*

TABLE 1-1: TRUTH TABLE[1,2,3,4,5,6]

$\overline{STBY}$	MODE	D0	D1	...	D15	D16	...	D31	$D_{IN}/\overline{AB}$	$\overline{LE}$/EN	CLR	SW0	SW1	...	SW15	SW16	...	SW31
H	H	L	—		—	—		—	X	L	L	OFF	—		—	—		—
H	H	H	—		—	—		—	X	L	L	ON	—		—	—		—
H	H	—	L		—	—		—	X	L	L	—	OFF		—	—		—
H	H	—	H		—	—		—	X	L	L	—	ON		—	—		—
H	H	—	—		—	—		—	X	L	L	—	—		—	—		—
H	H	—	—		—	—		—	X	L	L	—	—		—	—		—
H	H	—	—		L	—		—	X	L	L	—	—		OFF	—		—
H	H	—	—	...	H	—	...	—	X	L	L	—	—	...	ON	—	...	—
H	H	—	—		—	L		—	X	L	L	—	—		—	OFF		—
H	H	—	—		—	H		—	X	L	L	—	—		—	ON		—
H	H	—	—		—	—		—	X	L	L	—	—		—	—		—
H	H	—	—		—	—		—	X	L	L	—	—		—	—		—
H	H	—	—		—	—		L	X	L	L	—	—		—	—		OFF
H	H	—	—		—	—		H	X	L	L	—	—		—	—		ON
H	H	X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
H	H	X	X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						
H	L	X	X	X	X	X	X	X	L	H	X	EVEN SWITCHES OFF & ODD SWITCHES ON						
H	L	X	X	X	X	X	X	X	H	H	X	EVEN SWITCHES ON & ODD SWITCHES OFF						
H	L	X	X	X	X	X	X	X	X	L	X	ALL SWITCHES OFF						
L	X	X	X	X	X	X	X	X	X	X	X	ALL SWITCHES OFF, STANBY STATE						

Legend: X = Don't care; L = Low; H = High.

Note 1: The 32 switches operate independently (when MODE = H).

2: Serial data is clocked in on the L to H transition of the CLK (when MODE = H).

3: All 32 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$/EN. When $\overline{LE}$/EN is low, the shift registers' data flows through the latch (when MODE = H).

4: D_{OUT} is high when data in Register 31 is high (when MODE = H).

5: Shift register clocking has no effect on the switch states if $\overline{LE}$/EN is high (when MODE = H).

6: The CLR (clear) input overrides all the inputs (when MODE = H).

2.0 PACKAGE PIN CONFIGURATION AND FUNCTION DESCRIPTION

This section details the pin designation for the 132-Ball TFBGA package (Figure 2-1). The description of the pins are listed in Table 2-1.

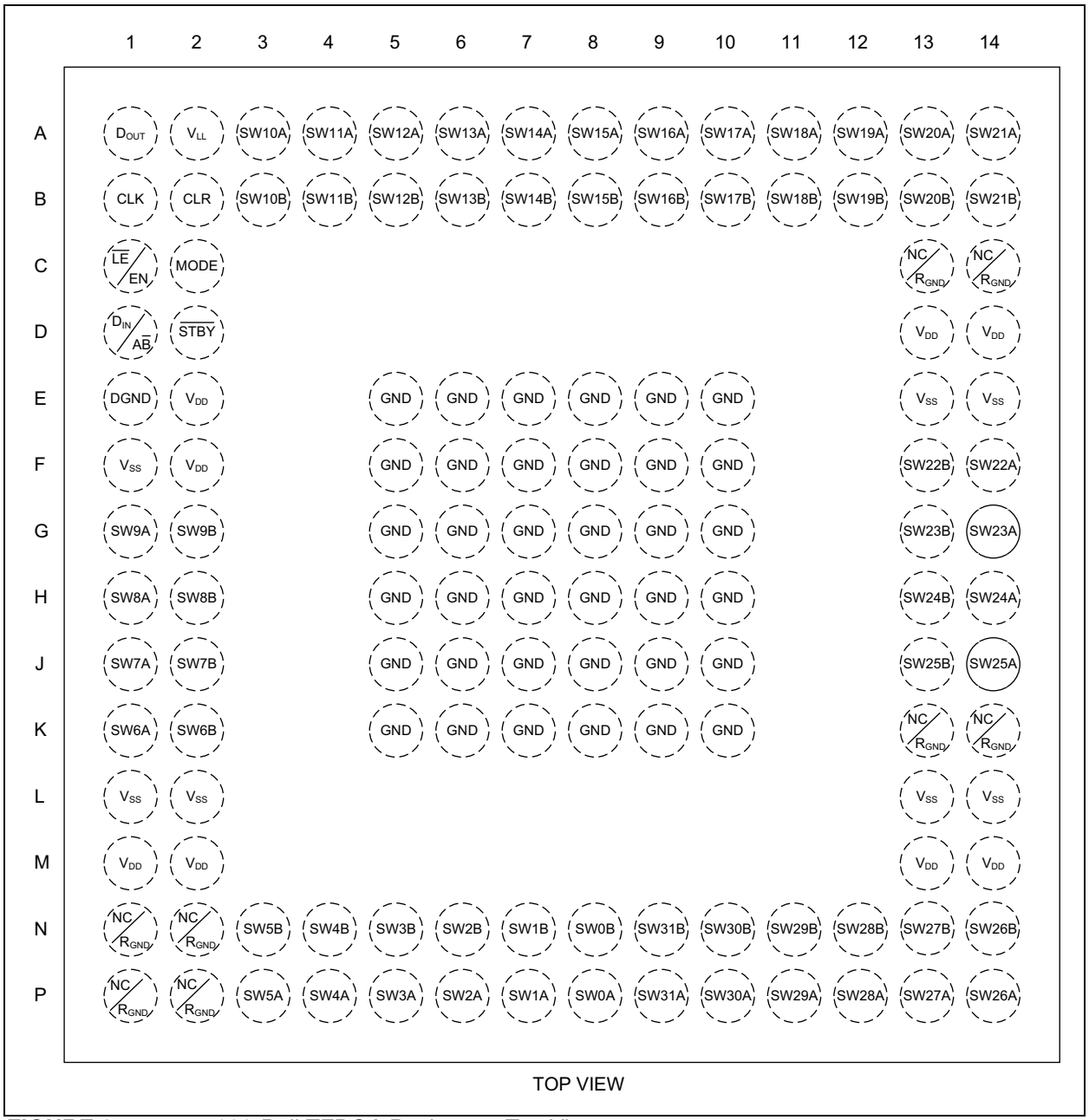


FIGURE 2-1: *132-Ball TFBGA Package – Top View.*

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol		Description
	HV2803	HV2903, HV2904	
A1	D_{OUT}	D_{OUT}	Data Out Logic Output
A2	V_{LL}	V_{LL}	Logic Supply Voltage
A3	SW10A	SW10A	Analog Switch 10 Terminal A
A4	SW11A	SW11A	Analog Switch 11 Terminal A
A5	SW12A	SW12A	Analog Switch 12 Terminal A
A6	SW13A	SW13A	Analog Switch 13 Terminal A
A7	SW14A	SW14A	Analog Switch 14 Terminal A
A8	SW15A	SW15A	Analog Switch 15 Terminal A
A9	SW16A	SW16A	Analog Switch 16 Terminal A
A10	SW17A	SW17A	Analog Switch 17 Terminal A
A11	SW18A	SW18A	Analog Switch 18 Terminal A
A12	SW19A	SW19A	Analog Switch 19 Terminal A
A13	SW20A	SW20A	Analog Switch 20 Terminal A
A14	SW21A	SW21A	Analog Switch 21 Terminal A
B1	CLK	CLK	Clock Logic Input for Shift Register
B2	CLR	CLR	Latch Clear Logic Input
B3	SW10B	SW10B	Analog Switch 10 Terminal B
B4	SW11B	SW11B	Analog Switch 11 Terminal B
B5	SW12B	SW12B	Analog Switch 12 Terminal B
B6	SW13B	SW13B	Analog Switch 13 Terminal B
B7	SW14B	SW14B	Analog Switch 14 Terminal B
B8	SW15B	SW15B	Analog Switch 15 Terminal B
B9	SW16B	SW16B	Analog Switch 16 Terminal B
B10	SW17B	SW17B	Analog Switch 17 Terminal B
B11	SW18B	SW18B	Analog Switch 18 Terminal B
B12	SW19B	SW19B	Analog Switch 19 Terminal B
B13	SW20B	SW20B	Analog Switch 20 Terminal B
B14	SW21B	SW21B	Analog Switch 21 Terminal B
C1	$\overline{LE}$/EN	$\overline{LE}$/EN	Latch Enable Logic Input, Low Active when in Individual Switching mode; Enable Logic Input when in Bank Switching mode
C2	MODE	MODE	Logic Input to decide the Switching mode; L = Bank Switching, H = Individual Switching
C13, C14	NC	R_{GND}	No Connect/Ground for Bleed Resistor
D1	$D_{IN}/A\overline{B}$	$D_{IN}/A\overline{B}$	Data in Logic Input when in Individual Switching mode; Logic Input to select Even SWs Bank or Odd SWs Bank when in Bank Switching mode
D2	$\overline{STBY}$	$\overline{STBY}$	Logic Input for Standby State; L = Standby mode (default), H = Normal Operation
D13, D14	V_{DD}	V_{DD}	Positive Supply Voltage
E1	DGND	DGND	Digital Ground
E2	V_{DD}	V_{DD}	Positive Supply Voltage
E5-E10	GND	GND	Ground
E13, E14	V_{SS}	V_{SS}	Negative Supply Voltage

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2803	HV2903, HV2904	
F1	V_{SS}	V_{SS}	Negative Supply Voltage
F2	V_{DD}	V_{DD}	Positive Supply Voltage
F5-F10	GND	GND	Ground
F13	SW22B	SW22B	Analog Switch 22 Terminal B
F14	SW22A	SW22A	Analog Switch 22 Terminal A
G1	SW9A	SW9A	Analog Switch 9 Terminal A
G2	SW9B	SW9B	Analog Switch 9 Terminal B
G5-G10	GND	GND	Ground
G13	SW23B	SW23B	Analog Switch 23 Terminal B
G14	SW23A	SW23A	Analog Switch 23 Terminal A
H1	SW8A	SW8A	Analog Switch 8 Terminal A
H2	SW8B	SW8B	Analog Switch 8 Terminal B
H5-H10	GND	GND	Ground
H13	SW24B	SW24B	Analog Switch 24 Terminal B
H14	SW24A	SW24A	Analog Switch 24 Terminal A
J1	SW7A	SW7A	Analog Switch 7 Terminal A
J2	SW7B	SW7B	Analog Switch 7 Terminal B
J5-J10	GND	GND	Ground
J13	SW25B	SW25B	Analog Switch 25 Terminal B
J14	SW25A	SW25A	Analog Switch 25 Terminal A
K1	SW6A	SW6A	Analog Switch 6 Terminal A
K2	SW6B	SW6B	Analog Switch 6 Terminal B
K5-K10	GND	GND	Ground
K13, K14	NC	R_{GND}	No Connect/Ground for Bleed Resistor
L1, L2	V_{SS}	V_{SS}	Negative Supply Voltage
L13, L14	V_{SS}	V_{SS}	Negative Supply Voltage
M1, M2	V_{DD}	V_{DD}	Positive Supply Voltage
M13, M14	V_{DD}	V_{DD}	Positive Supply Voltage
N1, N2	NC	R_{GND}	No Connect/Ground for Bleed Resistor
N3	SW5B	SW5B	Analog Switch 5 Terminal B
N4	SW4B	SW4B	Analog Switch 4 Terminal B
N5	SW3B	SW3B	Analog Switch 3 Terminal B
N6	SW2B	SW2B	Analog Switch 2 Terminal B
N7	SW1B	SW1B	Analog Switch 1 Terminal B
N8	SW0B	SW0B	Analog Switch 0 Terminal B
N9	SW31B	SW31B	Analog Switch 31 Terminal B
N10	SW30B	SW30B	Analog Switch 30 Terminal B
N11	SW29B	SW29B	Analog Switch 29 Terminal B
N12	SW28B	SW28B	Analog Switch 28 Terminal B
N13	SW27B	SW27B	Analog Switch 27 Terminal B
N14	SW26B	SW26B	Analog Switch 26 Terminal B

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2803	HV2903, HV2904	
P1, P2	NC	R_{GND}	No Connect/Ground for Bleed Resistor
P3	SW5A	SW5A	Analog Switch 5 Terminal A
P4	SW4A	SW4A	Analog Switch 4 Terminal A
P5	SW3A	SW3A	Analog Switch 3 Terminal A
P6	SW2A	SW2A	Analog Switch 2 Terminal A
P7	SW1A	SW1A	Analog Switch 1 Terminal A
P8	SW0A	SW0A	Analog Switch 0 Terminal A
P9	SW31A	SW31A	Analog Switch 31 Terminal A
P10	SW30A	SW30A	Analog Switch 30 Terminal A
P11	SW29A	SW29A	Analog Switch 29 Terminal A
P12	SW28A	SW28A	Analog Switch 28 Terminal A
P13	SW27A	SW27A	Analog Switch 27 Terminal A
P14	SW26A	SW26A	Analog Switch 26 Terminal A

3.0 TEST CIRCUIT EXAMPLES

This section details a few examples of test circuits.

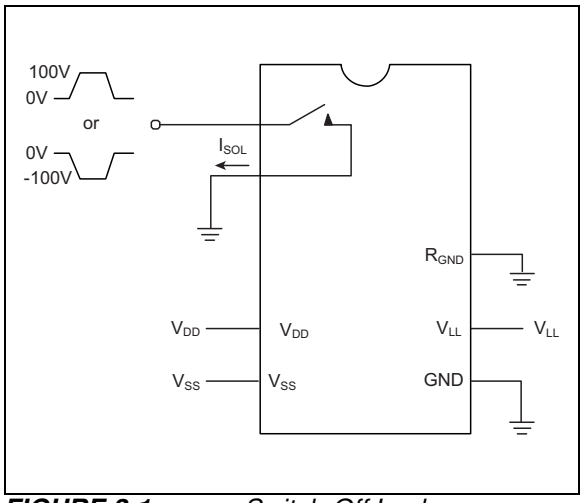


FIGURE 3-1: *Switch-Off Leakage per Switch.*

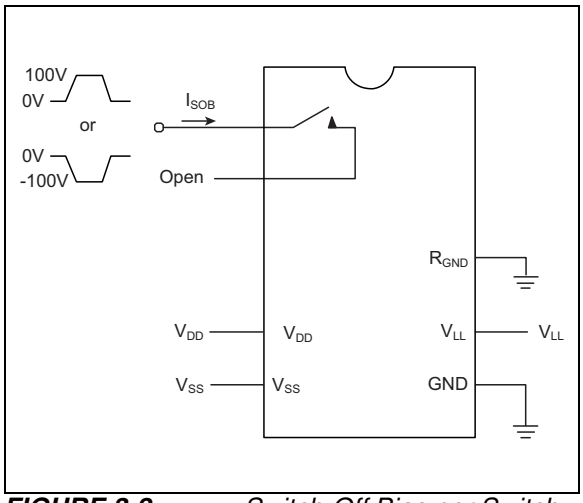


FIGURE 3-2: *Switch-Off Bias per Switch.*

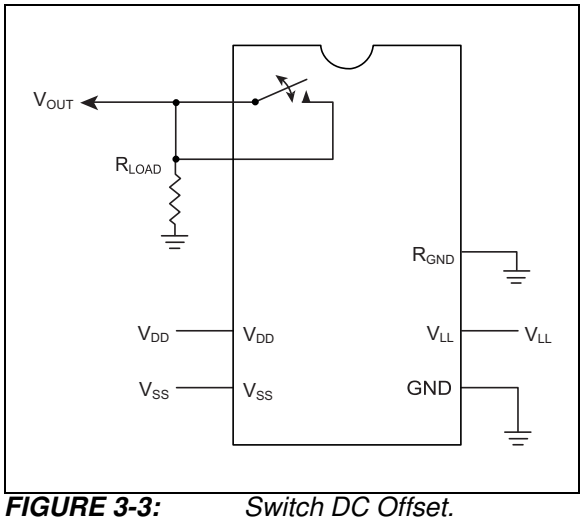


FIGURE 3-3: *Switch DC Offset.*

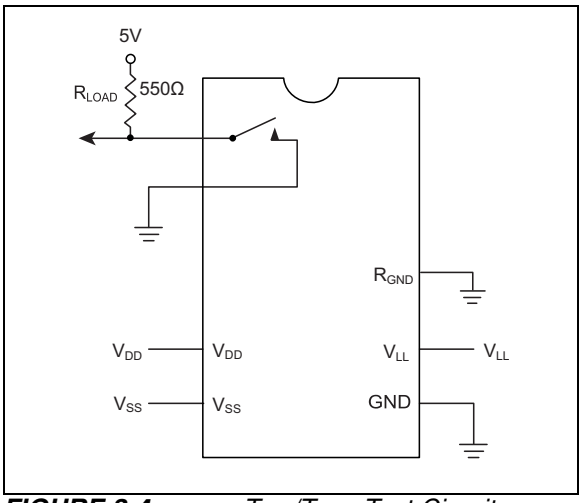


FIGURE 3-4: *T_{ON}/T_{OFF} Test Circuit.*

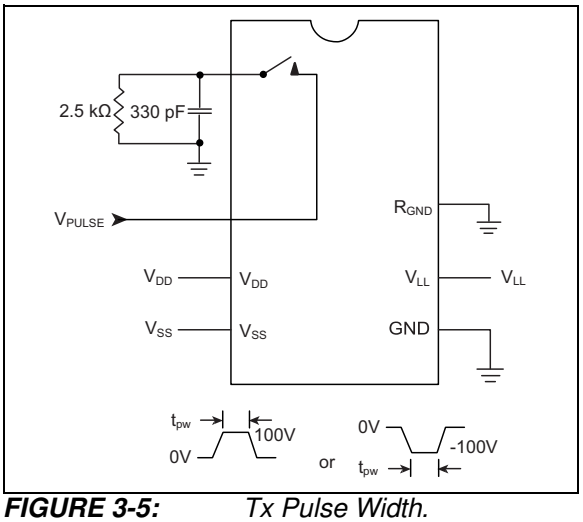


FIGURE 3-5: *Tx Pulse Width.*

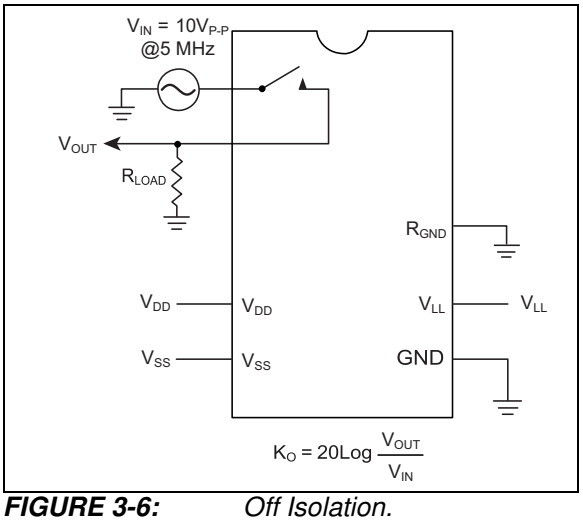


FIGURE 3-6: *Off Isolation.*

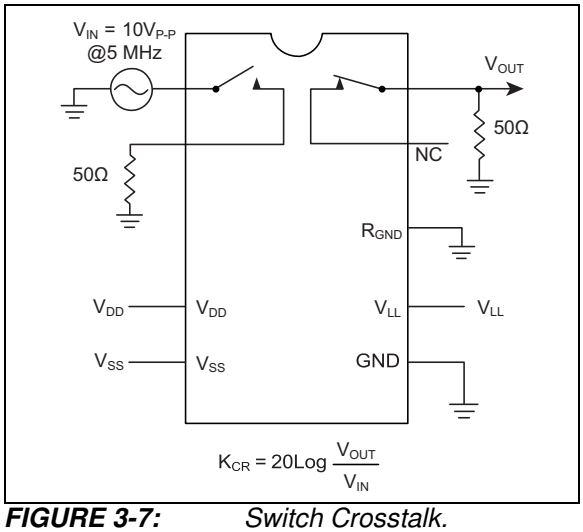


FIGURE 3-7: *Switch Crosstalk.*

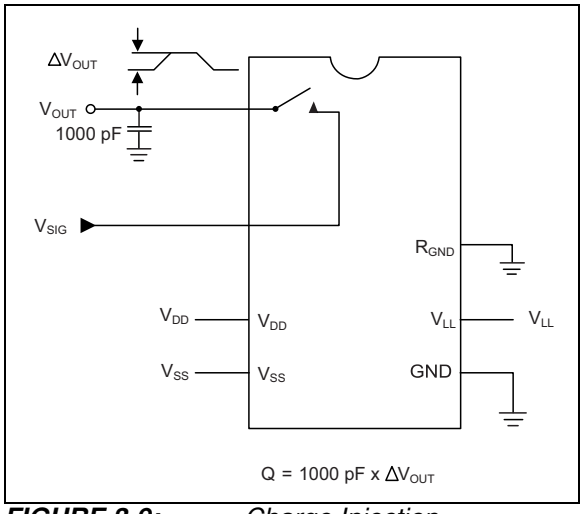


FIGURE 3-9: *Charge Injection.*

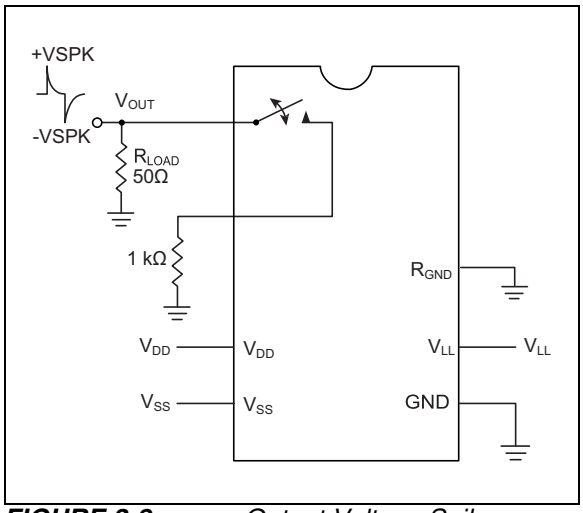


FIGURE 3-8: *Output Voltage Spike.*

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 6.0V, V_{SS} = -6.0V, V_{LL} = 3.3V, T_{AMB} = +25°C.

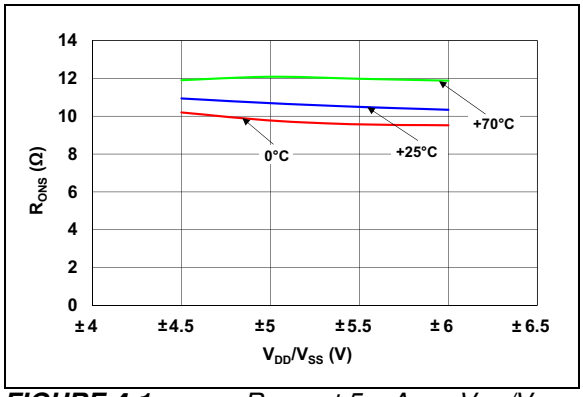


FIGURE 4-1: *R_{ONS} at 5 mA vs. V_{DD}/V_{SS}.*

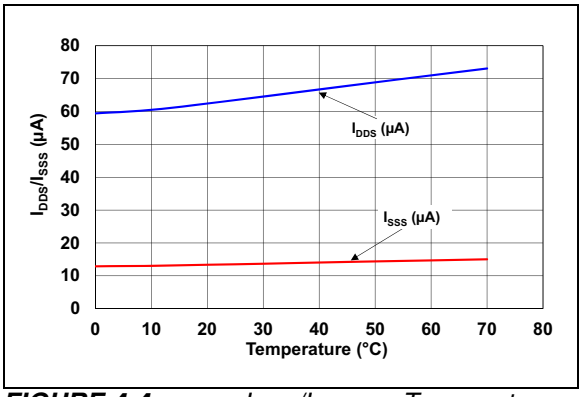


FIGURE 4-4: *I_{DDS}/I_{SSS} vs. Temperature.*

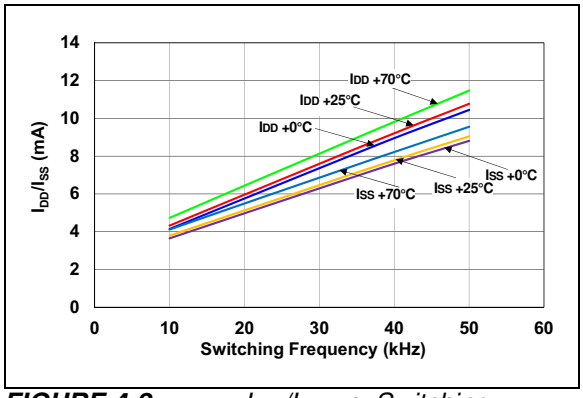


FIGURE 4-2: *I_{DD}/I_{SS} vs. Switching Frequency.*

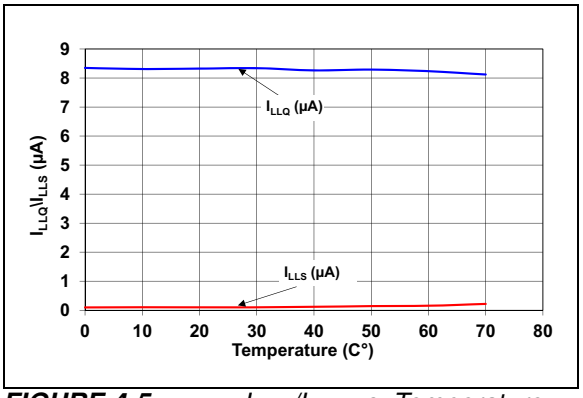


FIGURE 4-5: *I_{LLQ}/I_{LLS} vs. Temperature.*

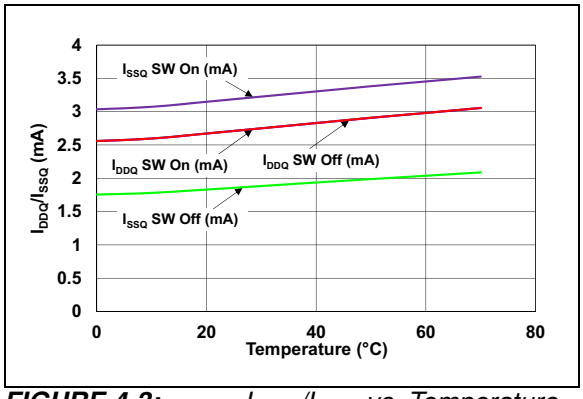


FIGURE 4-3: *I_{DDQ}/I_{SSQ} vs. Temperature.*

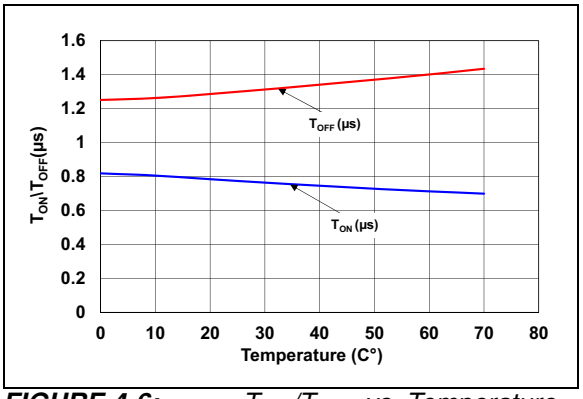


FIGURE 4-6: *T_{ON}/T_{OFF} vs. Temperature.*

Note: Unless otherwise indicated, V_{DD} = 6.0V, V_{SS} = -6.0V, V_{LL} = 3.3V, T_{AMB} = +25°C.

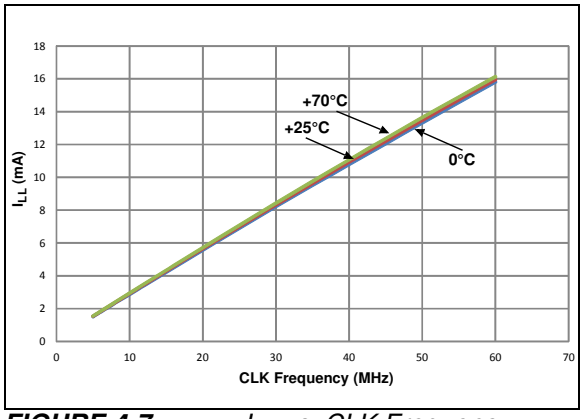


FIGURE 4-7: *I_{LL} vs. CLK Frequency.*

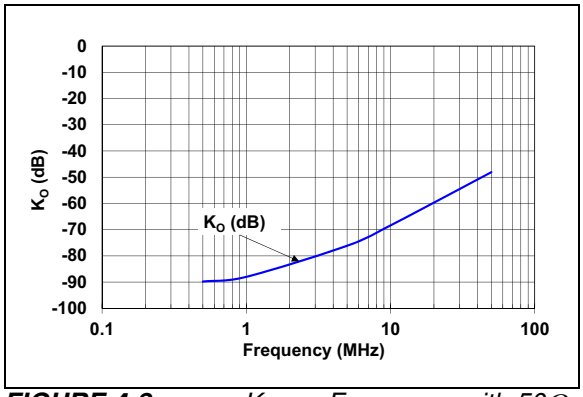


FIGURE 4-8: *K_O vs. Frequency with 50Ω Load.*

5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

The HV2803/HV2903/HV2904 devices are low harmonic distortion, low charge injection, 32-channel, high-voltage analog switches, which do not require high-voltage supplies.

The devices require no high-voltage supplies, only ±6V or ±5V low-voltage supplies. However, all of the analog switches can transmit ±100V high-voltage pulses with typical 10Ω on-resistance and 50 MHz bandwidth for small-signals.

The HV2803/HV2903/HV2904 devices are distinguished by bleed resistors that eliminate voltage build-up in capacitance loads, such as piezoelectric transducers. The devices have two digital logics and controls for two Switch Control modes: Individual Switching mode and Bank Switching mode.

Figure 5-1 shows a typical medical ultrasound imaging system, comprising 64 channels of transmit pulsers, 64 channels of receivers (LNA and ADC) and 64 channels of T/R switches, connecting to 192 elements of an ultrasound probe via a HV2XXX high-voltage analog switch array.

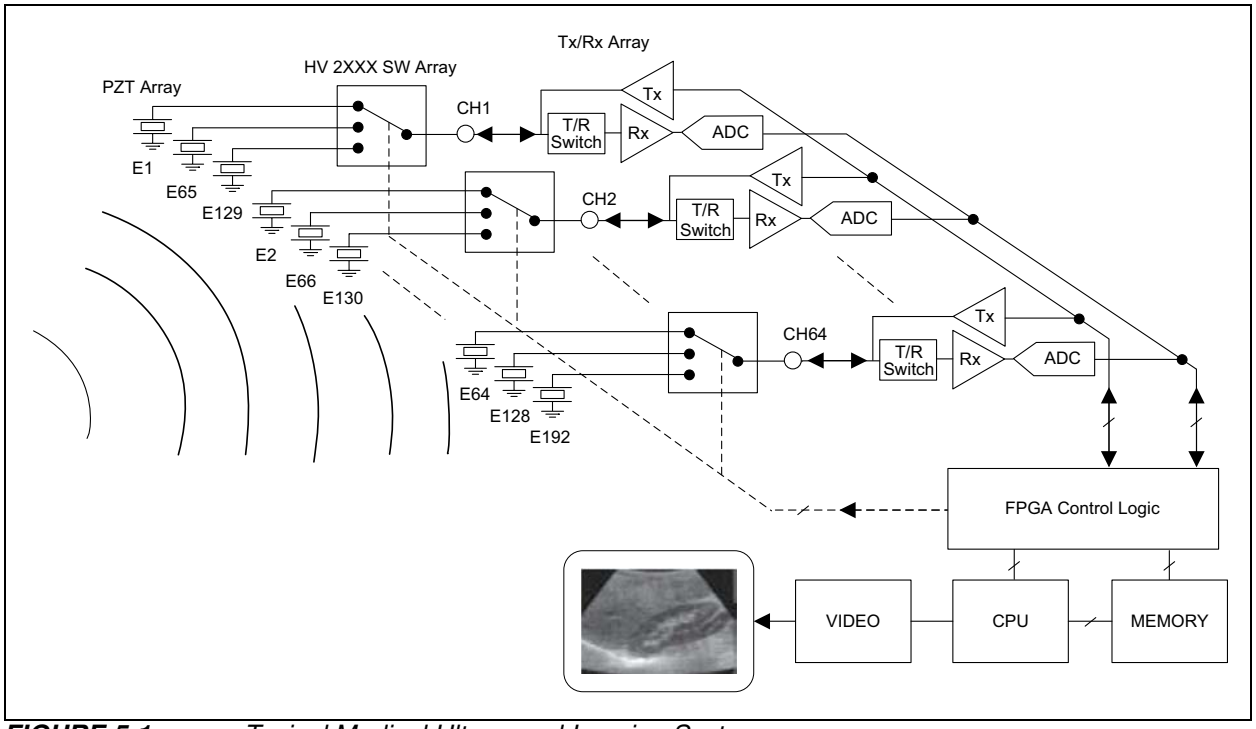


FIGURE 5-1: *Typical Medical Ultrasound Imaging System.*

5.2 Individual Switching Mode and Bank Switching Mode

The HV2803/HV2903/HV2904 devices have two logic circuitries that support two Switching modes determined by the MODE pin logic input. One mode is the Individual Switching mode and the other mode is the Bank Switching mode. When the MODE pin is high, the devices operate in Individual Switching mode and can control 32-channel SPST switches individually through a digital serial interface. When the MODE pin is low, they operate in Bank Switching mode, which works as a 16PDT switch for probe selection. Table 5-1 shows the functional difference of the logic pins in the two modes. When the MODE input is changed from low-to-high, all the shift registers are reset to zero.

TABLE 5-1: LOGIC PINS AT INDIVIDUAL SWITCHING VS. BANK SWITCHING

Pin Name	Individual Switching Mode (MODE = H)		Bank Switching Mode (MODE = L)	
	Function	Description	Function	Description
$\overline{STBY}$	$\overline{STBY}$	L = Standby mode (default) H = Normal operation	$\overline{STBY}$	L = Standby mode (default) H = Normal operation
$D_{IN}/A\overline{B}$	D_{IN}	Data in logic input	$A/\overline{B}$	Logic input to select on bank H = Even SWs on and Odd SWs off L = Even SWs off and Odd SWs on
$\overline{LE}$/EN	$\overline{LE}$	Latch enable logic input	EN	Logic input for enable/disable bank switching H = Enable L = Disable (all SWs off)
CLR	CLR	Latch clear logic input	GND	Should connect to GND
CLK	CLK	Clock logic input for shift register	GND	Should connect to GND
D_{OUT}	D_{OUT}	Data out logic output	high Z	High-Impedance

5.3 Individual Switching Mode Logic Input Timing

When the MODE pin logic input is high, the HV2803/HV2903/HV2904 devices operate in the Individual Switching mode. The HV2803/HV2903/HV2904 devices have a digital serial interface consisting of Data In ($D_{IN}/\overline{AB}$), Clock (CLK), Data Out (D_{OUT}), Latch Enable ($\overline{LE}$/EN) and Clear (CLR) for the Individual Switching mode. The digital circuits are supplied by V_{LL}. The serial clock frequency is up to 66 MHz.

The switch state configuration data is shifted into the shift registers on the rising edge (low-to-high transition) of the clock. The Switch Configuration bit of SW31 is shifted in first and the Configuration bit of SW0 is shifted in last. To change all the switch states at the same time, the Latch Enable Input ($\overline{LE}$/EN) should remain high while the 32-bit Data In signal is shifted into the 32-bit register. After the valid 32-bit data completes shifting into the shift registers, the high-to-low transition of the $\overline{LE}$/EN signal transfers the contents of the shift registers into the latches. Finally, setting the $\overline{LE}$/EN high again, allows all the latches to keep the current state while new data can now be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 32 latches to low. Consequently, all the high-voltage switches are set to an OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR signal. Therefore, when the CLR input is low, the shift register still retains the previous data.

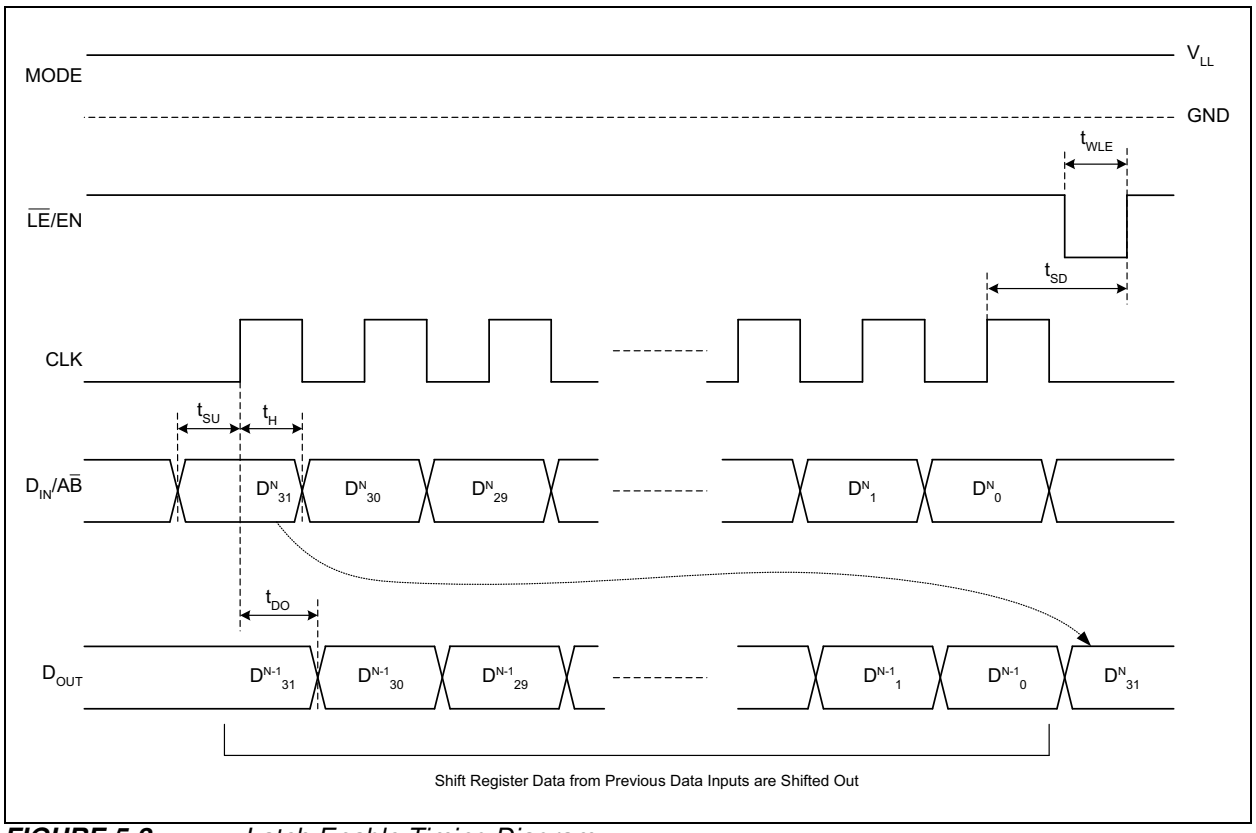


FIGURE 5-2: *Latch Enable Timing Diagram.*

5.4 Multiple Devices Connection in Individual Switching Mode

The serial input interface of the HV2803/HV2903/HV2904 devices allows multiple devices to daisy-chain together. In this configuration, the D_{OUT} pin of a device is connected to the $D_{IN}/\overline{AB}$ pin of the subsequent device, and so forth. The last D_{OUT} pin of the daisy-chained HV2803/HV2903/HV2904 devices can be either floating or fed back to an FPGA (Field Programmable Gate Array) to check the previously stored shift register data.

To control all the high-voltage analog switch states in daisy-chained N devices, N-times 32 clocks and N-times 32 bits of data are shifted into the shift registers, while $\overline{LE}$/EN remains high and CLR remains low. After all the data finishes shifting in, one single negative pulse of the $\overline{LE}$/EN pin transfers the data from all shift registers to all the latches simultaneously. Consequently, all N-times 32 high-voltage analog switches change states simultaneously.

5.5 Bank Switching Mode

When the MODE pin logic input is low, the HV2803/HV2903/HV2904 devices operate in the Bank Switching mode.

The $D_{IN}/\overline{AB}$ pin is used as the A/$\overline{B}$ input and the $\overline{LE}$/EN pin is used as the EN input in the Bank Switching mode. The CLR and CLK logic inputs are not used and are recommended to drive logic low. The D_{OUT} pin is in a high-impedance state. See Table 1-1 for details on Bank Switching mode.

The EN function allows the HV2803/HV2903/HV2904 devices to be configured as either a 2:1 or 4:1 multiplexer/demultiplexer. The HV2803/HV2903/HV2904 devices can replace the relay in a medical ultrasound system. Compared to the mechanical relay, the HV2803/HV2903/HV2904 devices are faster switching, less power consuming and no audible noise emitting switches. Figure 5-3 shows an application example of a 4-probe selection configuration using the HV2803/HV2903/HV2904 Bank Switching mode. Please note that the MODE pin is connected to GND.

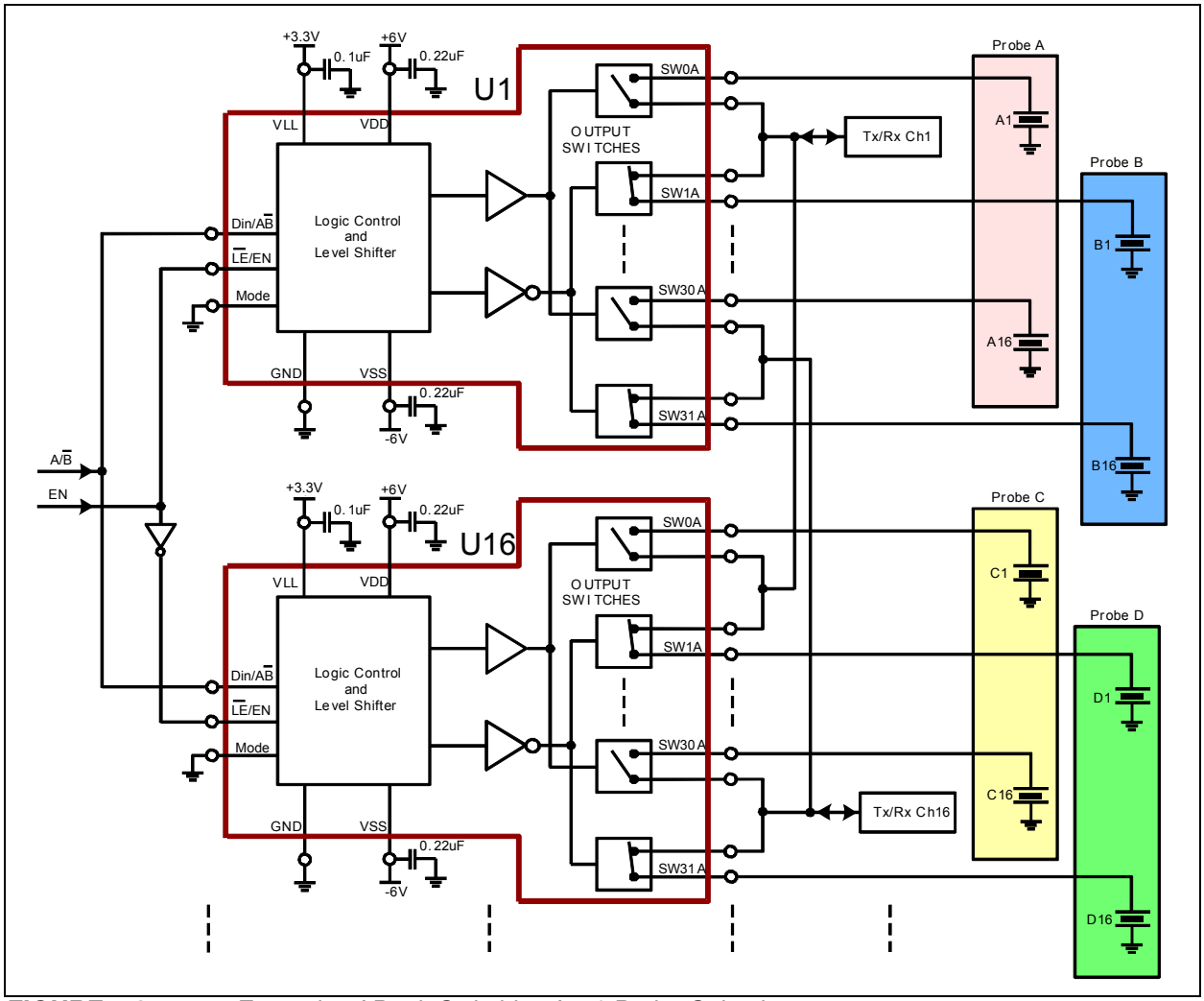
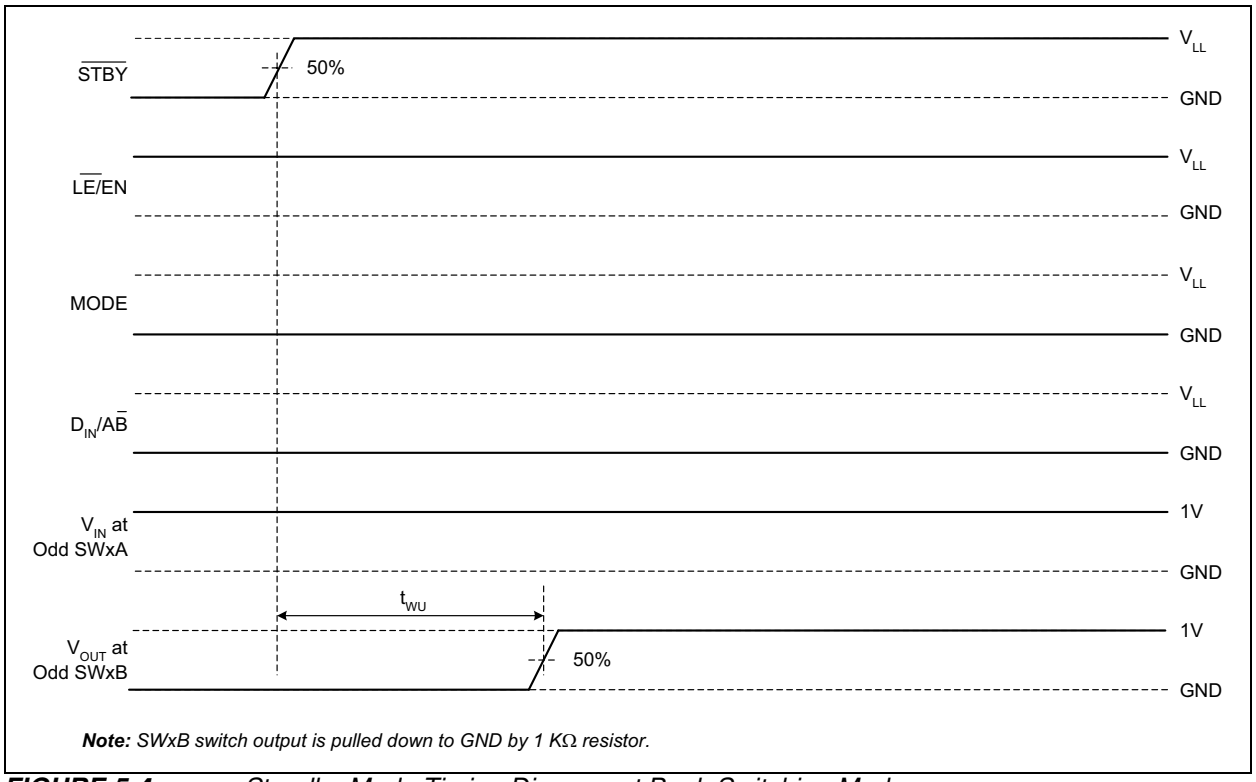


FIGURE 5-3: *Example of Bank Switching for 4-Probe Selection.*

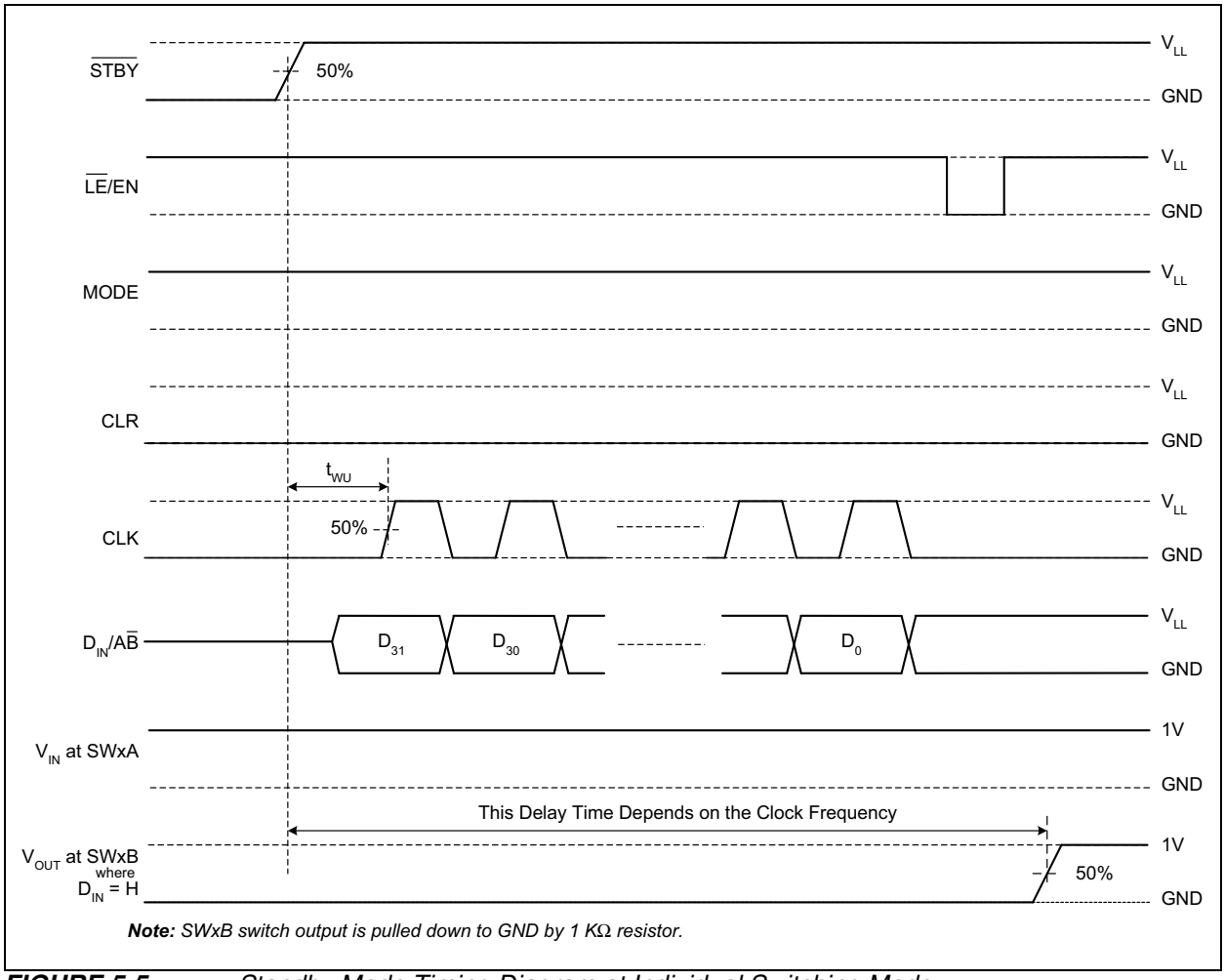
5.6 Standby Mode

To reduce the current consumption during the Idle time, the HV2803/HV2903/HV2904 devices include Standby mode. If the $\overline{STBY}$ logic input is low, the device is in Standby mode to reduce the current consumption by shutting down most of the circuity. If the $\overline{STBY}$ logic input is changed from low to high, the devices are out of Standby mode and the digital logic circuitry starts operating normally after the wake-up time, t_{WU}. Figure 5-4 and Figure 5-5 show the Standby mode timing diagram at Bank Switching mode and Individual Switching mode, respectively. The default logic condition is the standby state. The $\overline{STBY}$ logic input has the highest priority in logic control. See Table 1-1 for details.



Note: *SWxB switch output is pulled down to GND by 1 KΩ resistor.*

FIGURE 5-4: *Standby Mode Timing Diagram at Bank Switching Mode.*



Note: *SWxB switch output is pulled down to GND by 1 KΩ resistor.*

FIGURE 5-5: *Standby Mode Timing Diagram at Individual Switching Mode.*

5.7 Power-up Sequence

The HV2803/HV2903/HV2904 devices have a recommended power-up sequence. It is recommended that V_{SS} and V_{DD} are powered up first, and then V_{LL} is powered up. The power-down sequence is in reverse order of the power-up sequence.

During the power-up/down period, all the analog switch inputs should be within V_{DD} and V_{SS} or floating.

5.8 Layout Considerations

The HV2803/HV2903/HV2904 devices have two separate ground connections. DGND is the ground connection for digital circuitry, and GND is the ground connection for analog switches and substrate. It is important to have a good PCB layout which minimizes noise and ground bounce. It is recommended that two separate ground planes be used in the PCB and those ground planes be connected together at the return terminal of the input power line, as shown in Figure 5-6. It is recommended that 0.1 µF or larger ceramic decoupling capacitors, with low-ESR (Equivalent Series Resistance) and appropriate voltage ratings, be connected between ground and power supplies, as shown in Figure 5-6. The decoupling capacitor of V_{LL} should be connected to DGND, whereas the decoupling capacitors of V_{DD} and V_{SS} should be connected to GND. These decoupling capacitors should be placed as close as possible to the device.

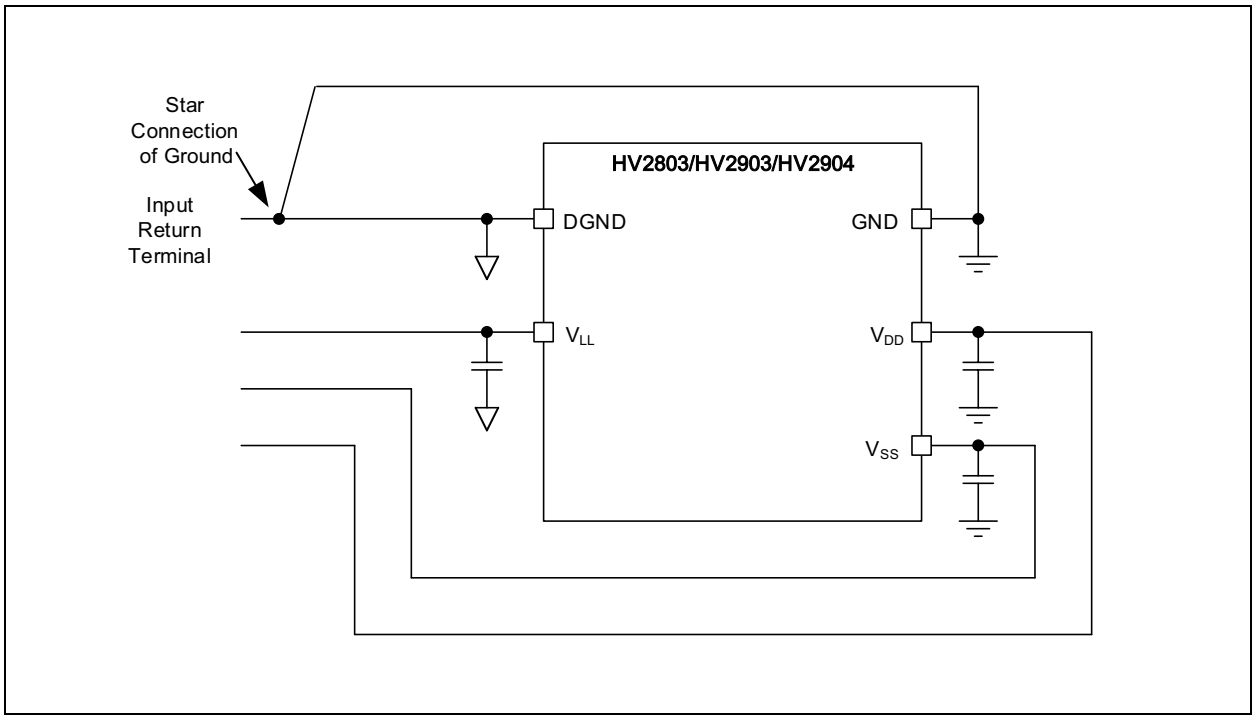
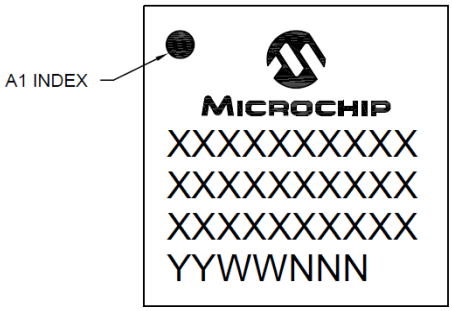


FIGURE 5-6: *Layout Guidelines.*

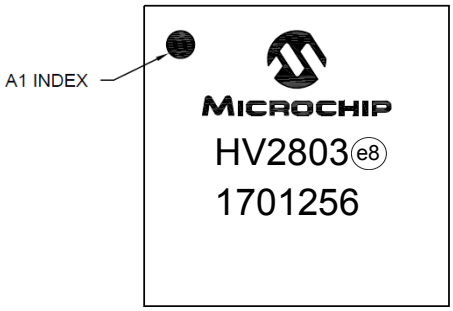
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

132-Ball TFBGA (12x12x1.2 mm)



Example

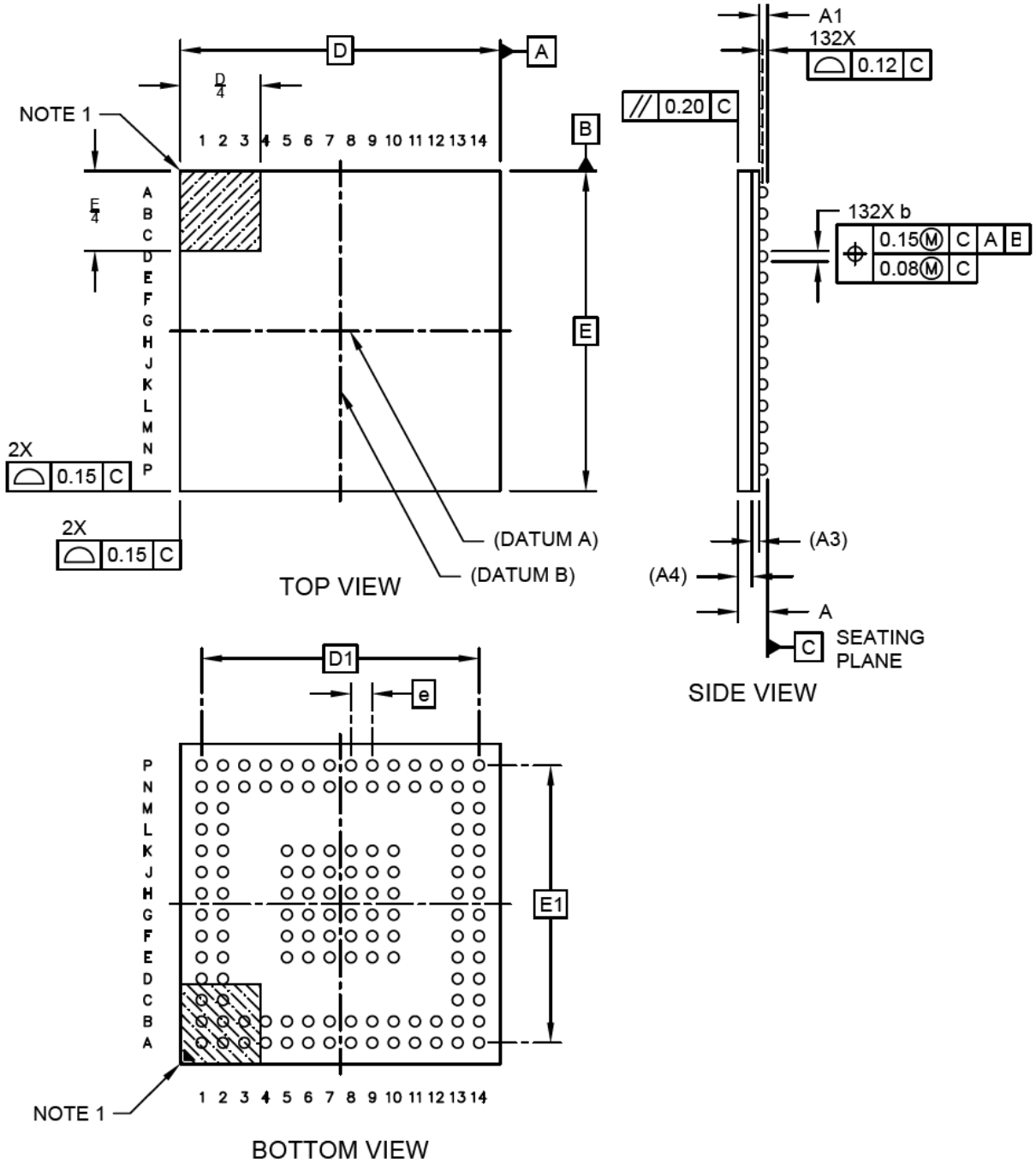


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e8)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e8)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

132-Ball Thin Fine Pitch Ball Grid Array (AHA) - 12x12x1.2mm Body [TFBGA]

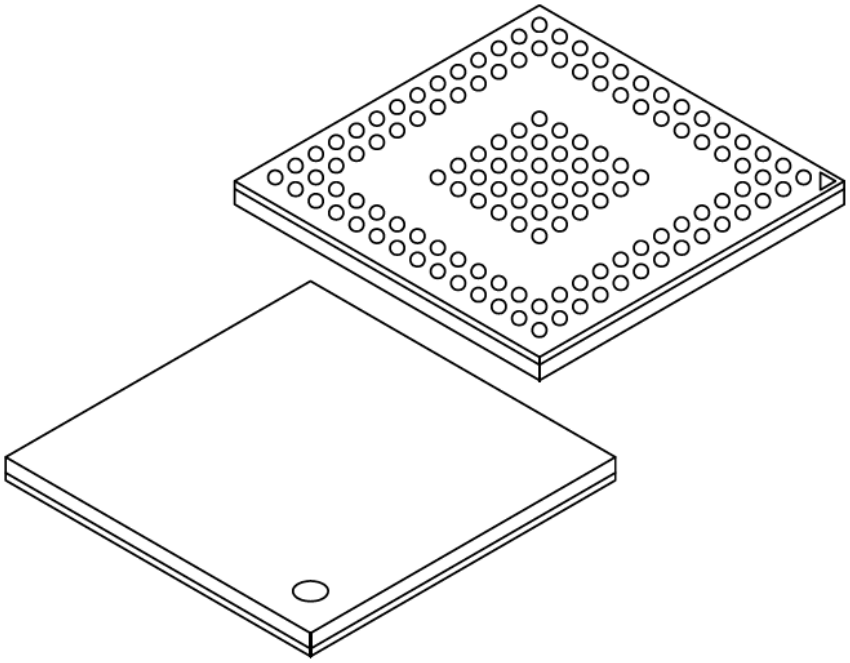
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1193 Rev B Sheet 1 of 2

132-Ball Thin Fine Pitch Ball Grid Array (AHA) - 12x12x1.2mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		132	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.27	0.32	0.37
Substrate Thickness	A2		0.26 REF	
Mold Cap Thickness	A4		0.53 REF	
Overall Length	D		12.00 BSC	
Overall Terminal Centers	D1		10.40 BSC	
Overall Width	E		12.00 BSC	
Overall Terminal Centers	E1		10.40 BSC	
Terminal Diameter	b	0.35	0.40	0.45

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1193 Rev B Sheet 2 of 2