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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

8-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs, POL, Hi-Z, and Short Circuit Detect

Features

- HVCMOS® technology
- Operating output voltage of 250V
- Low power level shifting from 5.0 to 250V
- Shift register speed 8.0MHz @ V_{DD} = 5.0V
- 8 latch data outputs
- Output polarity and blanking
- Output short circuit detect
- Output high-Z control
- CMOS compatible inputs

Applications

- Piezoelectric transducer driver
- Braille driver
- Weaving applications
- Printer drivers
- MEMs
- Displays

General Description

The HV513 is a low voltage serial to high voltage parallel converter with 8 high voltage push-pull outputs. This device has been designed to drive small capacitve loads such as piezoelectric transducers. It can also be used in any application requiring multiple high voltage outputs, with medium current source and sink capabilities.

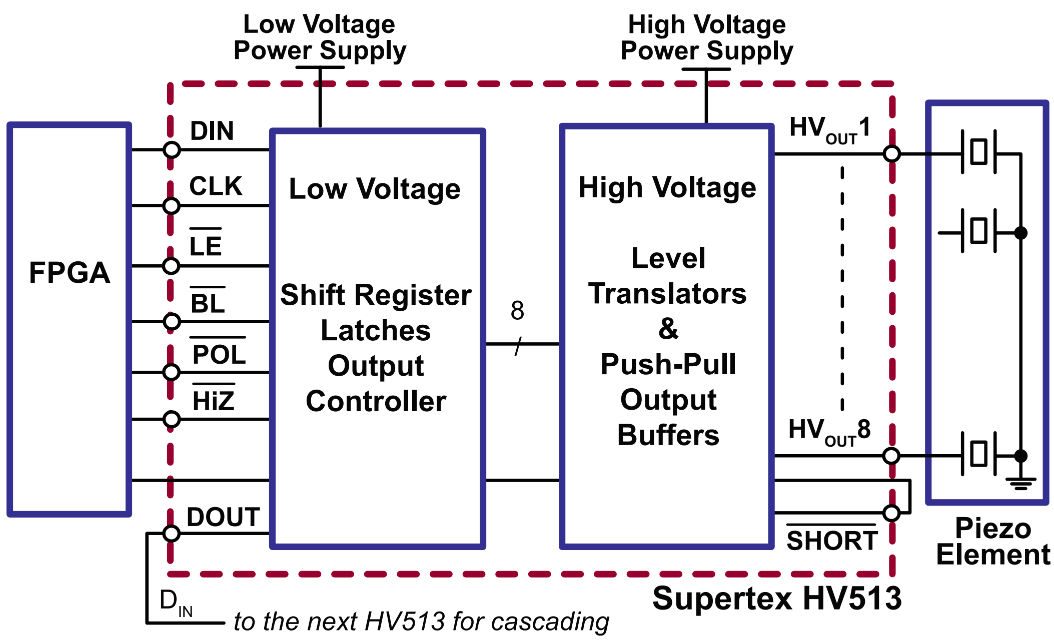
The device consists of an 8-bit shift register, 8 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the low to high transition of the clock. A data output buffer is provided for cascading devices. Operation of the shift register is not affected by the $\overline{\text{LE}}$, $\overline{\text{BL}}$, $\overline{\text{POL}}$, or the $\overline{\text{HI-Z}}$ control inputs. Transfer of data from the shift register to the latch occurs when the $\overline{\text{LE}}$ is high. The data in the latch is stored when $\overline{\text{LE}}$ is low. A high-Z ($\overline{\text{HI-Z}}$) pin is provided to set all the outputs in a high-Z state.

All outputs have short circuit protection that detects if the outputs have reached the required output state. If output does not track the required state, then the $\overline{\text{SHORT}}$ pin will be low. This output will pulse low during the output transistion period under normal operation; see SC Timing Diagram for details.

All outputs will have a break-before-make circuitry to reduce cross-over current during output state changes.

The $\overline{\text{POL}}$, $\overline{\text{BL}}$, $\overline{\text{LE}}$, and $\overline{\text{HI-Z}}$ inputs have an internal pull up resistor.

Typical Application Circuit



Ordering Information

Part Number	Package	Packing
HV513K7-G	32-Lead QFN	400/Tray
HV513K7-G M935	32-Lead QFN	2000/Reel
HV513WG-G	24-Lead SOW	1000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
Logic supply, V_{DD}	-0.5V to 6.0V
High voltage supply, V_{PP}	V_{DD} to 275V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[1]	0.3A
High voltage supply current[1]	0.25A
Continuous total power dissipation[2]	750mW
Operating junction temperature	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

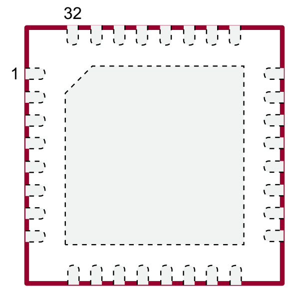
Notes:

1. *Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to 85°C at 12mW/°C.*

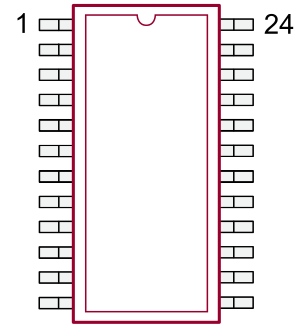
Typical Thermal Resistance

Package	θ_{ja}
32-Lead QFN	22°C/W
24-Lead SOW	44°C/W

Pin Configuration



32-Lead QFN
(top view)



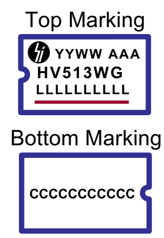
24-Lead SOW
(top view)

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
= “Green” Packaging

Package may or may not include the following marks: Si or

32-Lead QFN



YY = Year Sealed
WW = Week Sealed
A = Assembler ID
L = Lot Number
C = Country of Origin*
= “Green” Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

24-Lead SOW

Typical Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V	---
V_{PP}	High voltage supply	50	-	250	V	Note 1
V_{IH}	High-level input voltage	V_{DD}-0.9	-	V_{DD}	V	---
V_{IL}	Low-level input voltage	0	-	0.9	V	---
T_J	Operating junction temperature	-40	-	+85	°C	---

Notes:

1. *Below minimum V_{PP} the output may not switch.*
2. ***Power-up sequence should be the following:***
    1. *Connect ground*
    2. *Apply V_{DD}*
    3. *Set all inputs (Data, CLK, Enable, etc.) to a known state*
    4. *Apply V_{PP}*

Power-down sequence should be the reverse of the above

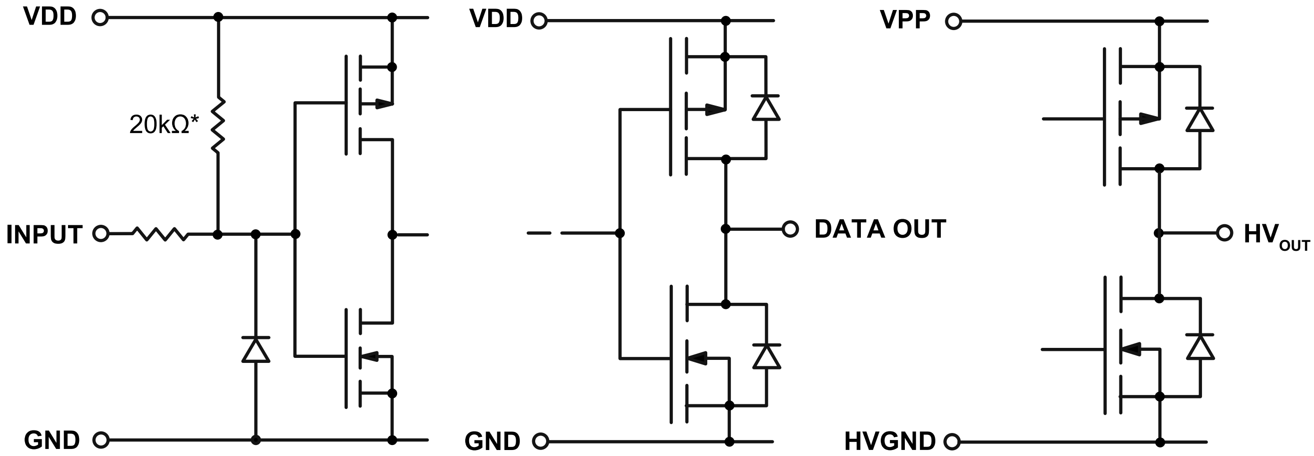
DC Electrical Characteristics *(Over typical operating conditions unless otherwise specified, $T_J = 25^oC$)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	-	4.0	mA	f_{CLK} = 8.0Hz, $\overline{\text{LE}}$ = Low
I_{DDQ}	Quiescent V_{DD} supply current		-	-	0.1	mA	All $V_{IN} = V_{DD}$
			-	-	2.0		All V_{IN} = 0V
I_{PP}	V_{PP} supply current		-	-	100	µA	V_{PP} = 250V, f_{OUT} = 300Hz, no load
I_{PPQ}	Quiescent V_{PP} supply current		-	-	100	µA	V_{PP} = 240V, outputs are static
I_{IH}	High-level logic input current		-	-	10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-		-10	µA	V_{IL} = 0V
			-	-	-350		V_{IL} = 0V, for inputs w/pull-up resistors
V_{OH}	High level output	HV_{OUT}	140	-	-	V	V_{PP} = 200V, I_{HVOUT} = -20mA
		Data out	V_{DD} -1.0V	-	-		I_{DOUT} = -0.1mA
V_{OL}	Low level output	HV_{OUT}	-	-	60	V	V_{DD} = 4.5V, I_{HVOUT} = 20mA
		Data out	-	-	1.0		I_{DOUT} = 0.1mA

AC Electrical Characteristics *(Over typical operating conditions unless otherwise specified, $T_J = 25^oC$)*

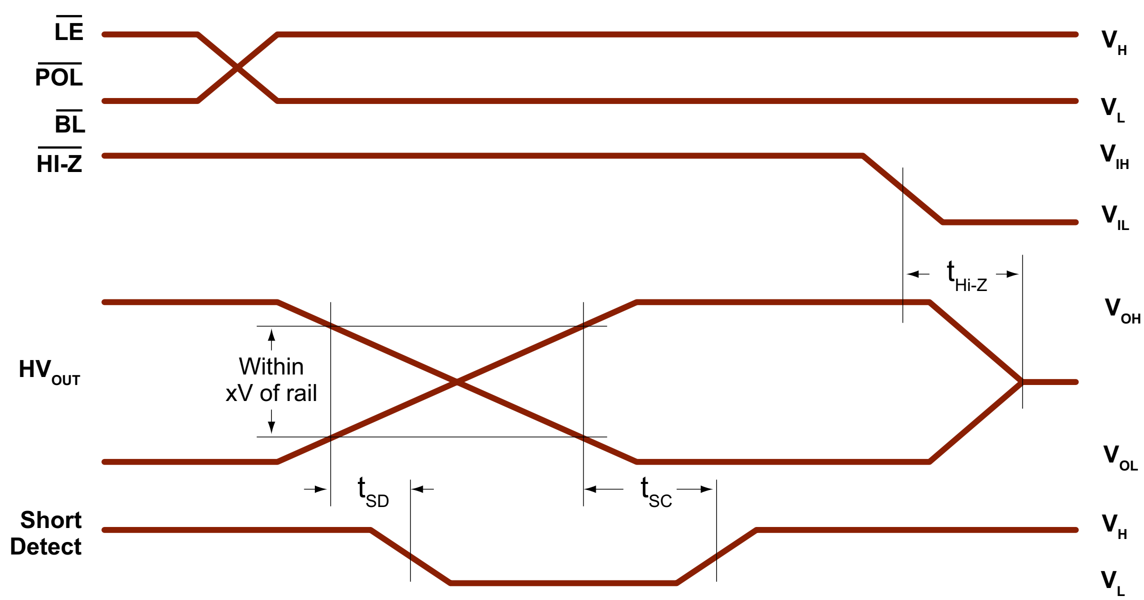
Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency	0	-	8.0	MHz	---
f_{OUT}	Output switching frequency (SOA limited)	-	300	-	Hz	C_L = 50nF, V_{PP} = 200V
t_W	Clock width high and low	62	-	-	ns	---
t_{SU}	Data setup time before clock rises	15	-	-	ns	---
t_H	Data hold time after clock rises	30	-	-	ns	---
t_{WLE}	Width of latch enable pulse	80	-	-	ns	---
t_{DLE}	$\overline{\text{LE}}$ delay time after rising edge of clock	35	-	-	ns	---
t_{SLE}	$\overline{\text{LE}}$ setup time before rising edge of clock	40	-	-	ns	---
t_{OR}, t_{OF}	HV_{OUT} rise/fall time	-	-	1000	µs	C_L = 100nF, V_{PP} = 200V
$t_{d\ ON/OFF}$	Delay time for output to start rise/fall	-	-	500	ns	---
t_{DHL}	Delay time clock to D_{OUT} high to low	-	-	110	ns	C_L = 15pF
t_{DLH}	Delay time clock to D_{OUT} low to high	-	-	110	ns	C_L = 15pF
t_R, t_F	All logic inputs	-	-	5.0	ns	---
t_{SD}	Output short circuit detection	-	-	500	ns	C_L = 15pF, Short to output fall of $\overline{\text{SHORT}}$
t_{SC}	Output short circuit clear	-	-	3000	ns	Short clear to output rise of $\overline{\text{SHORT}}$
t_{HI-Z}	Output $\overline{\text{HI-Z}}$ state	-	-	500	ns	---

Input and Output Equivalent Circuits



Logic Inputs **Logic Data Output** **High Voltage Outputs**

Short Circuit Detect Detail Timing



Note:

For V_{PP} greater than 150V:

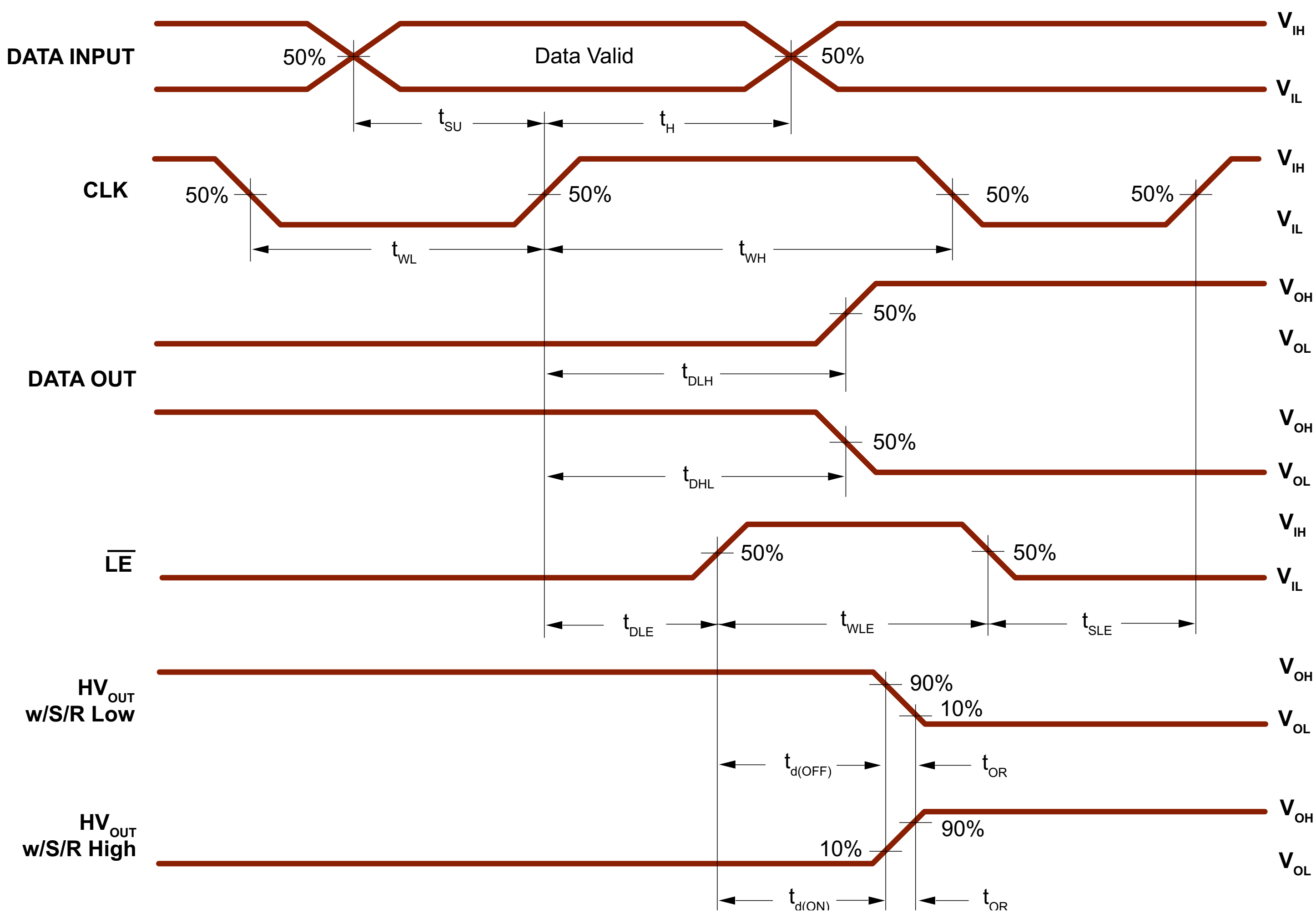
Short detect output will flag short conditions

- *HV_{OUT} is higher than 10V when expected low*
- *HV_{OUT} is lower than V_{PP} - 100V when expected high*

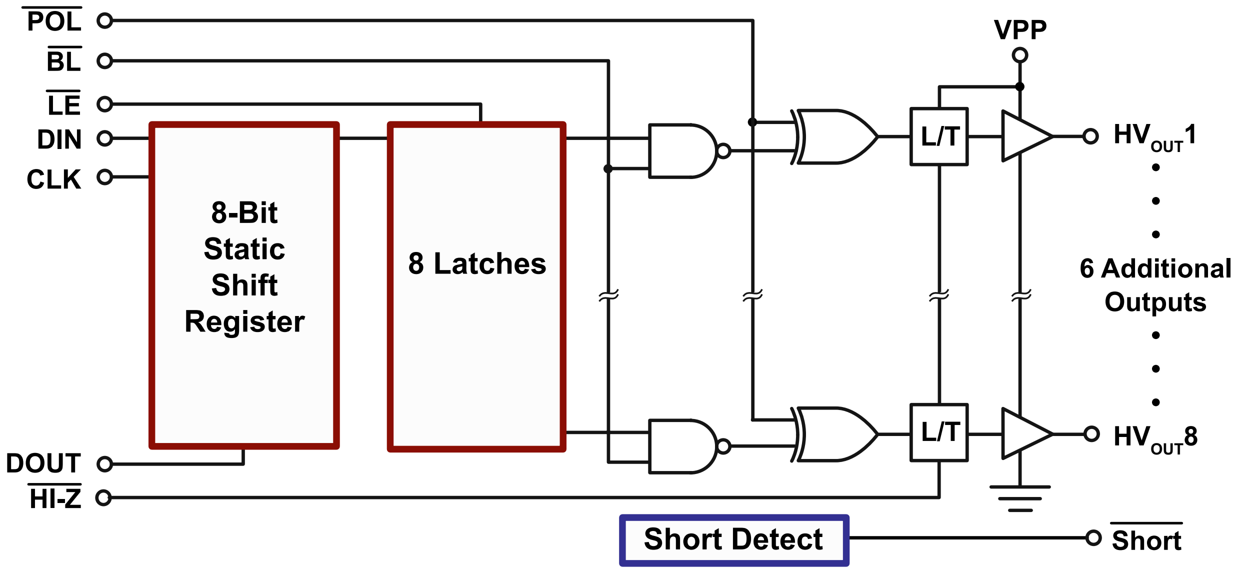
Short detect output will stay clear

- *HV_{OUT} is lower than 2.0V when expected low*
- *HV_{OUT} is higher than V_{PP} - 60V when expected high*

Switching Waveforms



Functional Block Diagram



Note:
$\overline{POL}$, $\overline{BL}$, $\overline{LE}$, and $\overline{Hi\text{-}Z}$ have internal 20kΩ pull-up resistors.

Function Table

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	POL	HI-Z	Shift Reg 1 2...8	HV Outputs 1 2...8	Data Out •
All on	X	X	X	L	L	H	• •...•	H H...H	•
All off	X	X	X	L	H	H	• •...•	L L...L	•
Invert mode	X	X	L	H	L	H	• •...•	• •...• (b)	•
Load S/R	H OR L	↑	L	H	H	H	H or L •...•	• •...•	•
Store data in latches	X	X	L	H	H	H	• •...•	• •...•	•
	X	X	L	H	L	H	• •...•	• •...• (b)	•
Transparent mode	L	↑	H	H	H	H	L •...•	L •...•	•
	H	↑	H	H	H	H	H •...•	H •...•	•
Outputs High-Z	X	X	X	X	X	L	• •...•	High impedence outputs	•
Outputs on	X	X	X	X	X	H	• •...•	• •...•	•

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition
• = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

Pin Description - 32-Lead QFN

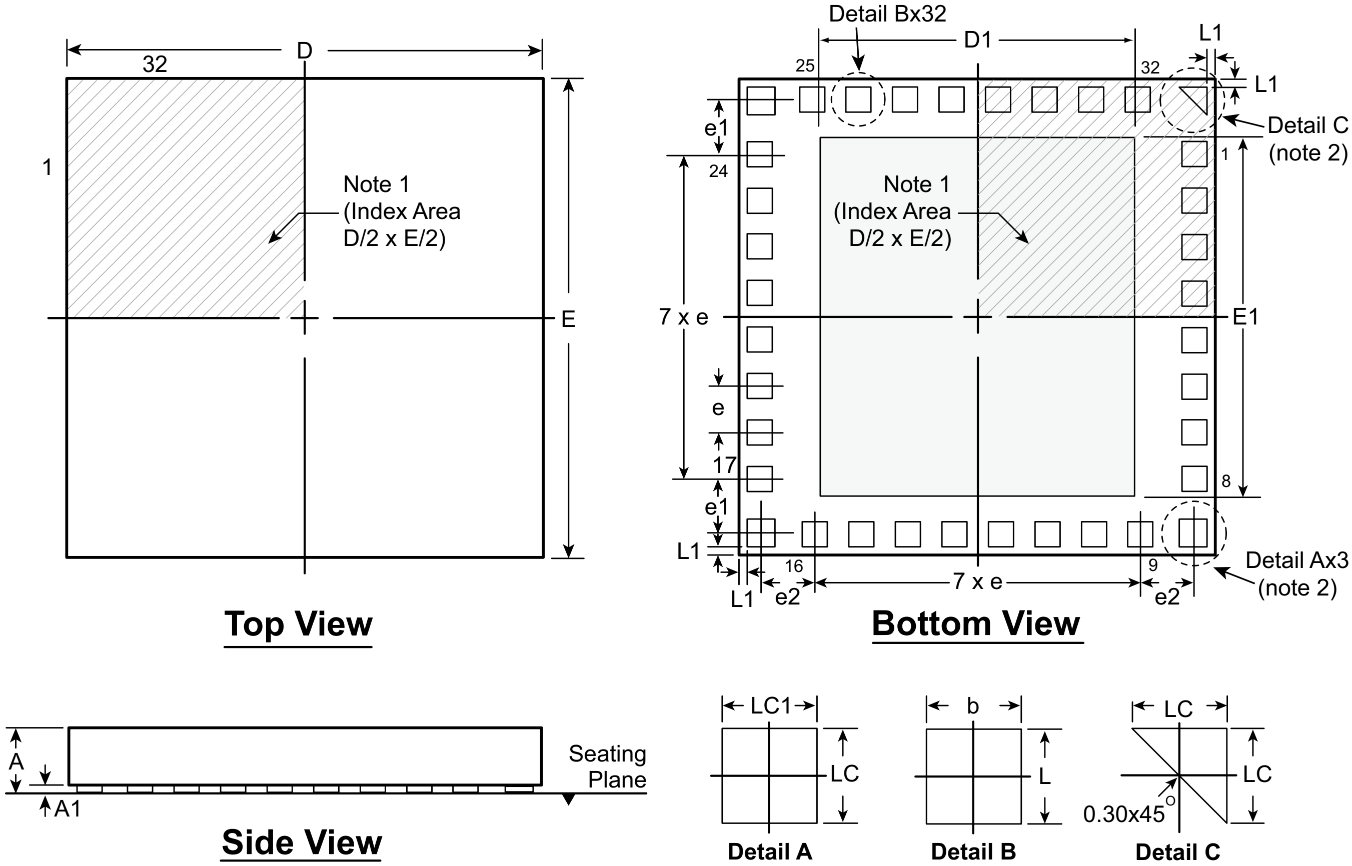
Pin #	Function	Description
1	NC	No internal connection
2		
3		
4	LGND	Low voltage ground
5	HVGND	High voltage ground
6		
7	NC	No internal connection
8		
9	$HV_{OUT}1$	High voltage push-pull output
10	$HV_{OUT}2$	High voltage push-pull output
11	$HV_{OUT}3$	High voltage push-pull output
12	$HV_{OUT}4$	High voltage push-pull output
13	$HV_{OUT}5$	High voltage push-pull output
14	$HV_{OUT}6$	High voltage push-pull output
15	$HV_{OUT}7$	High voltage push-pull output
16	$HV_{OUT}8$	High voltage push-pull output
17	NC	No internal connection
18		
19	VPP	High voltage supply
20		
21	VDD	Logic supply voltage
22	DOUT	Data output
23	NC	No internal connection
24		
25	$\overline{BL}$	Blanking pin, logic input low sets all HV_{OUTS} low
26	NC	No internal connection
27	$\overline{POL}$	Polarity bar input logic
28	CLK	Clock pin, shift registers shifts data on rising edge of input clock
29	$\overline{LE}$	Latch enable bar input logic
30	$\overline{SHORT}$	If output does not reach its required state, SHORT pin will output logic low
31	$\overline{HI\text{-}Z}$	High impedance pin, logic input low sets all outputs in a high impedance state
32	DIN	Data input
Center Pad	VPP	Center pad is at V_{PP} potential. Connect to VPP or leave floating.

Pin Description - 24-Lead SOW

Pin #	Function	Description
1	NC	No internal connection
2	VDD	Logic supply voltage
3	DOUT	Data output
4	$\overline{\text{BL}}$	Blanking pin, logic input LOW sets all HV_{OUTS} low
5	$\overline{\text{POL}}$	Polarity bar input logic
6	CLK	Clock pin, shift registers shifts data on rising edge of input clock
7	$\overline{\text{LE}}$	Latch enable bar input logic
8	$\overline{\text{SHORT}}$	If output does not reach its required state, SHORT pin will output logic LOW
9	HI-Z	High impedance pin, logic input LOW sets all outputs in a high impedance state
10	$\overline{\text{DIN}}$	Data input
11	LGND	Low voltage ground
12	NC	No internal connection
13	HVGND	High voltage ground
14		
15	$HV_{OUT}1$	High voltage push-pull output
16	$HV_{OUT}2$	High voltage push-pull output
17	$HV_{OUT}3$	High voltage push-pull output
18	$HV_{OUT}4$	High voltage push-pull output
19	$HV_{OUT}5$	High voltage push-pull output
20	$HV_{OUT}6$	High voltage push-pull output
21	$HV_{OUT}7$	High voltage push-pull output
22	$HV_{OUT}8$	High voltage push-pull output
23	VPP	High voltage supply
24		

32-Lead QFN Package Outline (K7)

6.00x6.00mm body, 0.80mm height (max), 0.50mm pitch



Notes:

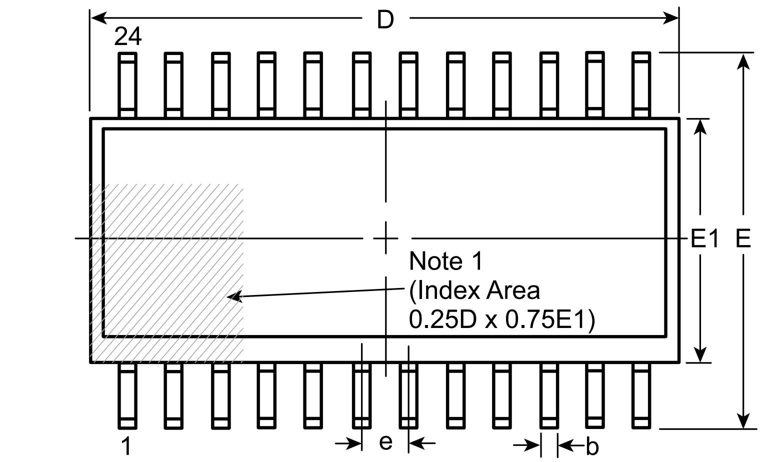
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *The 4 corner pads are for mechanical placement only, they are not internally connected.*

Symbol		A	A1	b	D	D1	E	E1	e	e1	e2	L	L1	LC	LC1
Dimension (mm)	MIN	0.70	0.00	0.20	5.90	3.20	5.90	4.30	0.50 BSC	1.00 REF	0.975 REF	0.20	0.10 REF	0.20	0.25
	NOM	0.75	-	0.30	6.00	3.30	6.00	4.40				0.30		0.30	0.35
	MAX	0.80	0.05	0.40	6.10	3.40	6.10	4.50				0.40		0.40	0.45

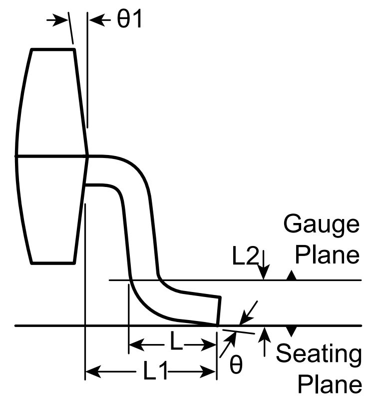
Drawings not to scale.
***Supertex Doc. #:** DSPD-32QFNK76X6P050, Version B092309.*

24-Lead SOW (Wide Body) Package Outline (WG)

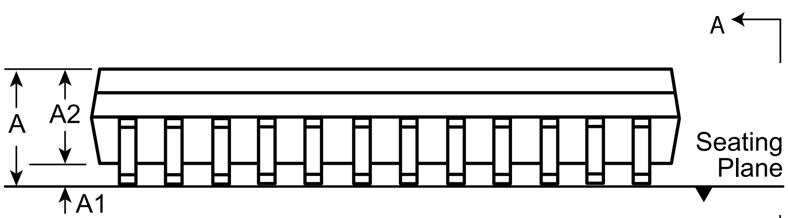
15.40x7.50 body, 2.65mm height (max), 1.27mm pitch



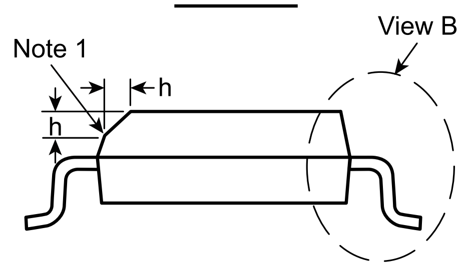
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	15.20*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	15.40	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	15.60*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AD, Issue E, Sep. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-24SOWWG, Version E041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com