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HV5122 / HV5222

32-Channel, Serial-to-Parallel Converter with Open-Drain Outputs

Features

- Processed with High Voltage CMOS technology
- Output voltages to 225V using a ramped supply voltage
- SINK current minimum 100mA
- Shift register speed 8.0MHz
- Strobe and enable inputs
- CMOS compatible inputs
- Forward and reverse shifting options

Description

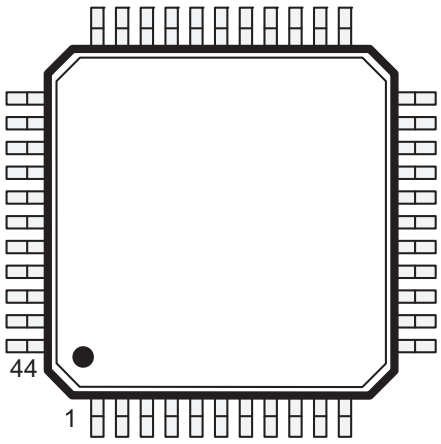
HV5122 / HV5222 are low-voltage serial to high-voltage parallel converters with open-drain outputs. These devices are primarily designed for use as a driver for AC electroluminescent displays. HV5122 / HV5222 can also be used in any application requiring multiple high-voltage, current-sinking output capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and all-on functions. Data is shifted through the shift register on the high-to-low transition of the clock. HV5122 shifts in the counter-clockwise direction when viewed from the top of the package and HV5222 shifts in the clockwise direction.

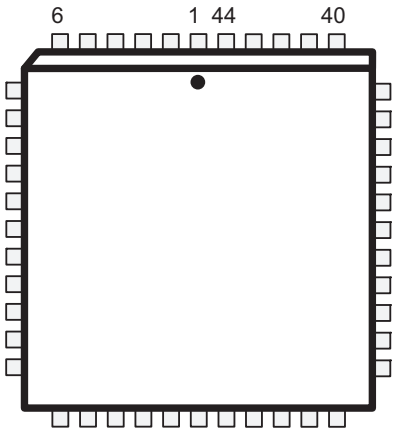
For cascading devices, HV5122 / HV5222 provides a data output buffer that reflects he current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

HV5122 / HV5222 are designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.

Package Type



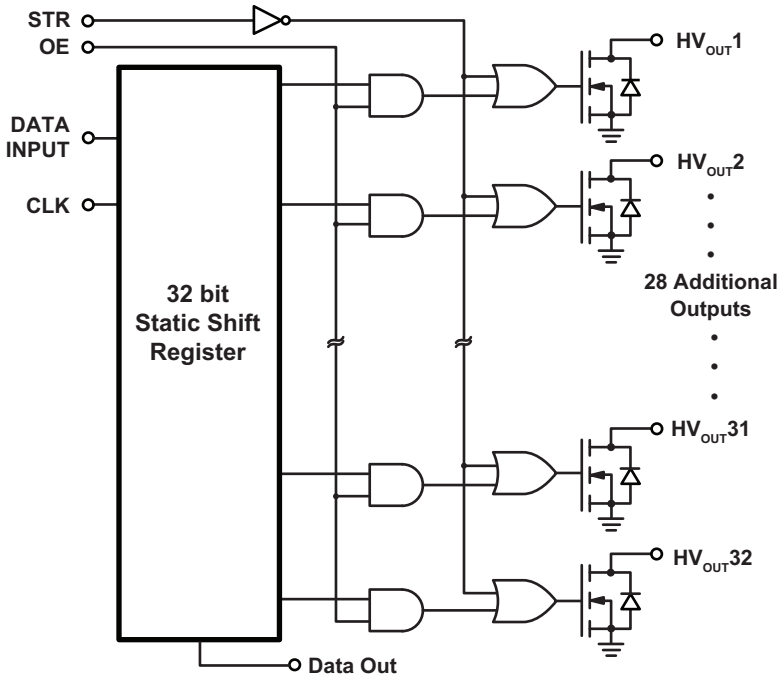
44-Lead PQFP



44-Lead PLCC

See Table 2-1 for pin information

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Supply voltage, V_{DD} ..... -0.5V to +15V
Supply voltage, V_{PP} ..... -0.5V to +250V
Logic input levels ..... -0.5V to V_{DD}+0.5V
Ground current[1] 1.5A
Continuous total power dissipation[2] 1200mW
Operating temperature range ..... -40°C to +85°C
Storage temperature range ..... -65°C to +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1: Duty cycle is limited by the total power dissipated in the package.
2: For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended conditions unless otherwise specified						
Symbol	**Parameter**		**Min**	**Max**	**Units**	**Conditions**
DC Characteristics						
I_{DD}	V_{DD} supply current		-	15	mA	f_{CLK}= 8.0MHz, f_{DATA}= 4.0MHz
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	D_{IN}= 0V, all input logic pins = 0V, all outputs off
$I_{O(OFF)}$	Off-state output current		-	10	µA	All outputs high, all switches parallel
I_{IH}	High level logic input current		-	1.0	µA	V_{IN}= V_{DD}
I_{IL}	Low level logic input current		-	-1.0	µA	V_{IL}= 0
V_{OH}	High level output data out		V_{DD} - 1.0V	-	V	I_{DOUT}= -100µA
V_{OL}	Low level output voltage	HV_{OUT}	-	15	V	I_{HVOUT}= +100mA
		Data out	-	1.0		I_{DOUT}= +100µA
V_{OC}	HV_{OUT} clamp voltage		-	-1.5	V	I_{OL}= -100mA
AC Characteristics (V_{DD} = 12V, T_A=25°C)						
f_{CLK}	Clock frequency		-	8.0	MHz	
t_W	Clock width, high or low		62	-	ns	
t_{SU}	Data setup time before CLK falls		25	-	ns	
t_H	Data hold time after CLK falls		10	-	ns	
t_{ON}	Turn-on time, HV_{OUT} from strobe		-	500	ns	R_L= 2.0kΩ to 200V
t_{DHL}	Data output delay after H to L CLK		-	100	ns	C_L= 15pF
t_{DLH}	Data output delay after L to H CLK		-	100	ns	C_L= 15pF

TABLE 1-2: TYPICAL THERMAL RESISTANCE

Package	**θ_{ja}**
44-Lead PQFP	51°C/W
44-Lead PLCC	37°C/W

2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Type.

TABLE 2-1: PIN DESCRIPTION PQFP

Pin #	HV5122	HV5222	Description
1	$HV_{OUT}11$	$HV_{OUT}22$	High voltage outputs.
2	$HV_{OUT}12$	$HV_{OUT}21$	
3	$HV_{OUT}13$	$HV_{OUT}20$	
4	$HV_{OUT}14$	$HV_{OUT}19$	
5	$HV_{OUT}15$	$HV_{OUT}18$	
6	$HV_{OUT}16$	$HV_{OUT}17$	
7	$HV_{OUT}17$	$HV_{OUT}16$	
8	$HV_{OUT}18$	$HV_{OUT}15$	
9	$HV_{OUT}19$	$HV_{OUT}14$	
10	$HV_{OUT}20$	$HV_{OUT}13$	
11	$HV_{OUT}21$	$HV_{OUT}12$	
12	$HV_{OUT}22$	$HV_{OUT}11$	
13	$HV_{OUT}23$	$HV_{OUT}10$	
14	$HV_{OUT}24$	$HV_{OUT}9$	
15	$HV_{OUT}25$	$HV_{OUT}8$	
16	$HV_{OUT}26$	$HV_{OUT}7$	
17	$HV_{OUT}27$	$HV_{OUT}6$	
18	$HV_{OUT}28$	$HV_{OUT}5$	
19	$HV_{OUT}29$	$HV_{OUT}4$	
20	$HV_{OUT}30$	$HV_{OUT}3$	
21	$HV_{OUT}31$	$HV_{OUT}2$	
22	$HV_{OUT}32$	$HV_{OUT}1$	
23	DATA OUT	DATA OUT	Data output for cascading to the data input of the next device.
24	N/C	N/C	No connect.
25			
26			
27			
28	OE	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
29	CLK	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.
30	GND	GND	Logic and high voltage ground.
31	VDD	VDD	Low voltage logic power rail.
32	STR	STR	Strobe.
33	DATA IN	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.
34	N/C	N/C	No connect.

TABLE 2-1: PIN DESCRIPTION PQFP (CONTINUED)

Pin #	HV5122	HV5222	Description
35	$HV_{OUT}1$	$HV_{OUT}32$	High voltage outputs.
36	$HV_{OUT}2$	$HV_{OUT}31$	
37	$HV_{OUT}3$	$HV_{OUT}30$	
38	$HV_{OUT}4$	$HV_{OUT}29$	
39	$HV_{OUT}5$	$HV_{OUT}28$	
40	$HV_{OUT}6$	$HV_{OUT}27$	
41	$HV_{OUT}7$	$HV_{OUT}26$	
42	$HV_{OUT}8$	$HV_{OUT}25$	
43	$HV_{OUT}9$	$HV_{OUT}24$	
44	$HV_{OUT}10$	$HV_{OUT}23$	

TABLE 2-2: PIN DESCRIPTION PLCC

Pin #	HV5122	HV5222	Description
1	$HV_{OUT}16$	$HV_{OUT}17$	High voltage outputs
2	$HV_{OUT}17$	$HV_{OUT}16$	
3	$HV_{OUT}18$	$HV_{OUT}15$	
4	$HV_{OUT}19$	$HV_{OUT}14$	
5	$HV_{OUT}20$	$HV_{OUT}13$	
6	$HV_{OUT}21$	$HV_{OUT}12$	
7	$HV_{OUT}22$	$HV_{OUT}11$	
8	$HV_{OUT}23$	$HV_{OUT}10$	
9	$HV_{OUT}24$	$HV_{OUT}9$	
10	$HV_{OUT}25$	$HV_{OUT}8$	
11	$HV_{OUT}26$	$HV_{OUT}7$	
12	$HV_{OUT}27$	$HV_{OUT}6$	
13	$HV_{OUT}28$	$HV_{OUT}5$	
14	$HV_{OUT}29$	$HV_{OUT}4$	
15	$HV_{OUT}30$	$HV_{OUT}3$	
16	$HV_{OUT}31$	$HV_{OUT}2$	
17	$HV_{OUT}32$	$HV_{OUT}1$	
18	DATA OUT	DATA OUT	Data output for cascading to the data input of the next device.
19	N/C	N/C	No connect.
20			
21			
22			
23	OE	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
24	CLK	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.
25	GND	GND	Logic and high voltage ground.
26	VDD	VDD	Low voltage logic power rail.
27	STR	STR	Strobe.

TABLE 2-2: PIN DESCRIPTION PLCC (CONTINUED)

Pin #	HV5122	HV5222	Description
28	DATA IN	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.
29	N/C	N/C	No connect.
30	$HV_{OUT}1$	$HV_{OUT}32$	High voltage outputs.
31	$HV_{OUT}2$	$HV_{OUT}31$	
32	$HV_{OUT}3$	$HV_{OUT}30$	
33	$HV_{OUT}4$	$HV_{OUT}29$	
34	$HV_{OUT}5$	$HV_{OUT}28$	
35	$HV_{OUT}6$	$HV_{OUT}27$	
36	$HV_{OUT}7$	$HV_{OUT}26$	
37	$HV_{OUT}8$	$HV_{OUT}25$	
38	$HV_{OUT}9$	$HV_{OUT}24$	
39	$HV_{OUT}10$	$HV_{OUT}23$	
40	$HV_{OUT}11$	$HV_{OUT}22$	
41	$HV_{OUT}12$	$HV_{OUT}21$	
42	$HV_{OUT}13$	$HV_{OUT}20$	
43	$HV_{OUT}14$	$HV_{OUT}19$	
44	$HV_{OUT}15$	$HV_{OUT}18$	

3.0 FUNCTIONAL DESCRIPTION

Table 3-1 provides functional information about HV5122 / HV5222.

TABLE 3-1: FUNCTIONAL TABLE

Function	Inputs				Outputs				
	Data In	CLK	OE	STR	Shift Reg		HV Outputs		Data Out
					1	2...32	1	2...32	
All on	X	X	X	L	●	●...●	ON	ON...ON	●
All off	X	X	L	H	●	●...●	OFF	OFF...OFF	●
Load S/R	H/L	↓	L	H	H/L	Q1...Q31	OFF	OFF...OFF	Q32
Output Enable	X	H/L	H	H	H/L	●...●	ON/OFF	●...●	●

Note 1: H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

2: ●= dependent on previous stage's state before the last CLK high-to-low transition

3.1 Power-Up and Recommended Operating Conditions

To power-up HV5122 / HV5222, perform the following power-up sequence:

1. Connect ground
2. Apply V_{DD}
3. Set all inputs to a known state

To power-down the device, reverse the steps above.

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic voltage supply	10.8	12	13.2	V
HV_{OUT}	High voltage output	-0.3	-	225	V
V_{IH}	High-level input voltage	V_{DD}-2.0	-	V_{DD}	V
V_{IL}	Low-level input voltage	0	-	2.0	V
f_{CLK}	Clock frequency	-	-	8.0	MHz
T_A	Operating free-air temperature	-40	-	+85	°C

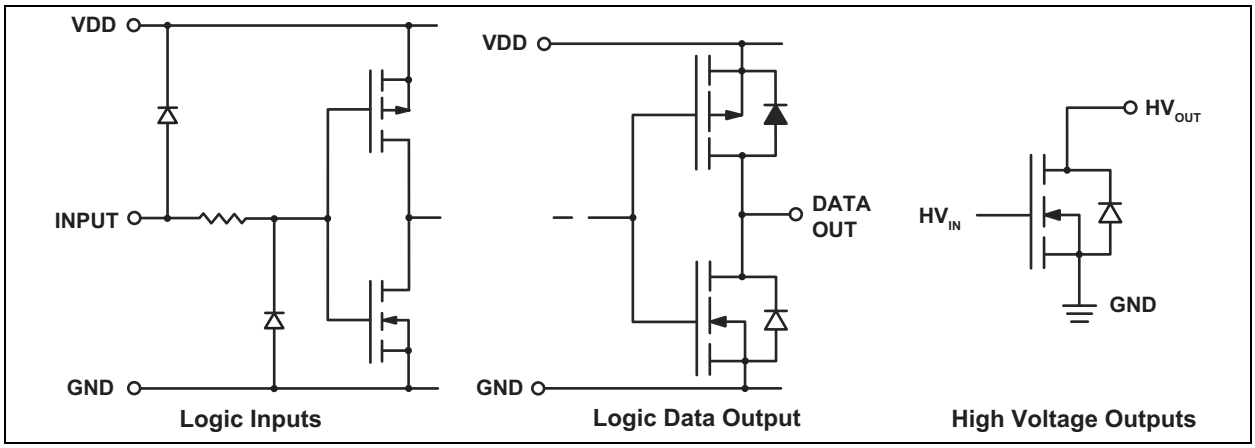


FIGURE 3-1: *Input and Output Equivalent Circuits*

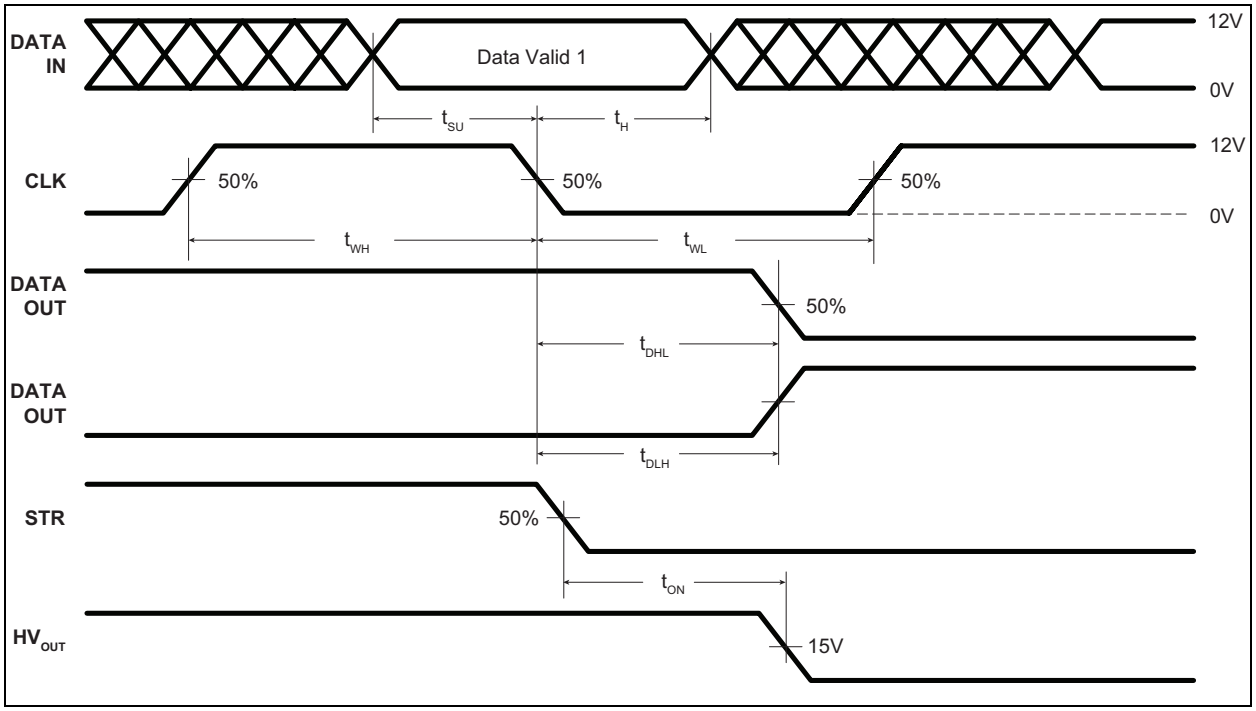
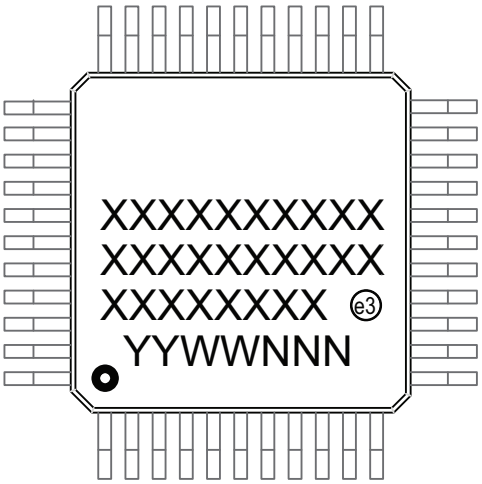


FIGURE 3-2: *Switching Waveforms*

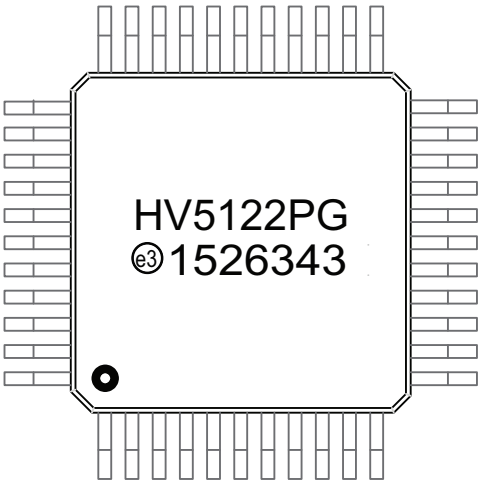
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

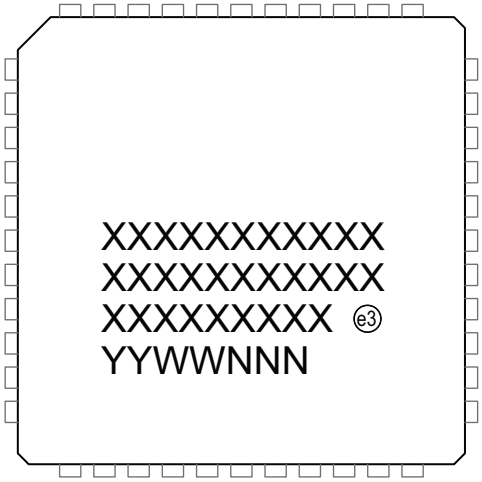
44-lead PQFP



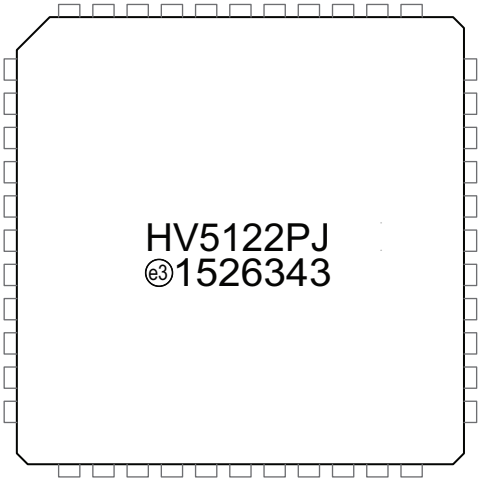
Example



44-lead PLCC



Example

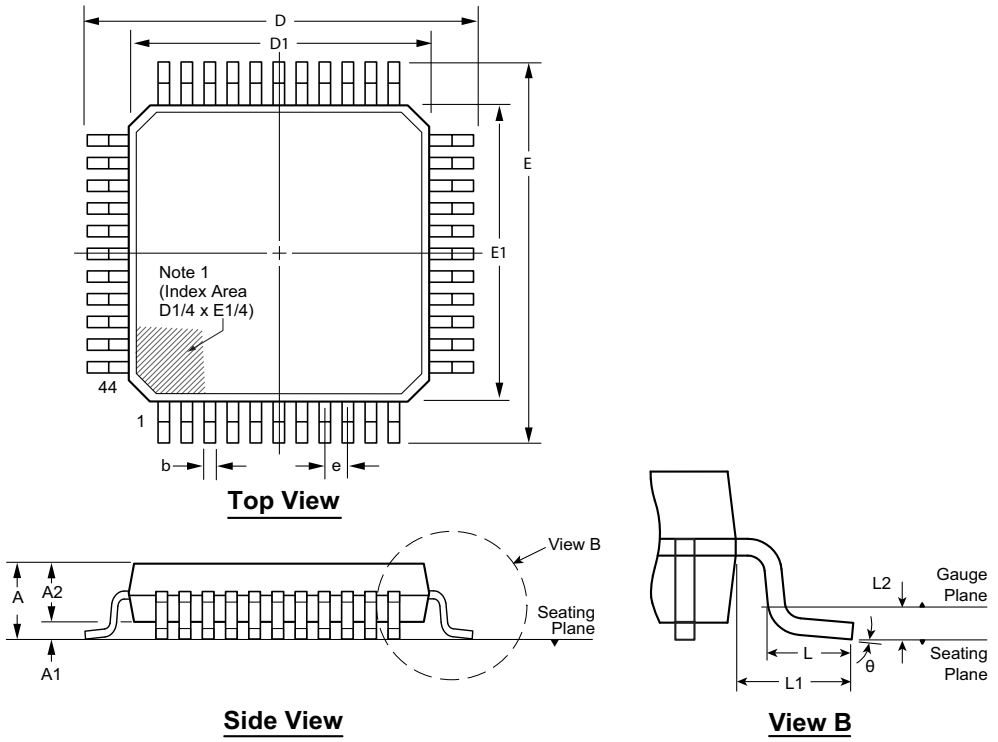


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

44-Lead PQFP Package Outline (PG)

10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

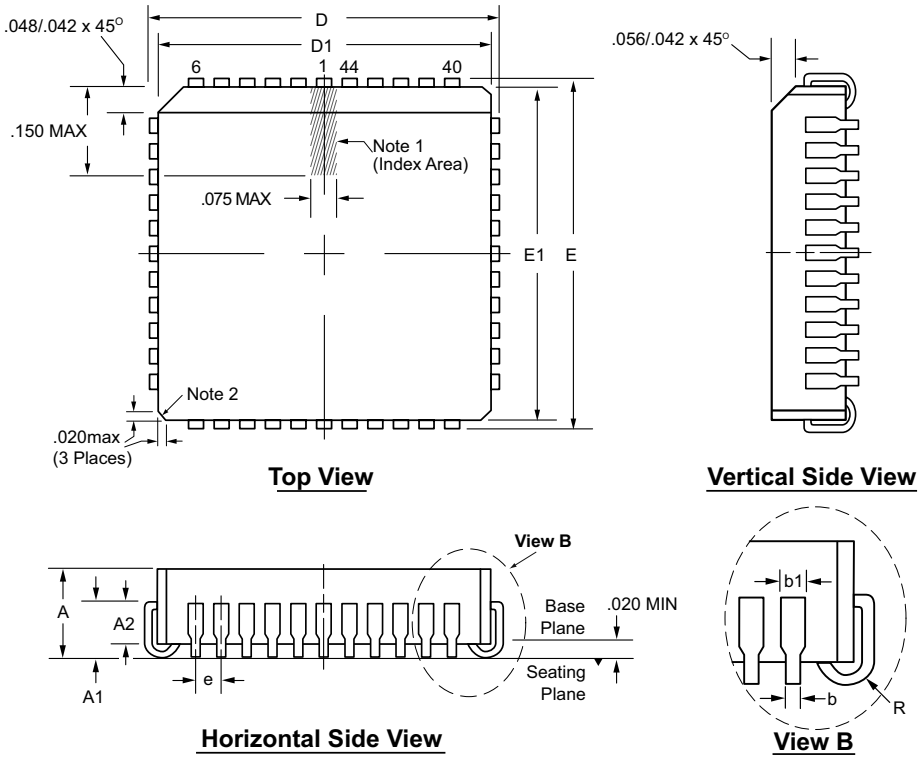
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (August 2015)

- Update file to new format

Revision B (October 2015)

- Updated Continuous total power dissipation in Absolute Maximum Ratings on page 3
- Corrected a typo on page 13

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV5122 =	32-Channel Serial to Parallel Converter, data shifts in counter-clockwise direction
	HV5222 =	32-Channel Serial to Parallel Converter, data shifts in clockwise direction
Package:	PG =	44-Lead PQFP
	PJ =	44-Lead PLCC
Environmental	G =	Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank) =	96/Tray for PG package
	=	27/Tube for PJ package

Examples:

a)	HV5122PG-G	Data shifts in counter-clockwise direction, 44-Lead PQFP package, 96/Tray
b)	HV5222PJ-G	Data shifts in clockwise direction, 44-Lead PLCC package, 27/Tube

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