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100MHz, 80-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

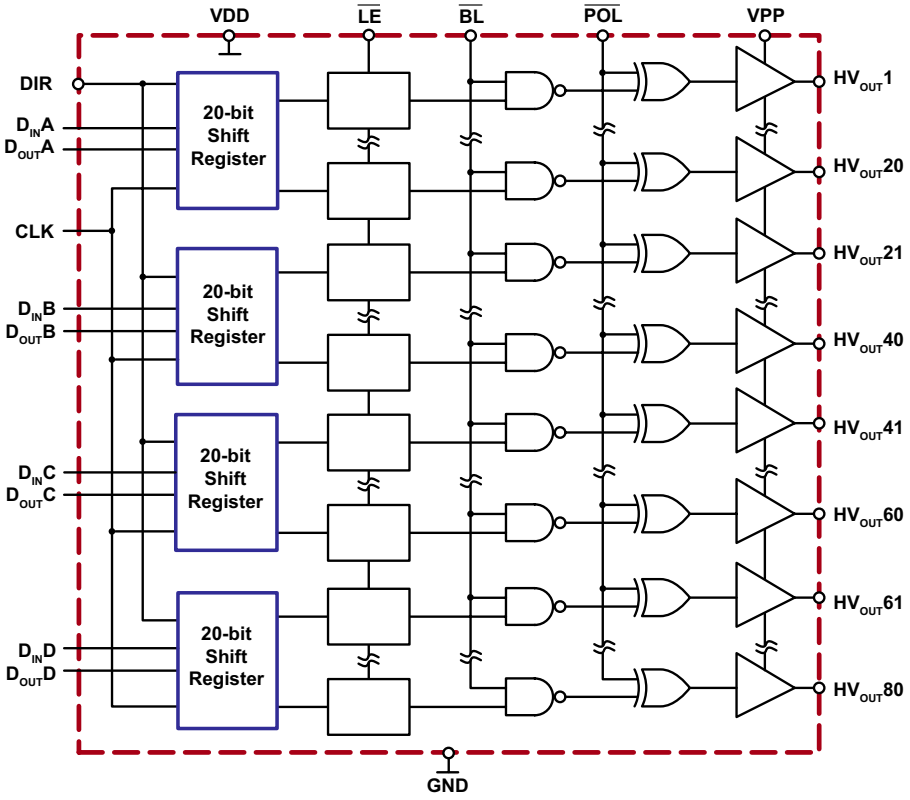
- HVCMOS® technology
- 5.0V CMS Logic
- Output voltage up to 80V
- Low power level shifting
- 100MHz equivalent data rate using four dynamic shift registers
- Latched data outputs
- Foreward and reverse shifting options (DIR pin)
- Diode to VPP allows efficient power recovery
- Outputs may be hot switched

General Description

The HV574 is a low-voltage serial to high-voltage parallel con-verter with push-pull outputs. This device has been designed for use as a driver for printer applications. It can also be used in any application requiring multiple output high-voltage current sour-cing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 4 parallel 20-bit dynamic shift registers, permitting data rates 4X the speed of one (they are clocked together). There are 80 static latches and control logic to perform the polarity select and blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to VDD. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}80$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latches is stored when $\overline{LE}$ is low.

Functional Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV574PG-G	100-Lead PQFP	66/Tray

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

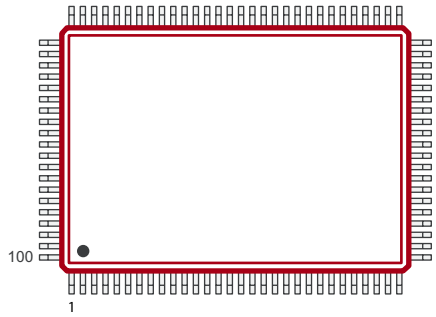
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +7.5V
Output voltage, V_{PP}	-0.5V to +90V
Logic input levels	-0.3V to V_{DD} +0.3V
Ground current[1]	1.5A
Continuous total power dissipation[2]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

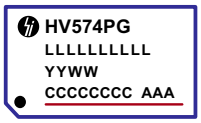
1. *Limited by the total dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to 85°C at 20mW/°C.*

Pin Configuration



100-Lead PQFP
(top view)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
____= "Green" Packaging

Package may or may not include the following marks: Si or

100-Lead PQFP

Typical Thermal Resistance

Package	θ_{ja}
100-Lead PQFP	39°C/W

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output voltage	12	80	V
V_{IH}	High-level input voltage	V_{DD} -0.5V	-	V
V_{IL}	Low-level input voltage	0	0.5	V
f_{CLK}	Clock frequency per register	0.001	25	MHz
T_A	Operating free-air temperature	-40	+85	°C

Notes:

Power-up sequence should be the following:

1. Apply ground
2. Apply V_{DD}
3. Set all inputs (Data, CLK, Enable etc.) to a known state
4. Apply V_{PP}

The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics *(Over recommended operating conditions unless otherwise noted)*

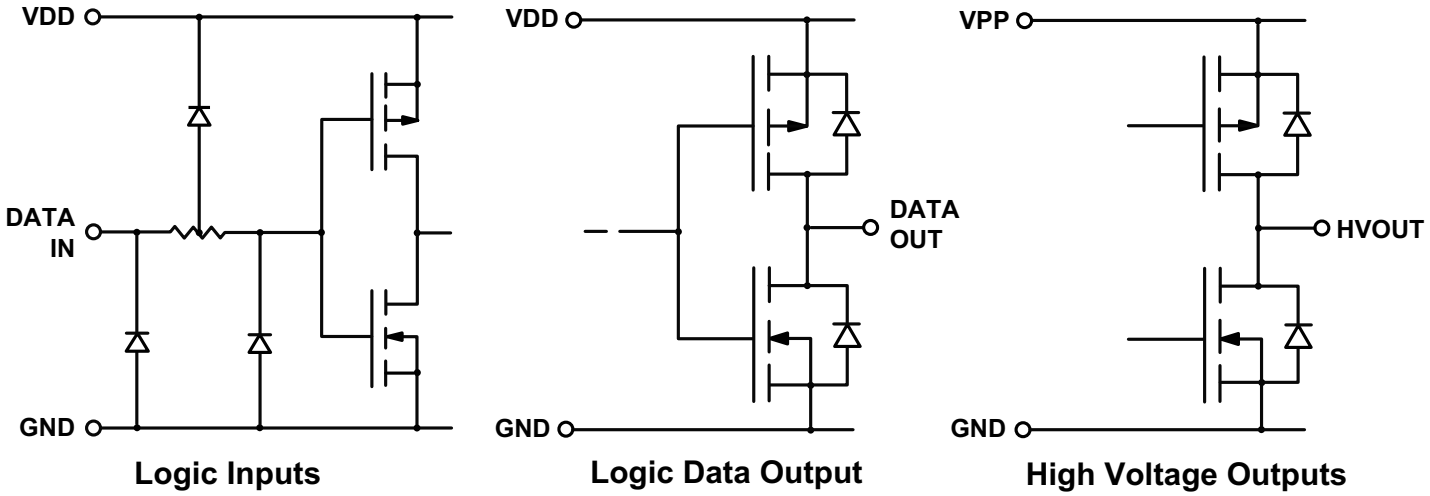
Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	30	mA	$V_{DD} = V_{DD}$ max, f_{CLK} = 25MHz
I_{PP}	Quiescent V_{PP} supply current		-	100	µA	Outputs high
			-	100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All $V_{IN} = V_{DD}$
V_{OH}	High-level output	HV_{OUT}	V_{PP} -9.0	-	V	I_O = -30mA, V_{PP} = +80V
		Data out	V_{DD} -0.5	-	V	I_O = -100µA
V_{OL}	Low-level output	HV_{OUT}	-	3.75	V	I_O = +15mA, V_{DD} = +5.0V
		Data out	-	0.5	V	I_O = +100µA
I_{IH}	High-level logic input current		-	1.0	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-	-1.0	µA	V_{IL} = 0V

AC Electrical Characteristics *(T_A = 85°C max. Logic signal inputs and data inputs have t_r, $t_f \leq$ 5.0ns [10% and 90% points])*

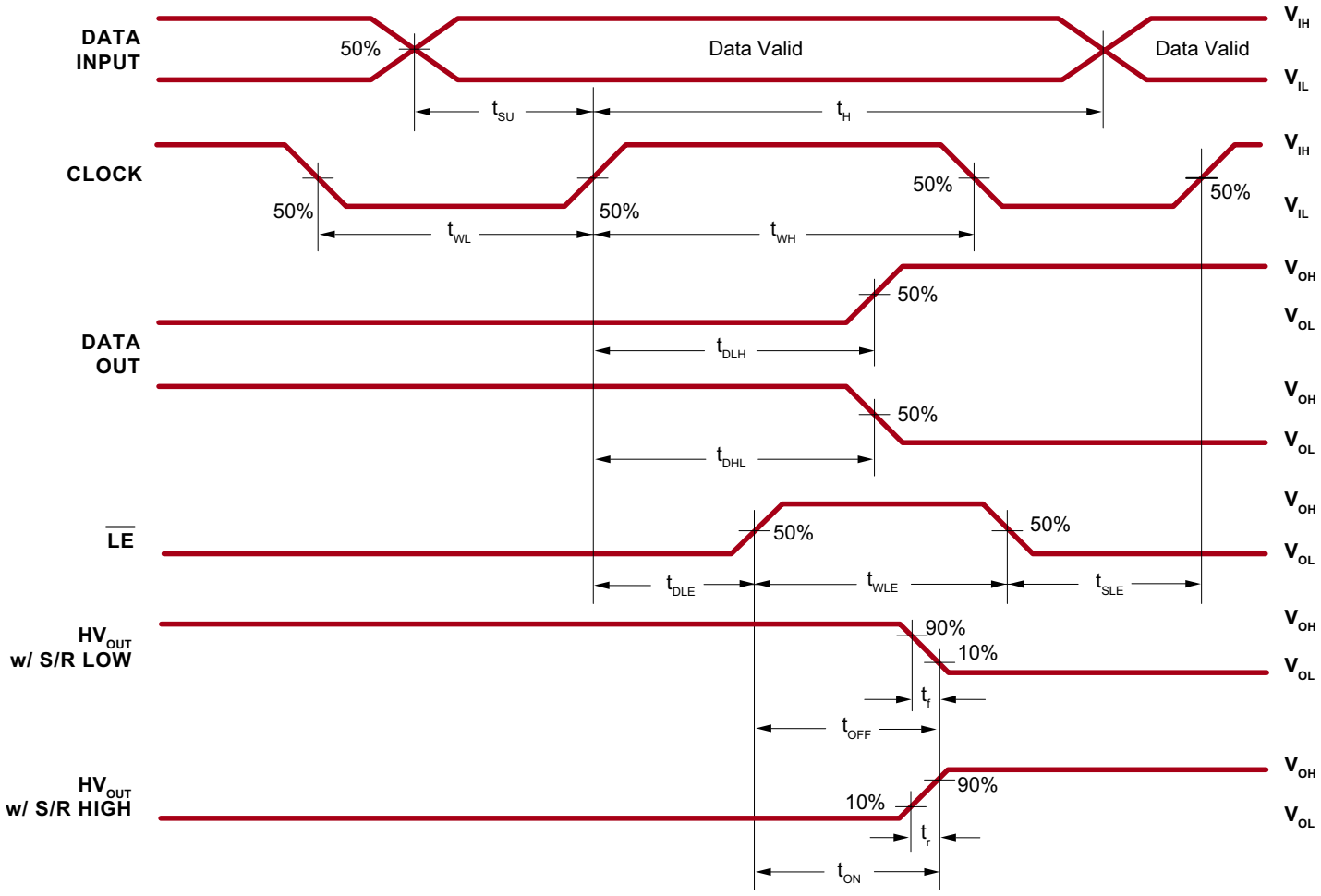
Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	0.001	25	MHz	V_{DD} = 4.5V, T_J = 25°C
		0.001	20		V_{DD} = 4.5V, T_J = 125°C
t_{WL}, t_{WH}	Clock width high or low	20	-	ns	---
t_{SU}	Data set-up time before clock rises	0	-	ns	---
t_H	Data hold time after clock rises	15	-	ns	---
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}	-	500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low	-	38	ns	C_L = 15pF, V_{DD} = 5.0V
t_{DLH}	Delay time clock to data low to high	-	38	ns	C_L = 15pF, V_{DD} = 5.0V
t_{DLE}*	Delay time clock to $\overline{LE}$ low to high	25	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	25	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0	-	ns	---
t_r, t_f	Output rise/fall time	-	1.0	µs	C_L = 600pF, HV_{OUT} from 0 - 60V

** t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).*

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P high	X	X	X	L	L	X	-	H	-
All O/P low	X	X	X	L	H	X	-	L	-
O/P normal	X	X	X	H	H	X	-	No inversion	-
O/P inverted	X	X	X	H	L	X	-	Inversion	-
Data falls through (latches transparent)	L	↑	H	H	H	X	L	L	-
	H	↑	H	H	H	X	H	H	-
	L	↑	H	H	L	X	L	H	-
	H	↑	H	H	L	X	H	L	-
Data stored/ latches loaded	X	X	L	H	H	X	*	Stored Data	-
	X	X	L	H	L	X	*	Inversion of stored data	-
I/O relation	$D_{IN}X$	↑	H	H	H	H	$Q_n \rightarrow Q_{n+1}$	New H or L	$D_{OUT}X$
	$D_{IN}X$	↑	L	H	H	H	$Q_n \rightarrow Q_{n+1}$	Previous H or L	$D_{OUT}X$
	$D_{OUT}X$	↑	L	H	H	L	$Q_n \rightarrow Q_{n-1}$	Previous H or L	$D_{IN}X$
	$D_{OUT}X$	↑	H	H	H	L	$Q_n \rightarrow Q_{n-1}$	New H or L	$D_{IN}X$

Note:

** = dependent on previous stage's state. See Pin configuration for DIN and DOUT pin designation for CW and CCW shift.*

Pin Function

Pin #	Function
1	$HV_{OUT}30$
2	$HV_{OUT}29$
3	$HV_{OUT}28$
4	$HV_{OUT}27$
5	$HV_{OUT}26$
6	$HV_{OUT}25$
7	$HV_{OUT}24$
8	$HV_{OUT}23$
9	$HV_{OUT}22$
10	$HV_{OUT}21$
11	$HV_{OUT}20$
12	$HV_{OUT}19$
13	$HV_{OUT}18$
14	$HV_{OUT}17$
15	$HV_{OUT}16$
16	$HV_{OUT}15$
17	$HV_{OUT}14$
18	$HV_{OUT}13$
19	$HV_{OUT}12$
20	$HV_{OUT}11$
21	$HV_{OUT}10$
22	$HV_{OUT}9$
23	$HV_{OUT}8$
24	$HV_{OUT}7$
25	$HV_{OUT}6$

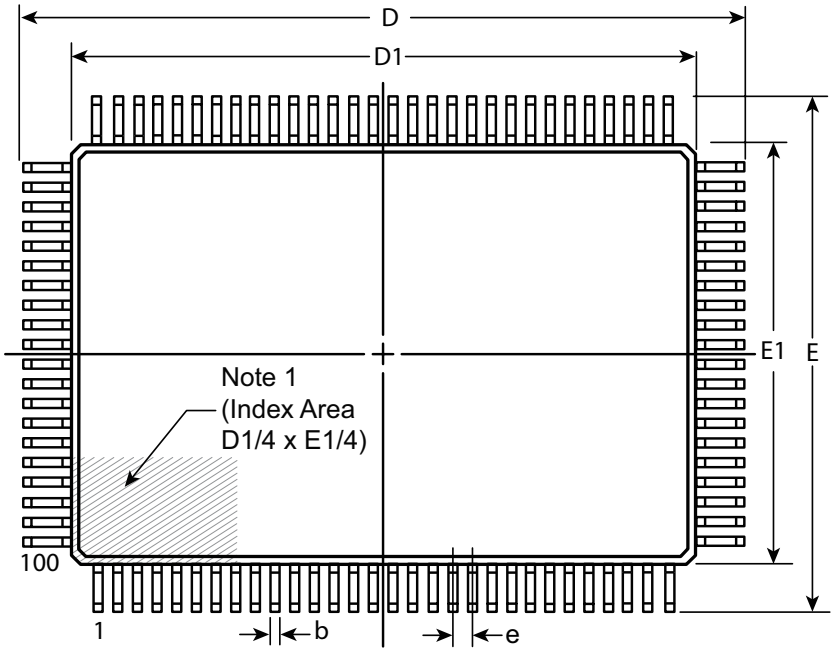
Pin #	Function
26	$HV_{OUT}5$
27	$HV_{OUT}4$
28	$HV_{OUT}3$
29	$HV_{OUT}2$
30	$HV_{OUT}1$
31	NC
32	VPP
33	HVGND
34	$D_{IN}A$
35	$D_{IN}B$
36	$D_{IN}C$
37	$D_{IN}D$
38	VDD
39	$\overline{POL}$
40	$\overline{LE}$
41	CLK
42	DIR
43	$\overline{BL}$
44	GND
45	$D_{OUT}D$
46	$D_{OUT}C$
47	$D_{OUT}B$
48	$D_{OUT}A$
49	HVGND
50	VPP

Pin #	Function
51	$HV_{OUT}80$
52	$HV_{OUT}79$
53	$HV_{OUT}78$
54	$HV_{OUT}77$
55	$HV_{OUT}76$
56	$HV_{OUT}75$
57	$HV_{OUT}74$
58	$HV_{OUT}73$
59	$HV_{OUT}72$
60	$HV_{OUT}71$
61	$HV_{OUT}70$
62	$HV_{OUT}69$
63	$HV_{OUT}68$
64	$HV_{OUT}67$
65	$HV_{OUT}66$
66	$HV_{OUT}65$
67	$HV_{OUT}64$
68	$HV_{OUT}63$
69	$HV_{OUT}62$
70	$HV_{OUT}61$
71	$HV_{OUT}60$
72	$HV_{OUT}59$
73	$HV_{OUT}58$
74	$HV_{OUT}57$
75	$HV_{OUT}56$

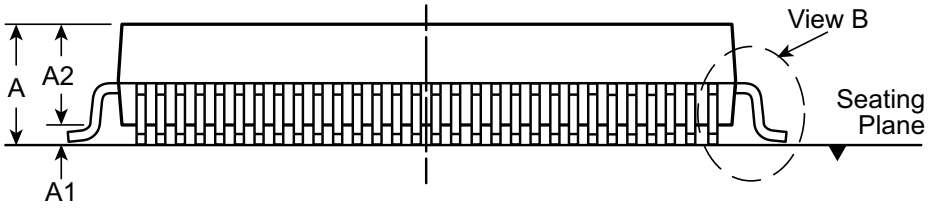
Pin #	Function
76	$HV_{OUT}55$
77	$HV_{OUT}54$
78	$HV_{OUT}53$
79	$HV_{OUT}52$
80	$HV_{OUT}51$
81	$HV_{OUT}50$
82	$HV_{OUT}49$
83	$HV_{OUT}48$
84	$HV_{OUT}47$
85	$HV_{OUT}46$
86	$HV_{OUT}45$
87	$HV_{OUT}44$
88	$HV_{OUT}43$
89	$HV_{OUT}42$
90	$HV_{OUT}41$
91	$HV_{OUT}40$
92	$HV_{OUT}39$
93	$HV_{OUT}38$
94	$HV_{OUT}37$
95	$HV_{OUT}36$
96	$HV_{OUT}35$
97	$HV_{OUT}34$
98	$HV_{OUT}33$
99	$HV_{OUT}32$
100	$HV_{OUT}31$

100-Lead PQFP Package Outline (PG)

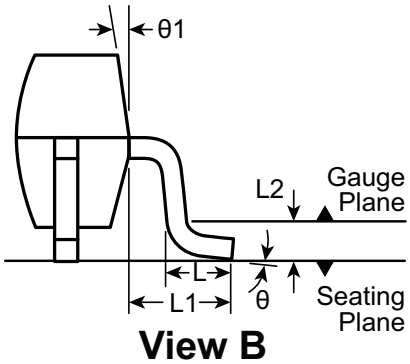
20.00x14.00mm body, 3.40mm height (max), 0.65mm pitch, 3.90mm footprint



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.80*	0.25	2.55	0.22	23.65*	19.80*	17.65*	13.80*	0.65 BSC	0.73	1.95 REF	0.25 BSC	0	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.38	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CC-1, Issue B, Sept.1995.
** This dimension is not specified in the JEDEC drawing..*
Drawings not to scale.
***Supertex Doc. #:** DSPD-100PQFPPG, Version B041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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