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AMS101 Evaluation Card

User Guide

UG886 (v1.3) November 6, 2013

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/16/2012	1.0	Initial Xilinx release.
10/19/2012	1.1	Section AMS101 Evaluation Card Overview, page 7 explains that reference designs are now supplied for the ZC702, KC705, and VC707 base boards, and how to download the designs. Cable terminology changed to *Standard-A plug to Mini-B plug USB cable* and *Standard-A plug to Micro-B plug USB cable*, and these two cables are added to the kit. Board drawings and photographs in Figure 1-2 and Figure 1-2 were updated. Procedures in Hardware and Software Setup, page 12 were updated. Figure 2-4, Figure 2-5, and Figure 2-9 were updated. The AMS102 characterization card was removed. In Analyze Internal Voltage and Temperature Sensors, page 24, *Open* is replaced with *Select*. Figure 3-4 and Figure 3-6 were replaced. In Appendix B, Required Jumper Settings for Base Boards, a note was added that the triangle represents pin 1. Jumper J65 on the ZC702 board changed to *In place*. Some references in the book and in Appendix C, Additional Resources changed. Appendix D, Regulatory and Compliance Information now includes a link to the Declaration of Conformity and markings for waste electrical and electronic equipment (WEEE), restriction of hazardous substances (RoHS), and CE compliance.

Date	Version	Revision
02/14/2013	1.2	Chapter 1, AMS101 Evaluation Card Overview: Instances of *AMS101* evaluator tool were corrected to *AMS* evaluator tool. Added part HW-AMS101-G. Reference design files are now downloaded from www.xilinx.com/support/documentation/ams101_evaluation_card.htm. The AC701 board is now supported. The bullet with "AMS evaluator tool graphical user interface" was removed from section AMS101 Evaluation Card, page 7. Download information for the AMS evaluator tool graphical user interface is listed in the last bullet on page 7 and the bullet about "FPGA programming files..." was removed. Chapter 2, AMS101 Evaluation Card Quick Start: The onboard signal source is from a 16-bit dual DAC, page 11. In step 1, page 12, download information changed. In step 7, page 16, the AC701 kit and kit documentation references were added. Various changes were added to step 9, page 18. Added section Power Monitoring with XADC on AC701, page 24. Chapter 4, AMS Evaluator Tool: Decimation information and Table 4-2 were added on page 44. Appendix A, Targeted Design Platforms, Schematics, and Dynamic Performance Metric Calculation Methodology: AC701 was added to the Supported Targeted Design Platforms section. Appendix B, Required Jumper Settings for Base Boards: Added Jumper Settings for the AC701 Board, page 52.
11/06/2013	1.3	Updated for Vivado® Design Suite 2013.3. Procedures in step 7, page 16 were revised for the Vivado tool and the KC705 ZIP file name changed. Support for Zynq®-7000 ZC706 AP SoC was added in Jumper Settings for the ZC706 Board, page 52. Updated Appendix C, Additional Resources links. The link to the Declaration of Conformity, page 55 was updated.

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Appendix D: Regulatory and Compliance Information

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Chapter 1

AMS101 Evaluation Card Overview

Overview

AMS101 Evaluation Card

The Xilinx 7 series FPGAs and Zynq-7000® All Programmable System on a Chip (AP SoC) each feature two 1 Mega-sample per second (MSPS), 12-bit, Xilinx analog-to-digital converters (XADCs) built into the device (FPGA or SoC). The Analog Mixed Signal (AMS) technology combines the XADC analog measurement with the device's logic for simple system monitoring to more signal processing-intensive tasks like linearization, calibration, oversampling, and filtering. The AMS101 evaluation card (part number HW-AMS101-G) provides an analog source to verify the XADC and AMS performance. The AMS101 evaluation card plugs into all Xilinx 7 series FPGA and Zynq-7000 AP SoC base boards. Reference designs are supplied for the ZC702, KC705, AC701, and VC707 base boards. Download these files from either the individual kit support pages or the AMS101 Evaluation Card website. For convenience, the KC705 FPGA base board is used as the example in this document (see Figure 1-1). The KC705 evaluation kit includes hardware and soft content required to evaluate XADC and to determine how it can be useful in the end system.

To evaluate the Xilinx Analog Mixed Signal (AMS) capability, these items from the kit are needed:

- Access to the XADC header (see Figure 1-1)
- AMS101 evaluation card (see Figure 1-2 and Table 1-1 for a description of features)
- Two USB cables (1x Standard-A plug to Mini-B plug USB cable and 1x Standard-A plug to Micro-B plug USB cable for download and debug
- USB-UART drivers
- Download AMS reference design files from the AMS101 Evaluation Card website.
- Download AMS evaluator tool graphical user interface (*7 Series FPGA and Zynq-7000 AP SoC AMS Evaluator Installer for AMS Targeted Reference Design*—see Figure 1-3).

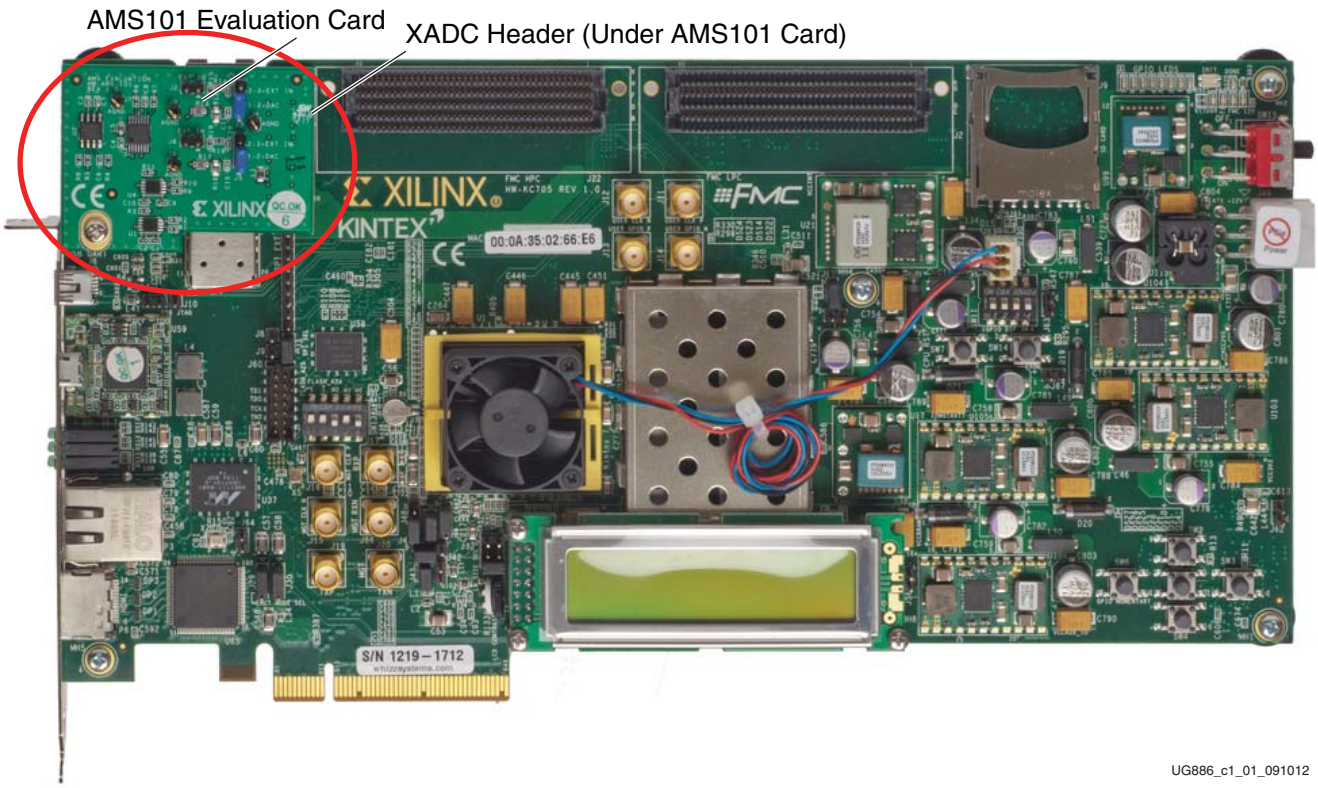

Figure 1-1: **KC705 Evaluation Board with the AMS101 Evaluation Card Installed**

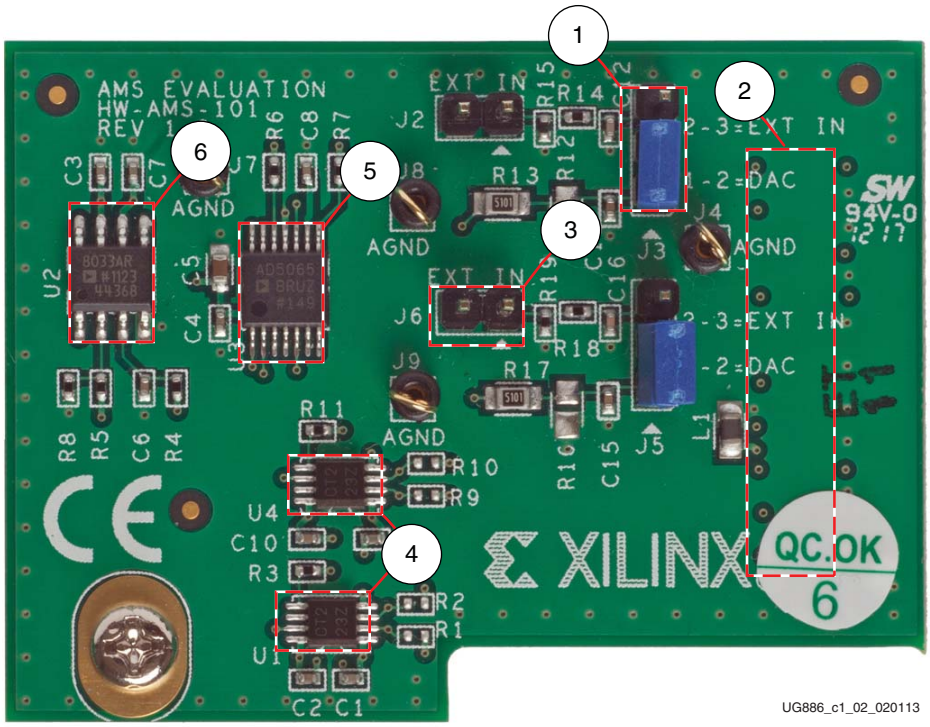

Figure 1-2: **AMS101 Evaluation Card Features**

Table 1-1: **AMS101 Evaluation Card Features**

Callout	Component Description
1	Jumpers to select DAC or external signal source.
2	20-pin connector to the XADC header on the FPGA or AP SoC base board.
3	Pins allow for external analog input signals.
4	Digital I/O level translators.
5	16-bit DAC sets analog test voltage.
6	Reference buffer for DAC.

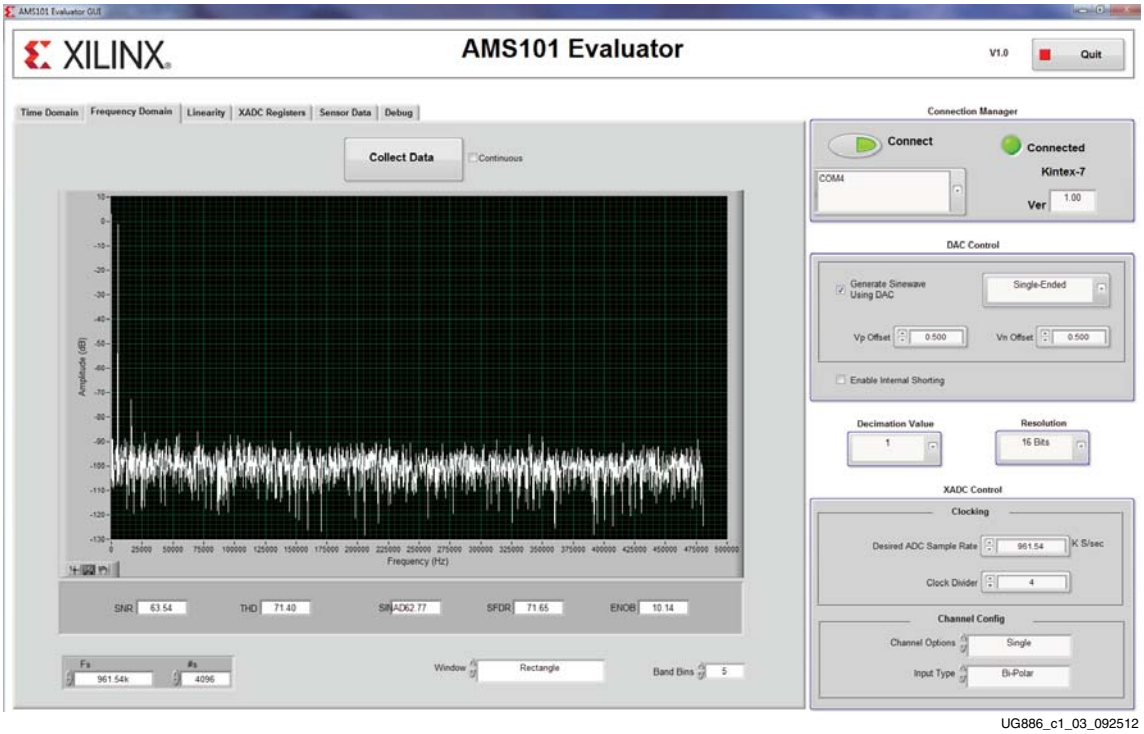

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Figure 1-3: **AMS Evaluator Tool GUI**

Chapter 2

AMS101 Evaluation Card Quick Start

To facilitate easy evaluation of key performance metrics of the XADC and AMS technology, Xilinx developed the AMS evaluation platform for all 7 series FPGA and Zynq-7000 AP SoC base boards. The AMS evaluation platform (Figure 2-1) enables key ADC performance metrics to be observed and evaluated. The remainder of this document describes in detail the hardware and software that comprise the AMS evaluation platform.

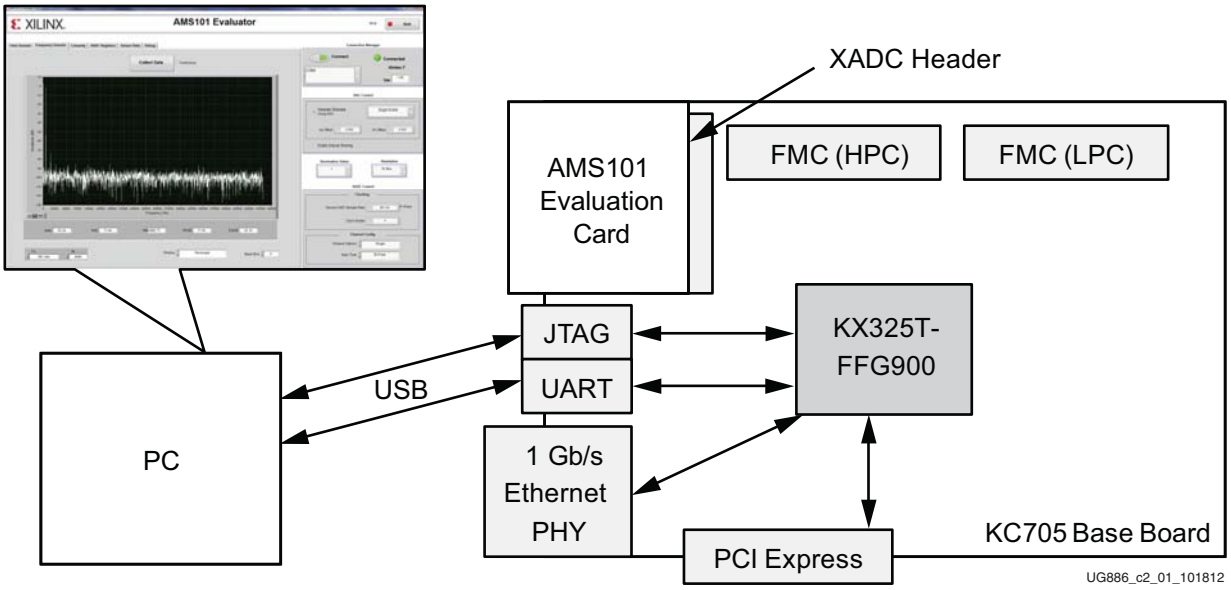

Figure 2-1: **AMS Evaluation Platform**

AMS Evaluation Platform Features

The AMS evaluation platform provides:

- A complete XADC and AMS evaluation solution
- An onboard signal source from a 16-bit dual DAC
- Configurable analog inputs
- An interactive GUI
- Interfaces for all the latest Xilinx FPGA or AP SoC base boards, including the KC705 Kintex-7 FPGA base board, as detailed in this document. (See the full list of supported base boards in Appendix A).

Each base board kit contains:

- One AMS101 evaluation card
- USB-UART drivers
- A base board *Getting Started Guide*

Quick Start

Eight steps are needed to get the AMS evaluation platform up and running. This chapter covers how to perform these steps as well as how to run key ADC performance tests after setup.

Hardware and Software Setup

1. Install the AMS Evaluator tool GUI.

   Download the AMS Evaluator installer files (*7 Series FPGA and Zynq-7000 AP SoC AMS Evaluator Installer for AMS Targeted Reference Design*) from the AMS101 Evaluation Card Support Page. Click the `setup.exe` file to install the National Instruments LabVIEW RunTime Engine needed to host the AMS Evaluator tool.

   The GUI itself has been built using National Instruments LabVIEW 2011 software. To enable use of the GUI without the need for a LabVIEW license, Xilinx has bundled the LabVIEW run-time engine with the GUI installer. During the installation process, the run time engine is installed on the PC.

2. Connect the FPGA base board.

   Ensure that the FPGA base board power switch (e.g., SW15 on the KC705 base board) is in the OFF position. Figure 2-2 shows the position of the power switch on the board.

3. Connect the host PC to the UART port with the Standard-A plug to Mini-B plug USB cable. Also connect the Standard-A plug to Micro-B plug USB cable to the JTAG port. See the corresponding photo in the *Getting Started Guide* for each particular base board.

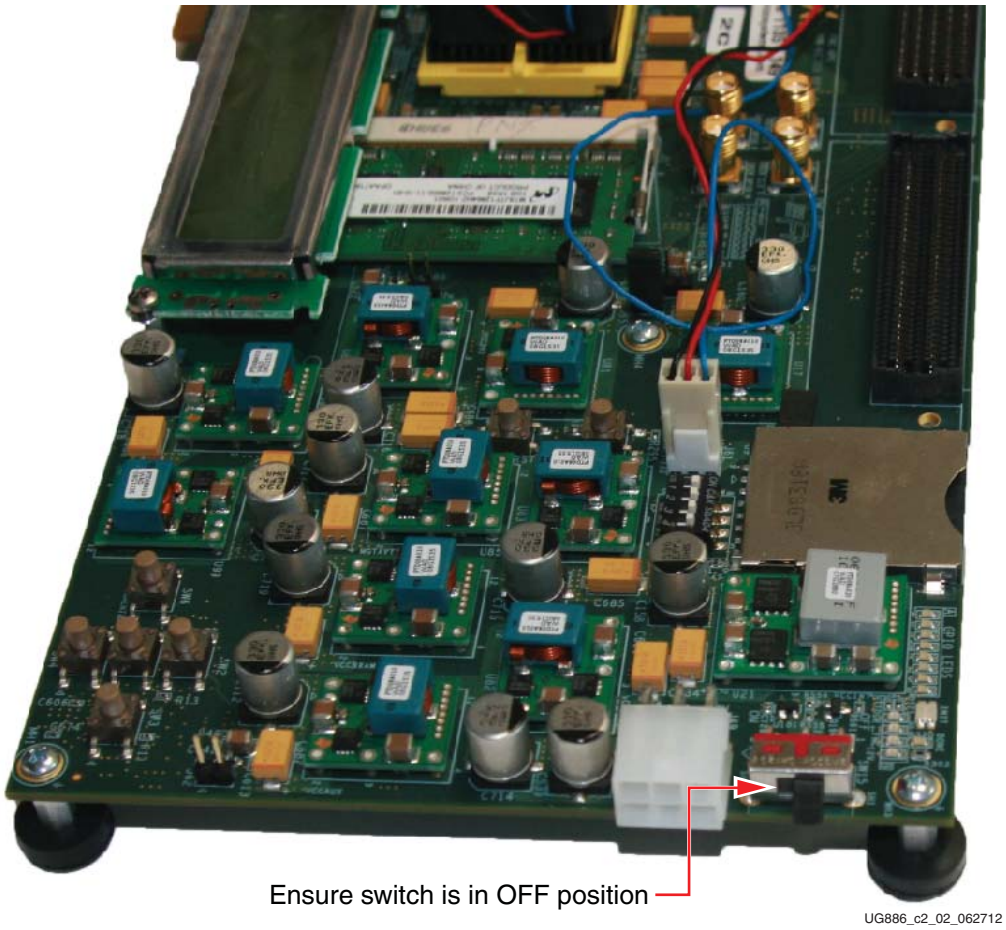

Figure 2-2: **Power Switch on the FPGA Base Board**

Three connections are required for the FPGA base board: power, the USB-UART connection to the PC, and the JTAG Standard-A plug to Micro-B plug USB programming cable. Figure 2-3 shows how to connect these on the KC705 base board.

Caution! Do not turn on the power switch until step 6, page 16.

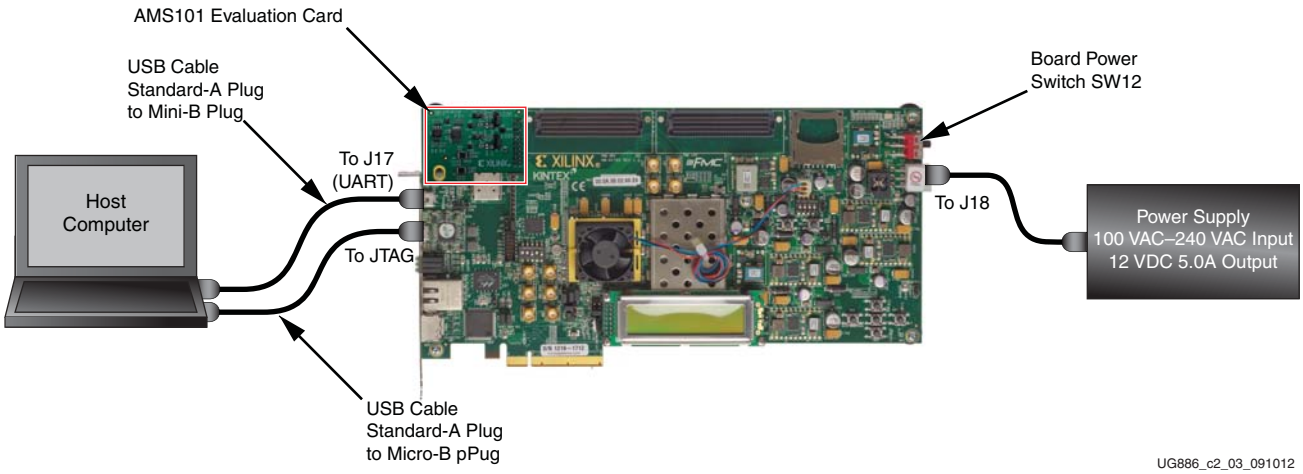

Figure 2-3: **FPGA Base Board Connectivity**

4. Configure the FPGA base board jumper settings as listed in Appendix B, Required Jumper Settings for Base Boards.
5. Connect the AMS101 evaluation card to the XADC header on the base board.

   The AMS101 evaluation card connects to the FPGA base board by plugging the card into the XADC header on the base board. The AMS101 evaluation card connector and XADC header socket are keyed to align properly. Pin 1 on the XADC header needs to connect to pin 1 of the 20-pin connector on the AMS101 evaluation card. Figure 2-4 shows this connection.

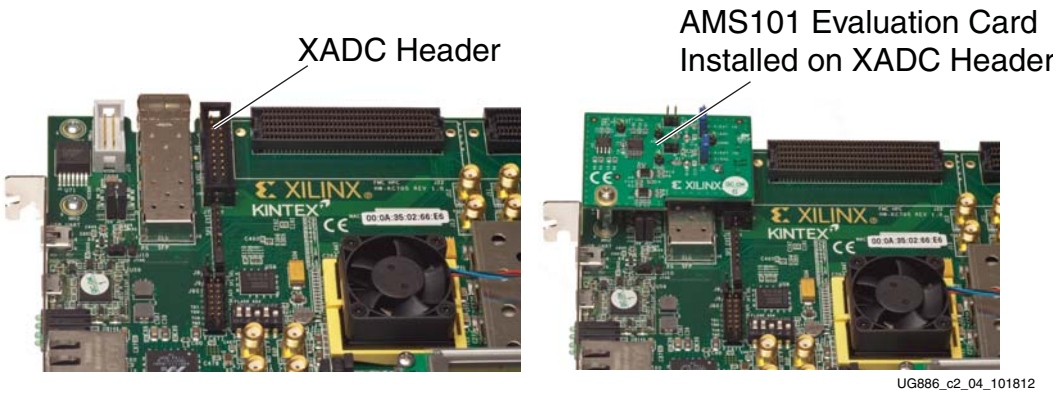

Figure 2-4: **AMS101 Evaluation Card Installed on the Base Board XADC Header**

Ensure that all the jumper settings are correct on the AMS101 evaluation card. Figure 2-5 shows an example of jumpers J3 and J5 (DACs enabled). Table 2-1 explains additional jumpers.

Note: The image in Figure 2-5 is for reference only and might not reflect the current revision of the board.

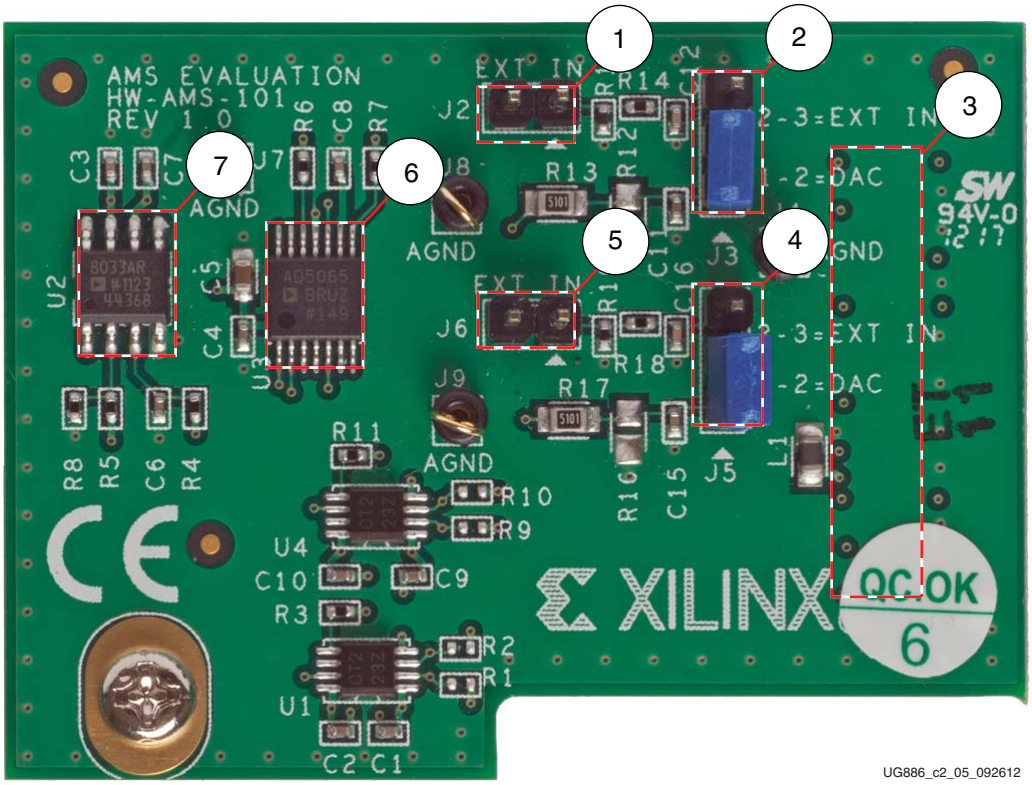

Figure 2-5: **AMS101 Evaluation Card Jumper Configuration**

Table 2-1: **AMS101 Evaluation Card Jumper Configuration Notes**

Callout	Reference Designator	Component Description	Notes	Schematics
1	J2	Jumper	External signal source to V_P positive analog input.	Figure A-2, page 49
2	J3	Jumper	1–2 selects DAC signal source. 2–3 selects external input source on J2.	Figure A-2, page 49
3		Connector	20-pin connector to XADC header on FPGA base board.	Figure A-2, page 49
4	J5	Jumper	1–2 selects DAC signal source. 2–3 selects external input source on J6.	Figure A-2, page 49
5	J6	Jumper	External signal source to V_N negative analog input.	Figure A-2, page 49
6		DAC	16-bit DAC sets analog test voltage.	Figure A-1, page 48
7		Amplifier	Reference buffer for DAC.	Figure A-1, page 48

6. Power up the FPGA base board.

   The power switch can now be put in the ON position (switch toward the power plug). Figure 2-6 shows the location of the power switch. It also shows the LEDs illuminated on the FPGA base board. This should occur directly after the FPGA base board switch is flipped into the ON position. A few seconds after power-up, the DONE LED should illuminate. At this stage, hardware connection is complete.

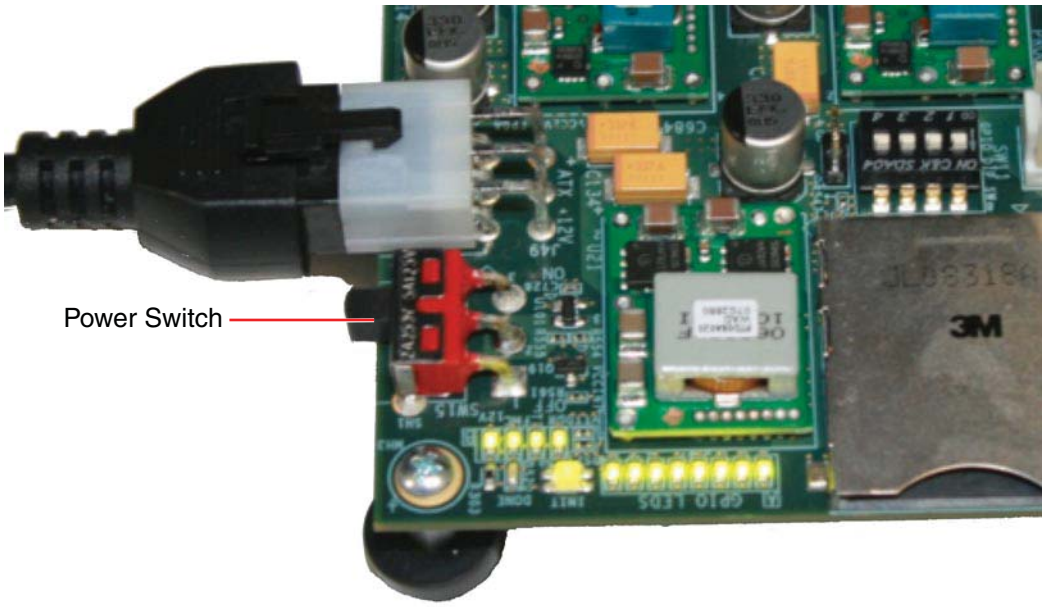

Figure 2-6: **Turning On the FPGA Base Board Power**

7. Download the design to the FPGA. See the individual kit (AC701, ZC702, KC705, or VC707) Getting Started Guides or the *7 Series FPGA AMS Targeted Reference Design User Guide* (UG960) [Ref 1], for more specific instructions on downloading the design.

   For the AMS101 evaluation card to function, the FPGA needs to be programmed with the appropriate design. To do this, download the design to the FPGA:

   a. Open the Vivado ® Design Suite. Here is one example path for Vivado tools: `Start menu/Xilinx Design Tools/Vivado 2013.3/Vivado 2013.3`
   b. Create a Vivado Project.
   c. Open a Hardware Session.
   d. Open a new Hardware Target and run through the wizard.
   e. Open `AMS_KC705_bitstream.bit` from the `rdf0280-ams101-kc705-trd-2013-3.zip` file.

The LEDs on the FPGA base board should light up as the design is downloading. Figure 2-7 shows an example of the LEDs lit up after the KC705 board is programmed.

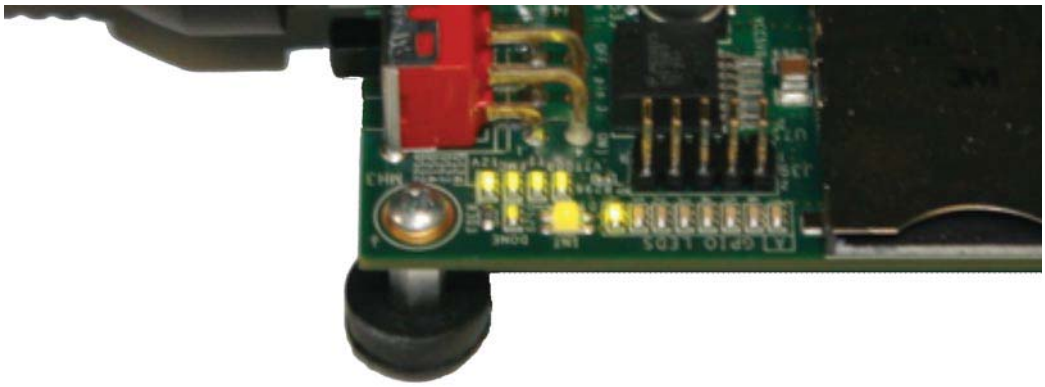

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Figure 2-7: **LEDs after Programming the FPGA with the Design**

8. Run the AMS101 evaluator LabVIEW GUI executable file.

   If the AMS Evaluator tool GUI was successfully installed, an icon should be displayed on the desktop and in the Windows start menu (see Figure 2-8). To open the AMS Evaluator tool GUI, click the red Xilinx **X** icon. The GUI shown in Figure 2-9 should appear.

   Note: Do not press anything on the GUI until step 9 is performed.

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Figure 2-8: **AMS Icon**

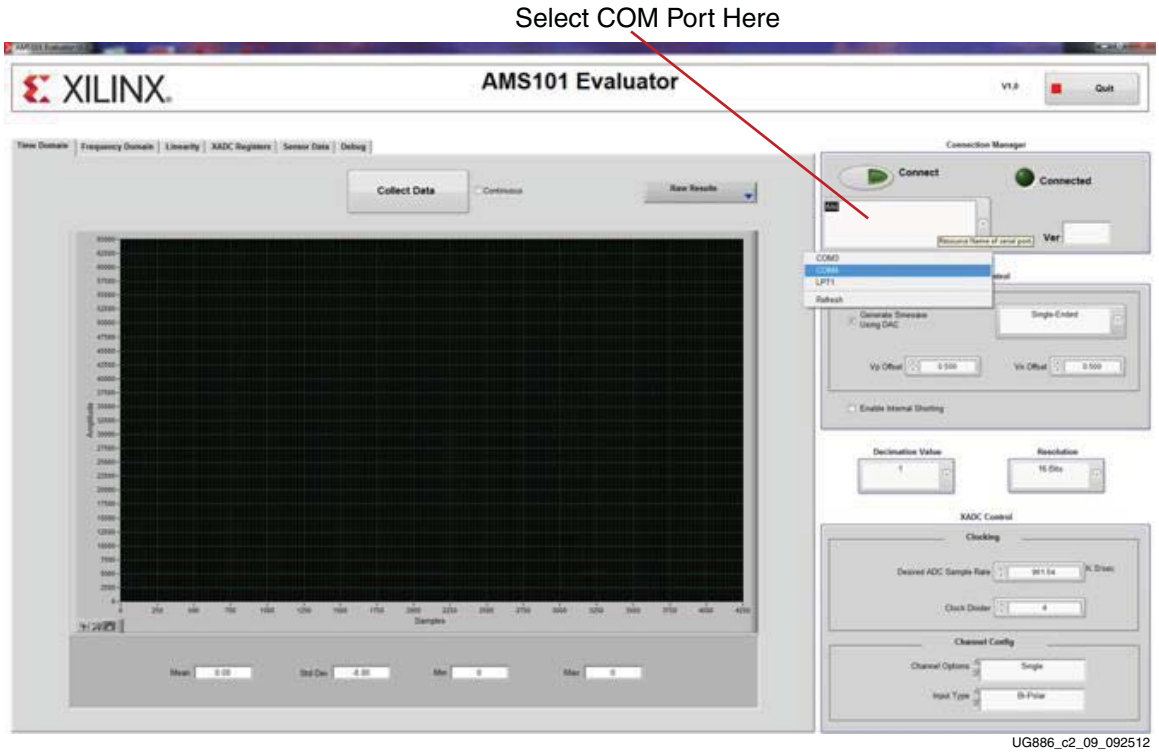

Figure 2-9: **AMS Evaluator Tool on Start-Up**

9. Connect to the UART port as detailed in the appropriate FPGA/processor base board Getting Started Guide:
   - *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883) [Ref 2]
   - *Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit* (UG848) [Ref 3]
   - *Zynq-7000 All Programmable SoC: ZC702 Evaluation Kit and Video and Imaging Kit Getting Started Guide* (UG926) [Ref 4]
   - *Artix-7 FPGA AC701 Evaluation Kit Getting Started Guide* (UG967) [Ref 5]

   Set the USB-UART connection to a known port in the Device Manager as follows:
   - Right-click **`My Computer`** and select **`Properties`**.
   - Select the **`Hardware`** tab. Click the **`Device Manager`** button.
   - Find and right-click the Silicon Labs device in the list. Then select **`Properties`**.
   - Click the **`Port Settings`** tab and the **`Advanced...`** button.
   - Select the COM port that corresponds to **`Silicon Labs CP210x USB to UART Bridge`** (see Figure 2-10).

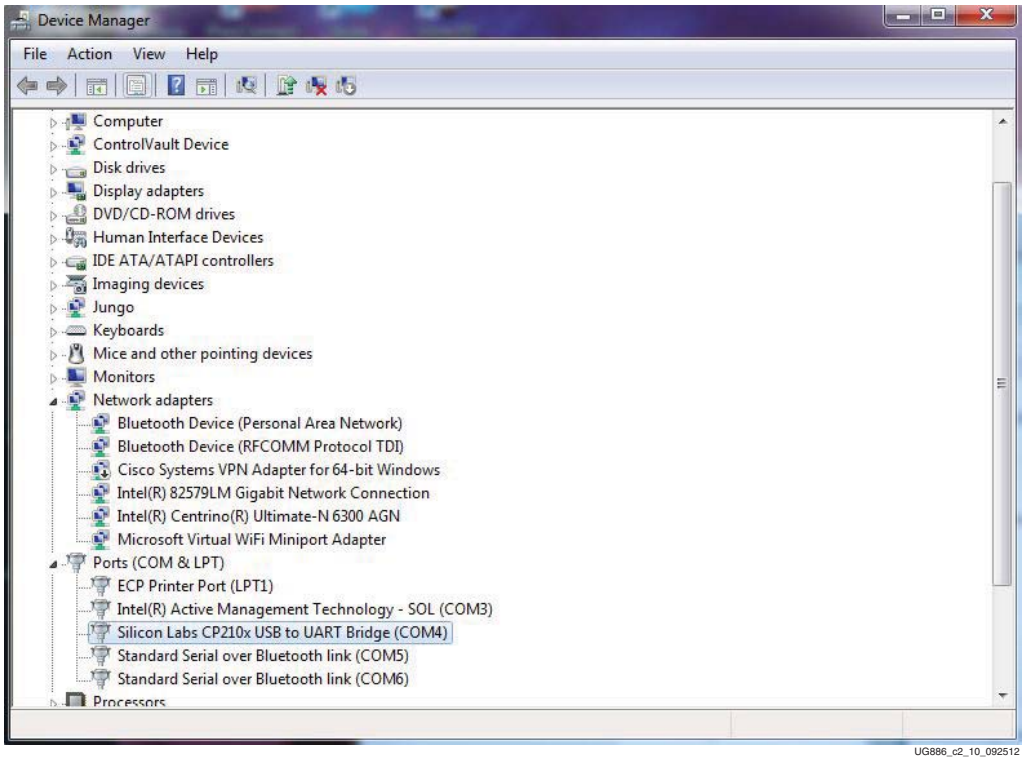

Figure 2-10: **UART-USB Port in Device Manager**

Select the appropriate COM port from the pull-down menu on the GUI as show in Figure 2-11. Then click the **Connect** button. After the AMS Evaluator tool is connected, the kit name is displayed below the green **`Connected`** circle. If the AMS Evaluator tool is unable to connect, be sure the correct COM port is selected and click refresh.

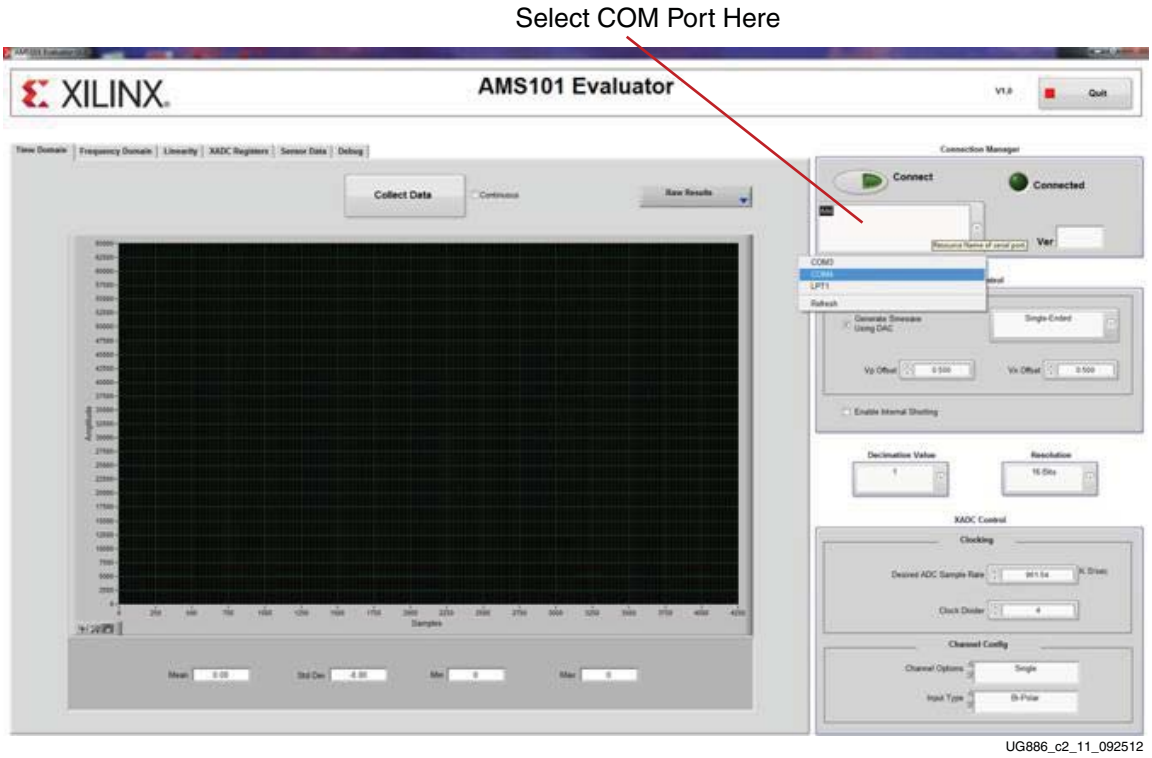

Figure 2-11: **AMS Evaluator Tool COM Port Selection**

Run Key Performance Tests

All of the software and hardware should be configured and running. The AMS101 evaluation card can now be used to perform measurement tests on the XADC.

Collect Time Domain Data

To collect time domain data, press the **Collect Data** button shown in Figure 2-12. A sine wave should display on the screen. This sine wave has been generated by the digital-to-analog converter (DAC) on the AMS101 evaluation card and passed through to the XADC inputs where it was digitized.

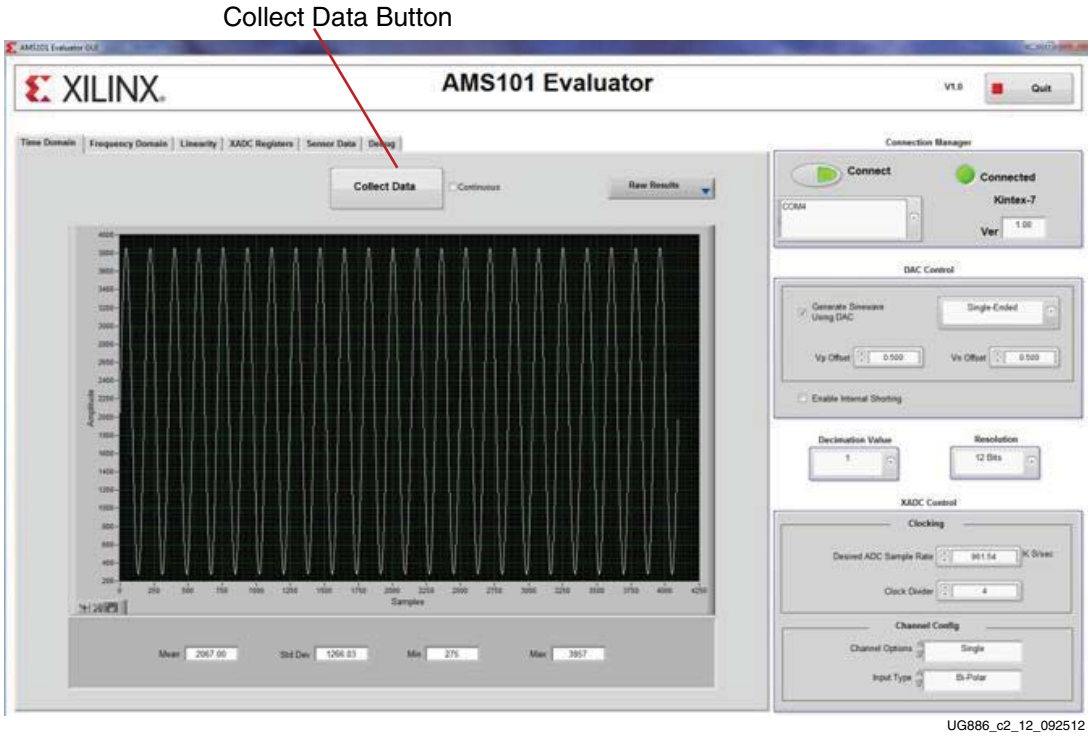

Figure 2-12: **Run-Time Domain Data Capture**

Perform Fast Fourier Transform Analysis

To analyze the performance of the XADC in the frequency domain, select the **Frequency Domain** tab (see Figure 2-13). When selected, a Fast Fourier Transform (FFT) is performed on the XADC data just viewed in the time domain. The signal-to-noise ratio, total harmonic distortion, effective number of bits (ENOB), and other AC parameters are calculated and displayed in the data panel below the FFT plot as shown in Figure 2-13. A new data capture from the XADC can be collected by pressing the **Collect Data** button.

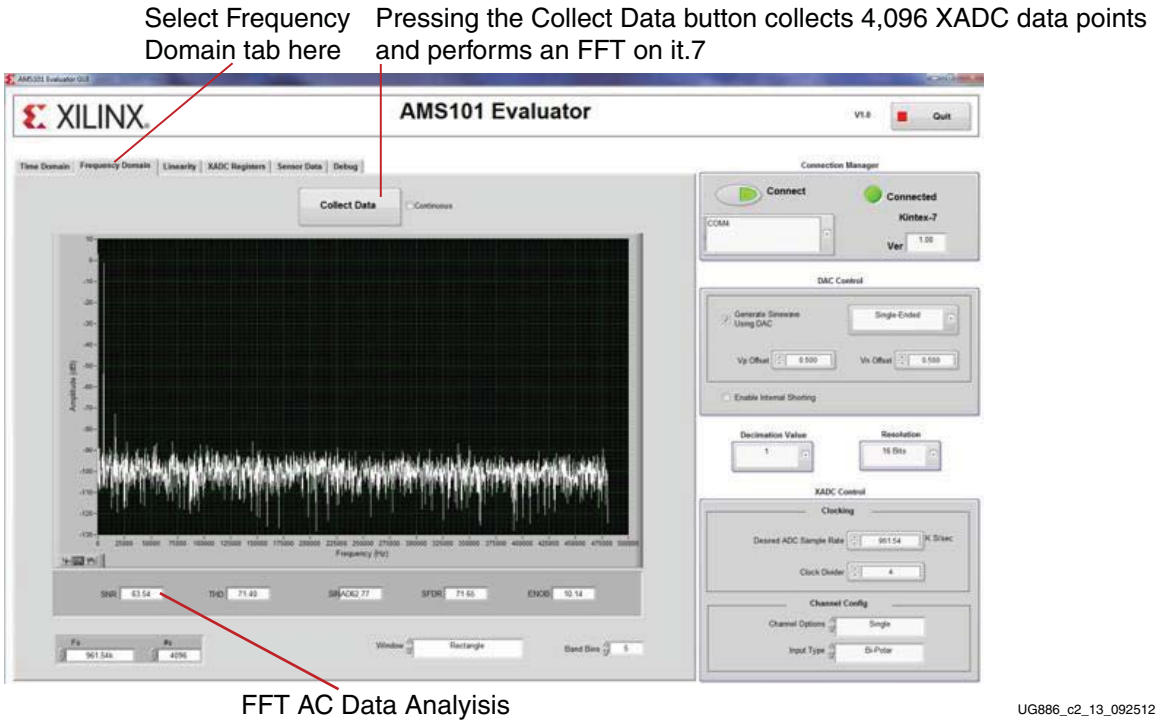

Figure 2-13: **Frequency Domain Analysis and Data Capture**

Perform a Linearity Test

To analyze the linearity of the XADC, select the **Linearity** tab and click the **Collect Data** button. After a short wait, both the integral and differential non-linearity data is displayed on two separate plots along with the minimum and maximum values at the bottom of the screen as shown in Figure 2-14.

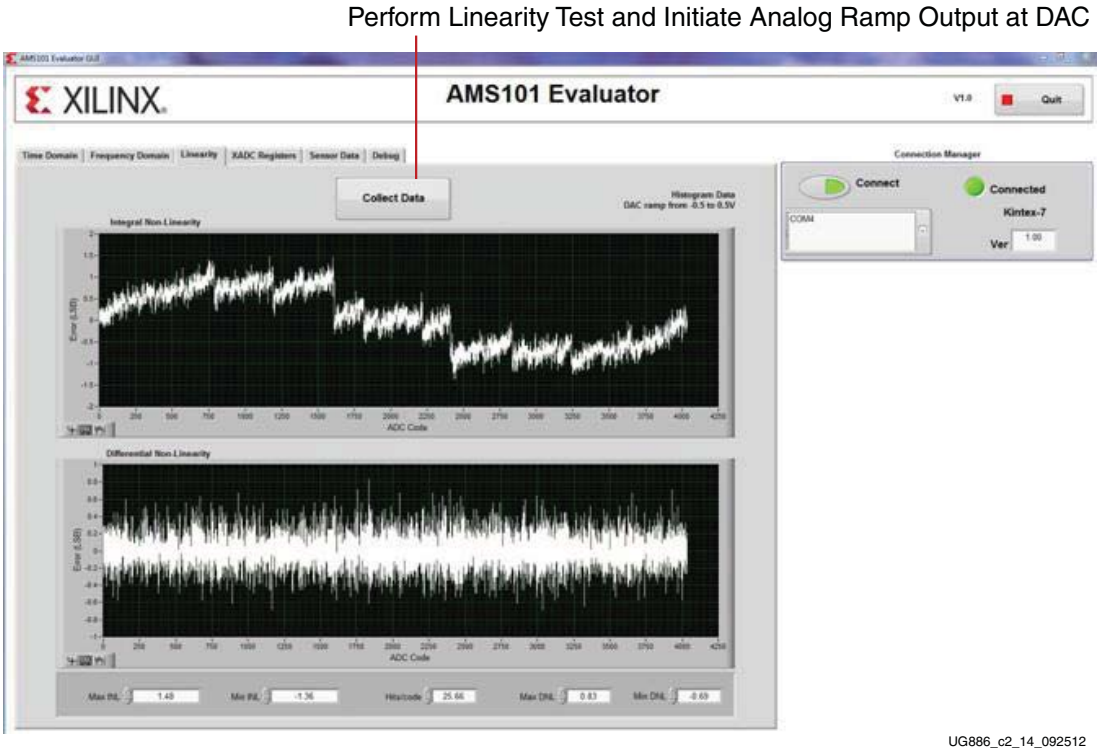

Figure 2-14: **Linearity Error Data Capture and Analysis**

Analyze Internal Voltage and Temperature Sensors

The XADC also has several internal sensors that it digitizes. These include a temperature sensor and FPGA voltage supply sensors. Select the **Sensor Data** tab to view the data corresponding to the four sensors, as shown in Figure 2-15.

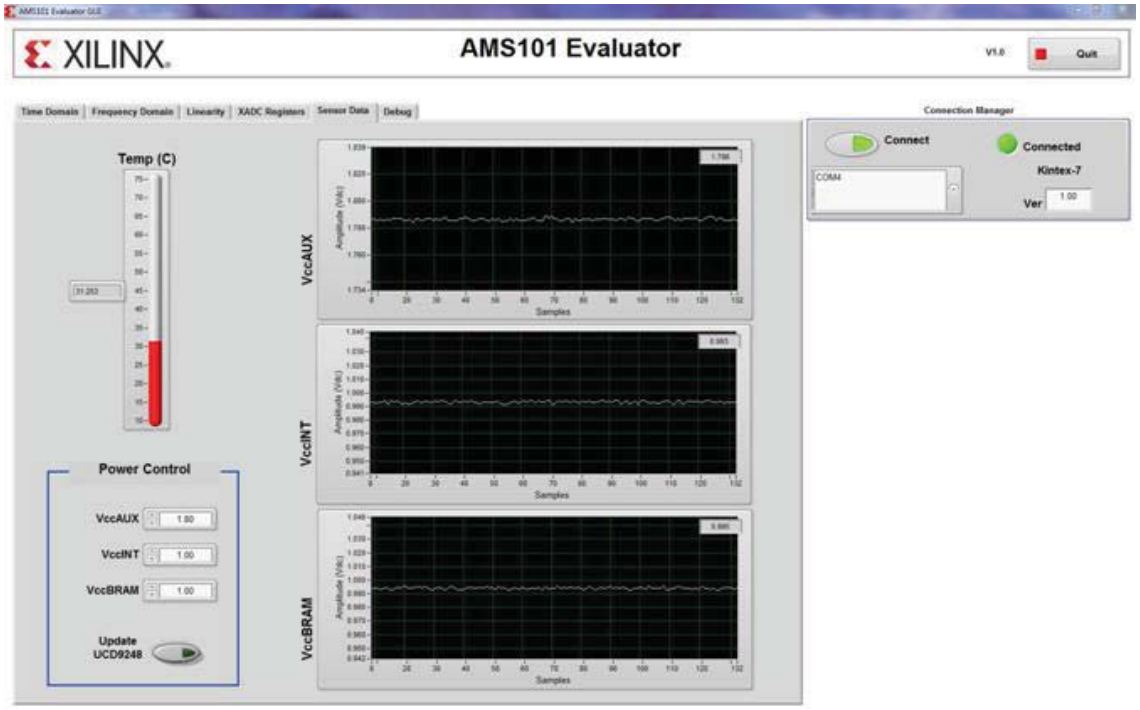

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Figure 2-15: **Sensor Data Capture**

Power Monitoring with XADC on AC701

The AC701 evaluation board and AMS Evaluator tool offer a complete system monitoring solution. The AC701 uses the XADC to measure voltage and load current on nine of the onboard power supplies. Voltage is measured using remote sensing. Current is measured across a sense resistor with individual current sense op amps. Power is then calculated for each of the nine rails by multiplying voltage x current. An external multiplexer is also used

to switch all 18 measurements into the XADC. Table 2-2 details the power rails monitored on the AC701.

Table 2-2: **AC701 Voltage Rails Measured with AMS Targeted Reference Design**

Rail Name	Voltage	Current
V_{CCINT}(1)	No	Yes
V_{CCAUX}(1)	No	Yes
V_{CCBRAM}(1)	No	Yes
1.5V Supply	Yes	Yes
V_{CCO_ADJ}	Yes	Yes
1.8V Supply	Yes	Yes
3.3V Supply	Yes	Yes
MGTAVCC	Yes	Yes
MGTAVTT	Yes	Yes

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} voltage levels are measured by XADC onboard sensors and displayed in both the **`Sensor Data`** tab and the **`Power Monitor`** tab.

The current sense values of V_{CCINT}, V_{CCAUX}, V_{CCBRAM}, 1.5V supply, and V_{CCO_ADJ} along with voltage levels of 1.5V supply, V_{CCO_ADJ}, and 1.8V supply are available on the AC701 board's onboard MUX positioned at U13. The differential output of the MUX is connected to auxiliary pin 1 (V_{AUX}P/N 1) of XADC and each channel is sampled once per second by the MicroBlaze™ processor program running as part of the AC701 AMS Targeted Reference Design.

The current sense values of 1.8V supply, 3.3V supply, MGTAVCC, and MGTAVTT along with voltage levels of 3.3V supply, MGTAVCC, and MGTAVTT are available on the AC701 board's onboard MUX positioned at U14. The differential output of the MUX is connected to auxiliary pin 9 (V_{AUX}P/N 9) of XADC.