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Xilinx Design Tools: Release Notes Guide

Vivado Design Suite and ISE Design Suite

UG631 (v2012.2, v14.2) July 25, 2012

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/25/2012	2012.2/14.2	Initial Xilinx Vivado Design Suite release./ISE Design Suite device and software updates.
05/08/2012	14.1	Initial Xilinx release.

Table of Contents

What's New in Xilinx Design Tools

Introducing Vivado Design Suite 2012.2

The Xilinx® Vivado™ Design Suite is a new IP and system-centric design environment which has been released for Public Access to all in-warranty ISE® Design Suite customers.

The following important information should be understood before beginning to use the Vivado Design Suite.

Improved Productivity

This entirely new tool solution was architected to increase the overall productivity for designing with the expanding portfolio of Xilinx devices. These new devices are now much larger and come with a variety of new technology including Stacked Silicon Interconnect Technology (SSIT), high speed I/O interfaces, hardened microprocessors and interfaces, analog mixed signal, etc. These new silicon features and capacity have allowed designers to move a lot more of the overall system design content into the FPGA. Designers are now faced with increased system design integration and verification challenges that require a different design methodology and toolset. This coupled with the increased capacity of the new devices made it clear a new tool solution was required. The Vivado Design Suite was developed to better address these new challenges.

Product Overview

The Vivado Design Suite is a completely new design solution created to address the design challenges described above. It is a complete replacement for the existing Xilinx ISE Design Suite of tools. It replaces all of the ISE point tools such as Xilinx Synthesis Tool (XST), implementation (ngdbuild-bitgen), Core Generator™system, Timing Constraints Editor, ISim, ChipScope™ analyzer, Xilinx Power Analyzer (XPA), FPGA Editor, PlanAhead™ design tool, SmartXplorer, etc. All of those capabilities are now built directly into the Vivado Integrated Design Environment (IDE) using a common data model and user interface.

The Vivado Design Suite takes advantage of a common data model used to process the design from RTL elaboration all the way through bitstream generation. The entire design process can be executed in memory without having to write or translate any intermediate

file formats. Having this common data model provides a lot of capabilities to analyze and affect the in-process design at each stage of the design flow.

The entire design process can be managed push-button by using the Flow Navigator in the Vivado IDE or controlled manually by using Tcl.

High-Level Synthesis

Engineers can quickly simulate, analyze and modify the design without being distracted with implementation details. By starting with MATLAB®/Simulink® or untimed C/C++/System C, one can quickly explore different system architectures, evaluating them against key system criteria without investigating effort in writing RTL. The Vivado System Edition extends algorithm development above RTL with Vivado High-Level Synthesis (HLS) and System Generator for DSP.

Vivado HLS (built on AutoESL tool technology) accelerates design implementation and verification by enabling C, C++, and SystemC specifications to be directly synthesized into VHDL or Verilog RTL, after exploring a multitude of micro-architectures based on design requirements. Functional simulation can be performed in C, providing an order of magnitude of acceleration over VHDL or Verilog simulation. This provides designers and system architects with a faster and more robust way of delivering quality designs.

Choosing Vivado Design Suite or ISE Design Suite

ISE Design Suite is an industry-proven solution for All Programmable Xilinx devices. The Xilinx ISE Design Suite continues to bring innovations to a broad base of developers, and extends the familiar design flow to all Xilinx FPGAs and Xilinx Zynq™-7000 projects.

The next-generation Xilinx Vivado Design Suite is a revolutionary IP and system-centric design environment that accelerates developer productivity for dramatically faster integration and implementation with an easy to use IP-centric design flow and up to 4x improvement in run times. Vivado Design Suite 2012.2 supports the Xilinx 7 series FPGAs, which include the Virtex®-7, Kintex™-7 and Artix™-7 families.

Vivado Design Suite offers better overall tool performance, especially on large designs. The design environment provides powerful flow customization and analysis using Tcl and Xilinx Design Constraints (XDC). Xilinx recommends customers starting a “new” design on Kintex K410 or larger device talk to your local FAE to determine if Vivado Design Suite is right for you. Xilinx does not recommend transitioning during the middle of a current design as design constraints and scripts are not compatible between the two tool flows.

No Cost in 2012 for Current ISE Design Suite Warranted Seats

If you purchased the ISE Design Suite in the last 12 months then you do not need to purchase the Vivado Design Suite during 2012. There is no additional cost for Vivado

Design Suite during 2012. All current, in warranty, seats of ISE Design Suite will receive an entitlement to a copy of Vivado Design Suite beginning with the 2012.2 release.

Vivado Design Suite Licensing

For customers who generated an ISE Design Suite license for versions 13 or 14, after February 2, 2012, your current license will also work for the Vivado Design Suite. Customers who are still in warranty but who have generated licenses prior to February 2, 2012, will need to regenerate their licenses in order to use Vivado Design Suite. For license generation, go to www.xilinx.com/getlicense.

ISE Design Suite to Vivado Design Suite Edition Mapping

Table 1-1: **Edition Mapping**

Pillars of Productivity	Vivado Features	ISE Design Suite License Level				
		WebPACK™ Tool*	Logic Edition	Embedded Edition	DSP Edition	System Edition
IP Integration and Implementation	Integrated Design Environment	X	X	X	X	X
Verification and Debug	Vivado Simulator	Limited	X	X	X	X
	Vivado Logic Analyzer		X	X	X	X
	Vivado Serial I/O Analyzer		X	X	X	X
Design Exploration and IP Generation	Vivado High-Level Synthesis				X	X
	System Generator for DSP				X	X

* The WebPACK design tools support a limited number of devices. The Webpack tool support for Vivado tools will not begin until late 2012.

Vivado Design Suite and WebPACK Design Tools

In 2012.2, the Vivado Design Suite is not available for users with a WebPACK tool license. The WebPACK tool access for the Vivado Design Suite is currently planned for late 2012.

Key New Features In Vivado Design Suite 2012.2

Device Support

- Production support for the following devices:
  - Kintex-7 325T

  - Kintex-7 410T
  - Virtex-7 X485T
- Virtex-7 HT devices are now in public access
- Performance increase of ~3.5% for the -2 speed grades for Kintex-7 and Virtex-7 FPGAs
- Updated Package Flight times and IBIS models for the Xilinx 7 series FPGAs
- Bitstream generation enabled for all the Xilinx 7 series FPGAs

Vivado Integrated Design Environment

- Vivado Simulator integration with common waveform viewer
- Integration with ISE Xilinx Platform Studio
- Xilinx Design Constraints (XDC) templates integrated into the source code editor
- Improved constraints file management
  - Integrated Design Environment (IDE) prompts user for target constraint file to write back to if changes are made in the IDE
- Ability to suppress and adjust message severity and verbosity
- Ability to create user-defined Design Rule Checks (DRC)
- Support for Verilog structural netlists flows from third-party synthesis tools
- Double-byte character support allowing Chinese characters to be present in paths and filenames

Vivado High-Level Synthesis

- High-Level Synthesis (HLS) is included in the Vivado System Edition, which supports all the Xilinx 7 series FPGAs. A stand-alone license which supports all devices supported by the ISE Design Suite is available, however Vivado System Edition must be installed to access the Vivado HLS software.
- Increased support for the number of `math.h` functions is now supported for synthesis.
- A new data type `hls::steam` has been added to support designs with streaming data.
- The synthesized RTL can now be exported as IP-XACT, Pcore and System Generator formats, allowing the RTL to be easily imported into Vivado, EDK and System Generator.
  - Exporting the synthesized RTL in IP-XACT and System Generator formats is only supported for the Xilinx 7 series FPGAs supported by Vivado Design Suite.
- Xilinx WebTalk and TouchPoint features are now integrated into Vivado HLS.

Vivado Synthesis Tools

- Support for finite state machine (FSM) optimizations
  - State encoding selectable with possible styles of “one-hot”, “sequential”, “Johnson” and “gray”
- RAM inference support for byte enable for all the modes of the BRAM
- DSP block inference for cascading and register packing and support for n-ary adders
- Support for synthesis attributes (including MARK_DEBUG)

Vivado Implementation Tools

- Timing report displays annotation for net delays to show delay type: no interconnect, estimation, or extracted route status
- Multi-threaded execution enabled by default
  - Default of 4 maximum simultaneous threads based on CPU availability
  - Configurable by users as needed
- Directed Routing support: ability to lock down routing for nets
- Strategies available based on place and route effort levels
- XDC enhanced
  - Support for LUT LOCK_PINS properties
  - XDC timing constraint equivalent for UCF FEEDBACK constraints added
- Timing report support for DDR interfaces - data sheet provides timing parameters in all corners and an optimal tap point
- New reporting commands
  - **`report_carry_chains`**
  - **`report_high_fanout_nets`**
- Native bitstream support
- Improved physical synthesis algorithms
- **`set_max_delay -datapathonly`** now permits combinatorial logic between **`-from`** and **`-to`**

Vivado Simulator

- Breakpoint support in the source code editor
- Value tool-tip in the source code editor

- Filter names in Scopes window
- Additional Tcl command support for
  - Adding conditions
  - Force commands
  - Write out Synopsys Activity Interchange Format file (SAIF)

Vivado IP Packager

The Vivado IP Packager is a unique design re-use feature based on the IP-XACT standard, that provides users the ability to package IP at any stage of the design flow - RTL, netlist, enabling the creation and deployment of system-level IP from Vivado IP Catalog. The key features of the Vivado IP Packager include:

- Package design as IP from the Vivado design tools project using the Vivado Integrated Design Environment (IDE) or automated script based flows using Tcl
- Specify synthesis, simulation, XDC constraints, HDL test bench, documentation and example sources for IP
- Create IP customization interface and specify device family support
- Create zip file for distribution of packaged IP

Vivado IP Catalog

The Vivado Design Suite has an extensible IP catalog which provides a repository for Xilinx, third-party and intra-company IP that can be shared across a design team, division, or company in a manner that facilitates design re-use. The key features of the Vivado IP Catalog include:

- Consistent, easy access to all Xilinx IP including building blocks, wizards, connectivity, DSP, embedded, AXI infrastructure and Video IP
- Support for multiple physical locations, including shared network drives, allowing users or organizations to leverage a consistent IP deployment environment for third-party or internally developed IP
- Instant access to IP customization and generation using the Vivado Integrated Design Environment (IDE) or automated script based flows using Tcl
- On demand delivery of optional IP output targets such as instantiation templates, simulation models (HDL, C, or MATLAB), and HDL example designs
- Integrated IP example designs that provide capability to evaluate IP directly as an instantiated source in a Vivado design tools project
- Global RTL synthesis of IP with design capability to use synthesizable RTL or behavioral simulation models of IP for simulation

- Capability to create a Verilog netlist by treating customized IP as top and then use post-synthesis back-annotated structural simulation models by using **`write_verilog`** or **`write_vhdl`**

Xilinx Documentation Navigator

To ensure access to the latest documentation, you should update the catalog in the Documentation Navigator weekly. It is especially important to update the catalog prior to your first use of Documentation Navigator.

Note: Additional Vivado Design Suite software documents will be made available August 8th through September 6th, 2012.

To update the catalog:

1. Launch the Xilinx Documentation Navigator by selecting **Help > Documentation and Tutorials** in the Vivado IDE.
2. In the Documentation Navigator, click the **Update Catalog** toolbar button.

For more information about the Documentation Navigator, see the *Vivado Design Suite User Guide: Getting Started (UG910)*, which is available on the Vivado Design Suite 2012.2 Documentation Page.

ChipScope Analyzer

- Debug Probing Flows
  - HDL Instantiation
  - Netlist Insertion
  - Flows (IDE push-button, Tcl, Checkpoints, Project & Non-Project)
- ILA 2.0 Core
  - Increased capacity and easier to use
  - No CONTROL port threading (No ICON core)
  - Compatible with Legacy IP (ICON, ILA, VIO 1.x)
  - Tcl scripting of IP parameterization and generation
- Vivado Logic Analyzer
  - Integration into Vivado IDE
  - Significantly enhanced waveform viewer with simulator-like capabilities
  - Tcl scripting of run-time operations

Pin Planner

- Export menu item from I/O ports view
- Support buses with ascending, descending, and negative bit indexes
- Expand selection menu item in IO ports view

System Generator for DSP

- MATLAB 2012a support
- Blockset Enhancements
  - Floating Point Natural Log
  - Floating/Fixed Point Abs
  - Interleaver/De-interleaver 7.1
- Demos and Examples Updated to target Kintex-7 device
- Vivado IP Generation for basic blocks including Dual Port RAM, ROM, Addressable Shift Register, FIFO, AXI_FIFO, Accumulator, AddSub, Counter, Multiplier, CMult
  - Up to 10x faster Netlist generation in designs containing these blocks
  - Ability to inspect the Vivado IP parametrization from Vivado project generated from SysGen
- Vivado HLS Block Enhancement
  - Enables inclusion of C/C++/SystemC source files through Vivado HLS integration
  - A new Median Filtering example introduced in examples/hls_filter to demonstrate the use of this block

IP Core Details

SMPTE SDI

- Support SD/HD/3G-SDI uncompressed serial digital video streams in the Xilinx 7 series FPGAs
- Verilog support only

Core Update Details

For detailed information on core updates in 2012.2, see Vivado IP Catalog.

ISE Design Suite 14.2

Device Support

- Production support for the following devices:
  - Kintex-7 325T
  - Kintex-7 410T
  - Virtex®-7 X485T
- Performance increase of ~3.5% for the -2 speed grades for Kintex-7 and Virtex-7 FPGAs
- Artix-7 FPGA family now supports bitstream generation
- Partial Reconfiguration support added for Zynq-7000 EPP devices

Partial Reconfiguration

- Per-frame CRC checks can be done on partial bitstreams (7 series)

PlanAhead Design Tool

- Clock Planner Fly Lines - the clock tree view for physical device resources now displays fly lines to help the user visualize physical connectivity in the device.

Pin Planner

- Export menu item from I/O ports view
- Improved handling of diff pairs creation
- Support buses with ascending, descending, and negative bit indexes
- Expand selection menu item in IO ports view
- Improved rendering focus on a cell in tables and trees
- Improved various views such as SSN report, IO port property editing, port rendering in package view, and clock resources view
- Improved DRC for VCCAUXIO, VCCAUXIOBT, VCCAUXIOSTD

System Generator for DSP

- MATLAB 2012a support
- Blockset Enhancements

- Floating Point Natural Log
- Floating/Fixed Point Abs
- Interleaver/De-interleaver 7.1

- Demos and Examples Updated to target Kintex-7 device

IP Core Details

GMII to RGMII

- Connects seamlessly to Zynq Gigabit Ethernet Controller

SMPTE SDI

- Support SD/HD/3G-SDI uncompressed serial digital video streams in the Xilinx 7 series FPGAs
- Verilog support only

Core Update Details

For detailed information on core updates in 14.2, see IP Core Generator Technology.

ISE Design Suite 14.1

Device Support

- Public access is now available for the following families:
  - Zynq™-7000 EPP (including bitstream generation)
  - Defense-grade 7 series FPGA and Zynq-7000 EPP
  - Automotive XA Zynq-7000 EPP
- Virtex®-7 XT FPGA family now supports bitstream generation.
- Artix™-7 FPGA GTPE2 support is now available, which includes:
  - SecureIP simulation models for all Xilinx-supported simulators.
  - 7 series FPGA GT Transceiver Wizard support.
- The following Artix-7 devices have been removed from the tools:
  - XC7A8
  - XC7A15

- XC7A30T
- XC7A50T

- ISE® Design Suite requires users to select all IO Standards and pin-placement in their designs prior to generating a bitstream. Please see the following Xilinx Answer Record for more information: http://www.xilinx.com/support/answers/41615.htm

PlanAhead Design Tool

More information on new features described in this chapter can be found in the *PlanAhead™ Design Tool User Guide*: www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_UserGuide.pdf

General

- The Flow Navigator now provides a more detailed view of the steps involved in the compilation flow. This includes the ability to easily collapse and expand the list of detailed tasks available within each design view (RTL Analysis, Synthesis, Implementation, and Program and Debug).
- The new clock resource view now displays connectivity of clocking and IO related resources using fly lines.
- Project settings now include more XPA options.

Pin Planning

- The PlanAhead design tool now provides the ability to convert pin-planning projects from an empty netlist project to a full RTL or netlist-based project. This allows you to migrate pin planning projects to more useful projects that manage more source types.
- Pin-planning support for Zynq-7000 EPP devices is now available.
- Pin-planning projects can now automatically infer differential pairs by recognizing one side of a differential standard and by providing the ability to automatically create the other side of the differential pair.
- There is an improved Simultaneous Switching Noise (SSN) reporting engine and improved 7 series FPGA noise prediction.
- There are improvements on the presentation of default IO standards.

Modelsim & Questa Advanced Simulator Integration

- The PlanAhead design tool now allows you to choose Modelsim or Questa® Advanced Simulator as the target simulator in the project settings. Simulation requires library compilation, which can be accomplished through Tcl command `compxlib`. The main advantage of this integration over ISE tools integration is the ability to have multiple simulation filesets with their own sets of properties. This allows you to simultaneously

create and maintain multiple simulation configurations that could vary depending on the testbench being used or other simulation properties.

Embedded Development Kit Integration

- The PlanAhead design tool can now create and add Xilinx Platform Studio (XPS) subsystems to a project through the `.xmp` source type. Double-clicking the `.xmp` source type launches Xilinx Platform Studio to generate and customize the embedded subsystem.
- Integration support also includes importing and converting ISE tools projects (`.xise`) that have `.xmp` sources embedded within them to PlanAhead design tool projects. The PlanAhead design tool manages generated files from XPS appropriately in the synthesis and implementation tool flows.

System Generator for DSP Integration

- PlanAhead design tool can now create and add DSP subsystems to a project through the `.sgp` source type. Double clicking the `.sgp` source type launches The MathWorks Simulink® to generate and customize the DSP subsystem.
- Integration support includes importing and converting ISE tools projects (`.xise`) that have `.sgp` sources embedded within them to PlanAhead design tool projects. PlanAhead design tool manages generated files from the DSP tools appropriately in the synthesis and implementation tool flows.

IP Repository

- PlanAhead design tool now allows the use of the IP repository without creating a design. You can create an empty project and open the IP repository for browsing, generating, and configuring an IP core. Generated sources, such as example designs, constraint files, data sheets, and more are now viewable in the project with a special IP Sources tab in the sources view.
- Initial support for the IEEE P1735 encryption standards.

Runs Infrastructure

- PlanAhead design tool can now force a run up-to-date if it has been marked stale and the user wishes to override the tool.
- Physical constraint updates do not cause the synthesis run state to go stale.
- There is a new "next step" option to run to intermediate states of the ISE tools (e.g. ngdbuild, map, par, trce).
- Bitgen options are now integrated with run options in project settings.

- There is now support for optional steps in the flow, as well as a mechanism to invoke Tcl "hook" scripts for use between stages of the run flow. You can specify a Tcl script that runs between compilation stages, you can use it for custom workarounds or reporting purposes.

Project Infrastructure

- Messages are now centralized to a common message manager, and should be visible in the messages tabs.
- PlanAhead design tool can now reset parameters and properties with the new Tcl commands `reset_param` and `reset_property`. These commands reset the value of the property and parameter to the built-in default, and if appropriate, to the specific target device.
- Certain invalid UCF messages are disabled for RTL elaboration.
- Improved falsely reported error and critical warning conditions when parsing UCF on RTL netlists.
- Improved include file support in RTL.

Embedded Design Tools

Embedded Design improvements in 14.1 are focused on 4 main areas:

- Zynq-7000 EPP support for bare-metal and Linux-based product development
- MicroBlaze™ processor updates
  - Performance improvements
  - New instructions for endianess conversion
  - Pre-integrated IO module
  - Multi-processor lock-step/result-voting for tamper & single event upset detection
  - Additional device support
- IP updates for improved system performance, configuration, and utility
- Tools updates for XPS and SDK

Zynq-7000 EPP Support

- 14.1 ISE WebPACK™ design tools now support Zynq-7000 EPP for the Xilinx Z7010, Z7020, Z7030 parts. Included in WebPACK design tools are the same tools as the Embedded Edition – XPS, SDK, MicroBlaze processor, and the full embedded IP library.
- XPS includes new configuration and MIO summary windows dedicated to Zynq-7000 EPP (see Embedded Tools below for further information).

- Zynq-7000 EPP documents are now available on the Xilinx website and also via the Xilinx Documentation Navigator tool which can be downloaded from http://www.xilinx.com/support.

MicroBlaze Processor Updates

New Low-latency interrupt mode

- The controller directly supplies the interrupt vector resulting in a reduction in latency response by as much as 10X depending on system design.

New Swap instructions

- New instructions for byte and halfword swapping help support endianness conversions between AXI big-endian and AXI little-endian.

Additional Device Support

- MicroBlaze processor has been validated across Xilinx 7 series FPGA families.

System Cache

- Embedded Edition adds a new embedded system cache IP peripheral between a MicroBlaze processor and external memory controller for AXI-based systems. MicroBlaze processor uses this System Cache IP core as Level 2 cache resulting in lower latency and faster performance depending on multiple system factors, design type, or connection points.

IO Module

- A new, configurable collection of general embedded processor peripherals packaged into a single IP block for connection to the MicroBlaze processor data-side LMB bus. This simplifies the definition, configuration and deployment of a standard Microcontroller system and enables MicroBlaze processor MCS designs to be moved seamlessly from Logic Edition into Embedded Edition.

Embedded IP Updates

14.1 includes IP core enhancements and additions focus on improved support for AXI, Zynq-7000 EPP, and MicroBlaze processor.

- AXI Quad SPI - Supports Execute In Place (XIP) mode and architectural improvements for performance. This IP core continues to work in Legacy mode as default option for existing customer.
- AXI Performance Monitor - Measures bus latency of a specific master/slave (AXI4/AXI4-Lite/AXI4-Stream) in a system, the amount of memory traffic for specific durations, and other performance metrics.

- Processing System7 - Wrapper IP for Zynq-7000 EPP, logic connection between PS and PL to assist with adding custom or other EDK IP.
- AXI System Cache - Level 2 Cache module for MicroBlaze processor when used in between MicroBlaze processor and external memory controller.
- Embedded IO Module - Common IO peripheral sub-set, introduced in MicroBlaze processor MCS, ported to Embedded Edition for compatibility.

Embedded Tools

In ISE Design Suite 14.1, the PlanAhead design tool now supports embedded design capture and management and is the recommended embedded design flow.

What's New in XPS?

In 14.1, XPS has been extended to provide Zynq-7000 EPP specific tools for configuration and first-stage bootloader generation with SDK.

- The new Zynq-7000 EPP Processing System provides developers with dozens of configuration options for memory, clocks, peripherals, DMA, IO, Interrupts and Flash memory interfaces. XPS now includes a new configuration window which enables users to graphically configure each parameter with guaranteed routing, voltage and clock-correct automated selections.
- 14.1 includes standard Zynq-7000 EPP configurations (for the ZC702 board), to enable developers to begin work immediately.
- The new Zynq-7000 EPP MIO summary window provides an aligned, color-coded graphic view of peripheral pin outs for faster, easier and guaranteed-correct MIO selection.

What's New in SDK?

- 14.1 now provides Xilinx SDK free of charge with all FlexLM license checks removed. SDK can be installed from a stand-alone installer (available on the Xilinx website) or within each ISE design tools edition installation.
- Full support for Zynq-7000 EPP
    - SDK now provides a full tools solution for bare-metal and Linux application development and profiling. Such tools include ARM GCC updated for bare-metal (EABI) and Linux development, Boot Image Creator, Flash programmer for QSPI, Device tree generator, and the remote system explorer (debug an IP-connected target board).
    - SDK works with XPS to build and generate design-specific firmware including the first stage boot loader with provision for device security, fallback boot, and bitstream management. It will also combine, build and deploy a complete bootable system image to the Zynq-7000 EPP target platform.

ChipScope Pro Tool and iMPACT

- Zynq-7000 EPP
  - Indirect Quad-SPI Flash programming support via iMPACT
  - ChipScope Pro tool device programming and debug support
  - iMPACT basic and advanced programming support
- Virtex-7 FPGA
  - IBERT 2-D Eye Scan enhancements
  - 7 series FPGA GTH support
  - ChipScope Pro tool device programming and debug support
  - iMPACT basic and advanced programming support
- Kintex-7 FPGA
  - IBERT 2-D Eye Scan enhancements
  - ChipScope Pro tool device programming and debug support
  - iMPACT basic and advanced programming support
- Artix-7 FPGA
  - Core generator tool and inserter support
- ChipScope Pro tool AXI Monitor now supports EDK and standard CORE Generator tool flows

System Generator for DSP

- Device support updated to include Defense-Grade 7 Series FPGA and Automotive XA Zynq-7000 EPP families
- PlanAhead design tool integration
  - Integrate System Generator modules in a larger RTL design
  - Includes tutorial
- New “Performance Tips” toolbar button which opens “High Performance Designs” documentation
- Blockset enhanced with FIFO support for embedded register in BRAM configuration

IBIS Simulation

- 7 series FPGA IBIS support is provided only through the PlanAhead design tool `write_ibis` command

- IBISWriter is not available for 7 series FPGA Families

Partial Reconfiguration

- Device support updated to include the XC7VX980T, XC7A200T, and XC7A350T.
  - Bitstream generation for Artix-7 devices is disabled in 14.1
- The list of resources that must remain static-only has been updated to include IO and configuration components.

Intellectual Property (IP)

Device Support

- Pre-production support has been added for the following families:
  - Defense-Grade Virtex-7Q FPGA
  - Defense-Grade Kintex-7Q FPGA
  - Defense-Grade Artix-7Q FPGA
  - XA Artix-7 FPGA
  - XA Zynq-7000 EPP

New IP Cores

- SMPTE 2022 5/6 Video over IP v1.0 - provides Transmitter and Receiver cores for broadcast applications that require bridging between Broadcast Connectivity standards (SD/HD/3G) and 10G networks.
- Ten Gigabit Ethernet 10GBASE-KR – 10G Ethernet PCS/PMA with optional Forward Error Correction (FEC) and Auto-Negotiation (AN) for 7 series FPGA GTX and GTH transceivers. Delivered as an optional, separately licensed configuration of the Ten Gigabit Ethernet PCS/PMA (10GBASE-R/KR) IP core.
- Asynchronous Sample Rate Converter for Digital Audio - converts stereo audio from one sample frequency to another. The input and output sample frequencies can be either an arbitrary fraction of each another, or the same frequency, but based on different clocks.
- Video In to AXI-4 Stream - converts common parallel clocked video signals to an AXI4-Stream interface. This enables connection of external video sources such as a DVI PHY to other video processing blocks that use the AXI4-Stream interface (for example Xilinx Video IP).
- AXI4-Stream to Video Out - converts AXI4-Stream interface signals to a standard parallel video output interface with timing signals. This enables connection of video

processing blocks that use the AXI4-Stream interface (for example Xilinx Video IP) to external video sinks such as DVI PHY.

- AXI4-Stream Interconnect - a key interconnect infrastructure IP that simplifies the process of connecting heterogenous master/slave AMBA® AXI4-Stream protocol compliant endpoint IP. The core routes connections from one or more AXI4-Stream master channels to one or more AXI4-Stream slave channels.
- AXI Performance Monitor - measures major performance metrics for the AMBA Advanced eXtensible Interface (AXI) system. Metrics supported include bus latency of a specific master/slave (AXI4/AXI4-Lite/AXI4-Stream) in a system, and the amount of memory traffic during specific periods of time.

Virtex-7 FPGA GTH Transceiver Support

- Pre-production Virtex-7 FPGA GTH support has been added to these IP Cores:
  - Ten Gigabit Ethernet 10GBASE-KR
  - 10GBASE-R
  - RXAUI
  - XAUI
  - QSGMII
  - 1000BASE-X/SGMII

Important Release Information

Vivado Design Suite 2012.2

This section contains detailed change information including improvements relative to the Vivado™ Design Suite Early Access 2012.1 release or ISE® Design Suite equivalent functionality.

Device Support

- Xilinx recommends all customers re-run implementation through timing analysis for all designs before generating bitstream in this version of the software.
- Support for the following General ES -2 speed grade devices require patches with this software release (see Xilinx® Answer Record 50886 at http://www.xilinx.com/support/answers/50886.htm).
  - Kintex™-7 325T, 480T, 420T and 410T
  - Virtex®-7 X485T and 2000T

Vivado Simulator

- ~2x memory usage reduction for elaborator over ISE tools
- ~50x speed up for Hierarchy Browser for large designs over Vivado Design Suite 2012.1
- Support for setting properties on simulation object
  - Properties added: **`array_display_limit`**, **`radiz`**, **`time_unit`**, **`trace_limit`**, **`line_tracing`**, **`process_tracing`**

Vivado High-Level Synthesis

- Vivado High-Level Synthesis (HLS) was previously named AutoESL and was invoked at the command line using **`autoesl`** but is now invoked using the command **`vivado_hls`**.
- The primary Tcl commands in the design flow have been changed:
  - The elaborate common is no longer required.

  - The new command **ccynth_design** replaces the elaborate and **autosyn** commands.
  - The new command **cosim_design** replaces the **autosim** command.
  - The new command **export_design** replaces the **autoimpl** command.
- The RTL implementation step in Vivado HLS has been depreciated (Tcl command **autoimpl**). This feature is now supported as the new RTL Export feature.
- The RTL co-simulation feature no longer requires a SystemC/HDL co-simulation license when using the supported third-party HDL simulators. Only the HDL license for supported third-party HDL simulators is required.
- The existing AP_STREAM macros have been deprecated. Streaming data is now supported by the new `hls::stream` data type.

Memory Interface Generator

All customers must re-generate their memory controller design with MIG 7 Series Version 1.6.

Pin Planner

- Improved handling of diff pairs creation
- Improved rendering focus on a cell in tables and trees
- Improved various views such as SSN report, IO port property editing, port rendering in package view, and clock resources view
- Improved DRC for VCCAUXIO, VCCAUXIOBT, VCCAUXIOSTD

System Generator for DSP

- Improvements to Vivado and System Generator for DSP Integration
  - Automatic regeneration based on mdl file time stamp changes
  - Vivado IP Generation for basic blocks improves generation times

Vivado Synthesis Tools

- System Verilog and VHDL language support enhancements

Vivado IP Catalog

Readme files included with IP provided through the Vivado IP Catalog and ISE CORE Generator™ tools have been updated to show a running history of new feature additions.

Updates to Existing IP

- 7 Series Transceiver Wizard
  - Added several new protocol templates
  - Added Virtex-7 2000T and HT (GTZ) device support
- Aurora 64B/66B
  - V7-GTH characterization updates
  - Hot plug detect support for the Xilinx 7 series FPGAs
  - Validation using KC724 board-to-board
- Aurora 8B/10B
  - Virtex-7 GTH device support
    - Super Logic Region (SLR) support
  - 16-bit additive scrambler/descrambler
  - 16-bit or 32-bit CRC for user data
  - Hot-plug detect support for the Xilinx 7 series FPGAs
  - Updated test bench
  - Validation using KC724 board-to-board
- ChipScope™ Pro IP Core
  - IBERT 7 Series GTH support for Virtex-7 FPGA devices
    - Analyzer support for RX Margin Analysis, including 2D Eye Scan measurement
  - IBERT 7 Series GTP support for Artix™-7 FPGA devices
    - CORE Generator tool support
    - Analyzer support for basic measurements
  - IBERT 7 Series GTZ support for Virtex-7 FPGA devices (Limited Access via Virtex-7 HT GTZ lounge only)
    - Analyzer support for basic measurements
- Clocking Wizard
  - Spread spectrum support added to version 4.2
  - Fast simulation support added to version 4.2
- Distributed Memory Generator v7.2
  - Example test bench support added
- PCI EXPRESS® Gen3/Gen2

- IP support
- 10 Gigabit Ethernet MAC
  - Added Artix device support
- 1000BASE-X/SGMII
  - Added Artix device support
  - Added SGMII over LVDS sync support for Virtex-7 and Kintex-7 families
- QSGMII
  - Added Artix device support
- PCI32 and PCI64
  - Added Vivado Design Suite 2012.2 support

Additional IP Supporting AXI4 Interfaces

- The latest versions of CORE Generator IP have been updated with Production AXI4 interface support. For more detailed AXI IP support information see http://www.xilinx.com/ipcenter/axi4_ip.htm.
- In general, the AXI4 interface is supported by the latest version of an IP, for Virtex-7, Kintex-7, Virtex-6 and Spartan®-6 devices families. Older "Production" versions of IP continue to support the legacy interface for the respective core on Virtex-6, Spartan-6, Virtex-5, Virtex-4 and Spartan-3 devices families only.
- For general information on AXI4 support, see http://www.xilinx.com/ipcenter/axi4.htm.
- A comprehensive listing of cores that have been updated in the 2012.2 release can be viewed at www.xilinx.com/ipcenter/coregen/updates_14_2.htm.

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Device Support

- Designs targeting the following devices must be re-implemented (place and route) in this release of the software:
  - All Artix-7 devices
  - Zynq™-7000 EPP 7z030 and 7z045
- Xilinx recommends all customers re-run implementation through timing analysis for all designs before generating bitstream in this version of the software.