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Spartan-3 for PCI Express

Starter Kit Board User Guide v1.3

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
5/08/06	1.1	Initial Xilinx release
7/21/06	1.2	Minor Editorial Updates
5/23/07	1.3	Updated file names to conform to PCI-SIG guidelines for trademarks.

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About This Guide

This Spartan™-3 Starter Board Kit for PCI Express User Guide provides basic information about the capabilities, functions, and design of the Xilinx Spartan-3 PCI Express Starter Kit Board. It includes general information for using the various peripheral functions included on the board. For detailed reference designs, including VHDL or Verilog source code, please visit the Spartan-3 Starter Board for PCI Express product page.

Acknowledgements

Xilinx wishes to thank the following companies for their support of the Spartan-3 Starter Kit board for PCI Express:

- Avnet Electronics
- Philips Semiconductors for the PCI Express x1 lane PHY
- Micron Technology, Inc. for the 32M x 16 DDR SDRAM
- STMicroelectronics for the 4M x 1 SPI serial EEPROM
- Texas Instruments Incorporated for the various power supply solutions

Contents

This guide contains the following chapters:

- Preface, "About this Guide" introduces the organization and purpose of this guide, a list of additional resources, and the conventions used in this document.
- Chapter 1, "Introduction" describes the Starter Kit Board, and provides information about its key components and features. This chapter also provides information about additional resources, recommended design experience, providing feedback, and securing technical support.
- Chapter 2, "PCI Express Interface" provides detailed information about the interface for PCI-Express (PCIe) two-chip solution consisting of the Xilinx Spartan-3 FPGA and the Philips PX1011A-EL1 PCI Express PHY (PX1011A).
- Chapter 3, "EXP Expansion Connectors" describes expansion capabilities for customized user application daughter cards and interfaces over two EXP expansion connectors.
- Chapter 4, "Clock Sources" details the Spartan-3 FPGA global clock input pins that can be used for high-performance, low-skew clocking.
- Chapter 5, "Switches and Buttons" describes the operation, connection, and example constraints for use-defined switches and buttons.

- Chapter 6, "LEDs" details the overview, operation, and connections of the eight user LEDs.
- Chapter 7, "VGA Display Port" describes the video display port that is available through an on-board Philips TDA8777 Triple DAC.
- Chapter 8, "RS-232 PORT" describes the DCE compatible RS-232 serial port for connection to most computer serial ports.
- Chapter 9, "DDR SDRAM" provides information about the two 512 MB (32M x 16) Micron Technology DDR SDRAM (MT46V32M16) that provide a 32-bit data interface to the Spartan-3 FPGA.
- Chapter 10, "SPI Serial Flash" details the STMcroelectronics M25P40 4Mb SPI serial flash and its possible uses.
- Chapter 11, "FPGA Configuration" describes the two supported FPGA configuration options.
- Chapter 12, "Power Supplies" describes the power supplies for all components on the board, as well as the EXP expansion connectors.
- Appendix A, "Example User Constraints File (UCF)" contains the contents of the MASTER Constraints File for the starter board.
- Appendix B, "Schematics" contains comprehensive and detailed schematic maps.

Additional Resources

For additional information and resources, see www.xilinx.com/support. To go directly to a specific area of the support site, click a link in the table below.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging www.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records www.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Application+Notes
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging www.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues www.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment www.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, signal names, and program files	`speed grade: - 100`
`Courier bold`	Literal commands you enter in a syntactical statement	**`ngdbuild`** `design_name`
Italics	Variables in a syntax statement for which you must supply values	See the *Development System Reference Guide* for more information.
	References to other manuals	See the *User Guide* for details.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Shading	Unsupported or reserved items	This feature is not supported
Square brackets [ ]	Optional entry or parameter, with the exception of bus specifications. For bus specifications, brackets are required, for example **`bus[7:0]`**.	**`ngdbuild`** `[option_name] design_name`
Braces { }	A list of items from which you must choose one or more	**`lowpwr ={on|off}`**
Vertical bar |	Separates items in a list of choices	**`lowpwr ={on|off}`**

Vertical ellipsis
.
.
.
	Omitted repetitive material	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Omitted repetitive material	**`allow block`** `block_name loc1 loc2 ... locn;`
Notations	The prefix '0x' or the suffix 'h' indicate hexadecimal notation	A read of address `0x00112975` returns `45524943h`
	An '_n' means the signal is active low	`usr_teof_n` is active low

Online Document

The following conventions are used in this document for cross-references and links to URLs.

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See "Additional Resources" for more information. See "Title Formats" in Chapter 1 for detailed information.
Blue, underlined text	Hyperlink to a website (URL)	Go to www.xilinx.com for the latest speed files.

Chapter 1

Introduction

The Xilinx Spartan-3 Starter Kit Board for PCI-Express provides everything you need to build a low-cost Spartan-3-based PCI Express application. To help you understand the full functionality and features of this board kit, the LogiCORE™ evaluation core for PCI-Express can be downloaded and installed at no extra cost. This IP core has been tested and defined to work with the board kit, and is an integral part of the coprehensive solution.

Key Components and Features

The key features of the Spartan-3 PCI Express Kit board are listed below:

- Xilinx XC3S1000 Spartan-3 FPGA
  - Up to 391 user I/O pins
  - 676-pin FBGA package
  - Over 17,000 logic cells
- Xilinx 8 Mbit Platform Flash configuration PROM
- Philips 2.5 Gbps, PCI Express single lane PHY
- EXP compatible expansion connectors
  - 168 User I/O
  - Full and half card support
  - 2.5V and 3.3V
  - 2 global clock inputs
- 128 Mbyte (512 Mbit x 2) of DDR SDRAM, x32 data interface, 100+ MHz
- VGA display port
- 9-pin RS-232 serial port
- 4 Mbits of SPI serial flash memory with data and code storage
- 25.175 MHz clock oscillator
- 50 MHz clock oscillator
- 8-pin DIP socket for auxiliary clock input
- Eight discrete LEDs
- Three push button switches
- Four position DIP switch

Figure 1-1 illustrates the block diagram of the board functions.

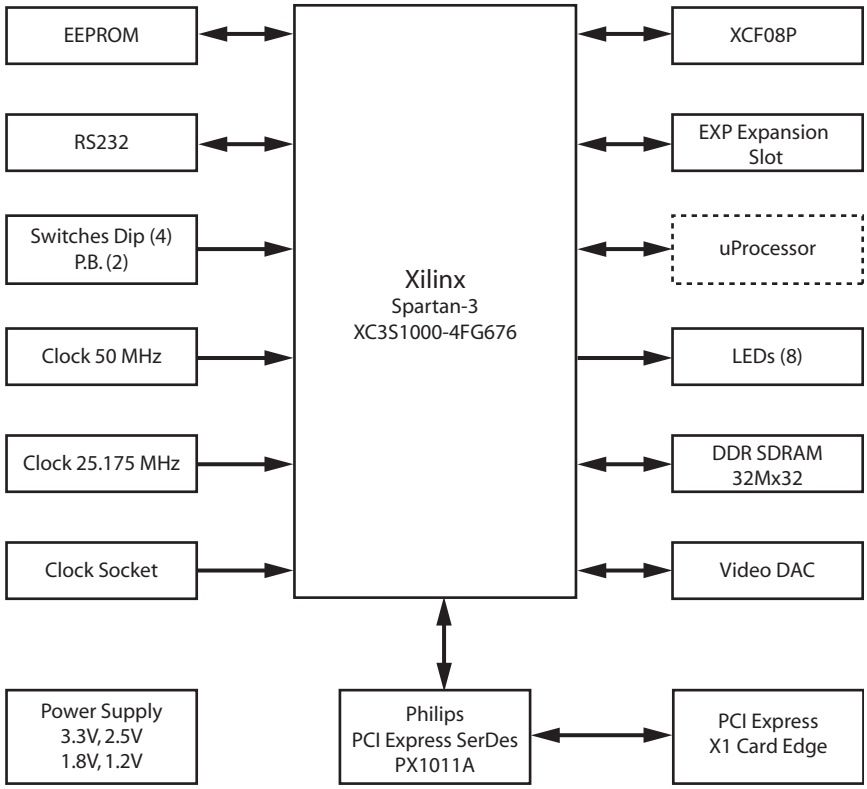

Figure 1-1: **Spartan-3 Starter Kit Board for PCI Express Block Diagram**

Figure 1-2 shows a detailed diagram of the board connectors, jumpers, and main functional blocks.

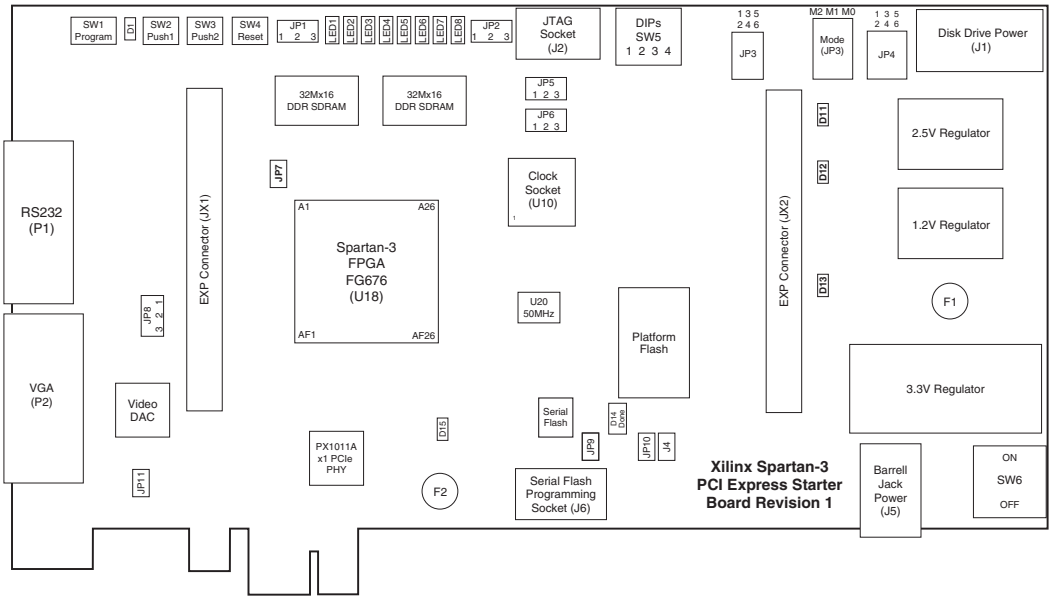

Figure 1-2: **Spartan-3 Starter Kit Board for PCI Express Functional Diagram**

The Evaluation Core for PCI Express

The instructions for downloading the evaluation core are included in the Spartan-3 Starter Kit Board for PCI-Express hardware packaging.

Additional Core Resources

For additional information and documentation for the LogiCORE Endpoint for PCI Express core, go to the product page at www.xilinx.com/pciexpress.

Technical Support

For technical support, go to www.xilinx.com/support. Questions are routed to a team with expertise using the LogiCORE Endpoint for PCI Express core.

Xilinx will provide technical support for use of this product as described in the LogiCORE Endpoint for PCI Express User Guide and the LogiCORE Endpoint for PCI Express Getting Started Guide. Xilinx cannot guarantee timing, functionality, or support of this product for designs that do not follow these guidelines.

Document

For comments or suggestions about the documentation, please submit a WebCase from www.xilinx.com/support/clearexpress/websupport.htm. Be sure to include the following information:

- Document title
- Document number
- Page number(s) to which your comments refer
- Explanation of your comments

Chapter 2

PCI Express Interface

Overview

The Spartan-3 Starter Kit Board for PCI-Express provides an PCI-Express (PCIe) interface using a two-chip solution consisting of the Xilinx Spartan-3 FPGA and the Philips PX1011A-EL1 PCI Express PHY (PX1011A). The PX1011A is a high-performance, low-power PCI Express electrical Physical layer (PHY) that handles the low level PCI Express protocol and signaling. The Spartan-3 FPGA is configured to include a PCIe PIPE (PHY Interface for PCI Express) endpoint core that interfaces to the external PX1011A, and provides the MAC layer function for the PCIe interface.

The PX1011A PHY includes features such as data serialization and de-serialization, 8b/10b encoding, analog buffers, elastic buffer and receiver detection, which provides superior performance to the media access control (MAC) layer in the FPGA. The PX1011A is a 2.5 Gb/sec. PCI Express PHY with 8-bit data PXPIPE interface. Its PXPIPE interface is a superset of the PHY Interface for the PCI Express (PIPE) specification, enhanced and adapted for off-chip applications. It contains a source synchronous clock for transmit and receive data. The 8-bit data interface operates at 250 MHz with SSTL_2 signaling. The SSTL_2 signaling is compatible with the I/O interfaces available in the Xilinx Spartan-3 FPGA.

Figure 2-1 shows a simple block diagram of the FPGA and PHY implementation.

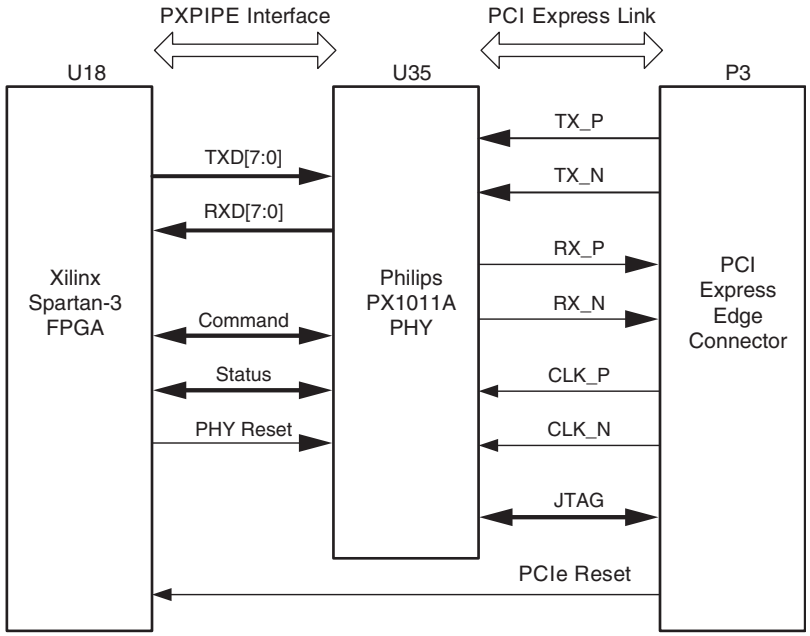

Figure 2-1: **Spartan-3 FPGA and PX1011A PHY Connections**

Operation

The PX1011A-EL1 PCI Express PHY consists of the physical coding sub-layer (PCS), a Serializer and De-serializer (SerDes) and a set of I/Os (pads). The PCI Express PHY handles the low level PCI Express protocol and signaling. The PX1011A interface between the MAC and PHY is a superset of the PIPE specification, with the addition of source synchronous clocks for RX and TX data to simplify timing closure. The digital interface between the FPGA-based MAC and the PHY is also referred to as PXPIPE interface. It consists of 8-bit input and output words, each with control signals and source synchronous clocks. The data rate across the PXPIPE is 250 MB per second in both directions.

The PCI Express link consists of a differential input and differential output pair. The data rate of these signals is 2.5 Gb per second.

The PIPE receive (RXD) and transmit (TXD) signals must be properly terminated SSTL2-I signals at both the driving device and the receiving device. PCB signal routing for these signals are length matched to minimize skew.

Connections

The following shows the user constraints file (UCF) location constraints for the PX1011A PCI Express PHY interface.

```
# System reset signal from the PCIe interface to the FPGA
NET "sys_reset_n"         LOC = "AE4"  | IOSTANDARD = LVCMOS25 | IOBDELAY = NONE ;

# Receive Input Signals
NET "rxclk"               LOC = "AE13" | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "phystatus"           LOC = "AF12" | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxvalid"             LOC = "AD12" | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxstatus<2>"         LOC = "AC11" | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxstatus<1>"         LOC = "AD10" | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxstatus<0>"         LOC = "AC10" | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdatak<0>"          LOC = "AF8"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<0>"           LOC = "AE8"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<1>"           LOC = "AC7"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<2>"           LOC = "AF6"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<3>"           LOC = "AE6"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<4>"           LOC = "AD6"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<5>"           LOC = "AC6"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<6>"           LOC = "AE5"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxdata<7>"           LOC = "AD5"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;
NET "rxelecidle"          LOC = "AF4"  | IOSTANDARD = SSTL2_I | IOBDELAY = NONE ;

# Transmit Output Signals
NET "resetn"              LOC = "AF24" | IOSTANDARD = SSTL2_I ;
NET "rxpolarity"          LOC = "AE24" | IOSTANDARD = SSTL2_I ;
NET "txelecidle"          LOC = "AF23" | IOSTANDARD = SSTL2_I ;
NET "txcompliance"        LOC = "AE23" | IOSTANDARD = SSTL2_I ;
NET "powerdown<1>"        LOC = "AD23" | IOSTANDARD = SSTL2_I ;
NET "powerdown<0>"        LOC = "AF22" | IOSTANDARD = SSTL2_I ;
NET "txdatak<0>"          LOC = "AE22" | IOSTANDARD = SSTL2_I ;
NET "txdetectrx_loopback" LOC = "AF21" | IOSTANDARD = SSTL2_I ;
NET "txclk"               LOC = "AE21" | IOSTANDARD = SSTL2_I ;
NET "txdata<7>"           LOC = "AD21" | IOSTANDARD = SSTL2_I ;
NET "txdata<6>"           LOC = "AF20" | IOSTANDARD = SSTL2_I ;
NET "txdata<5>"           LOC = "AE20" | IOSTANDARD = SSTL2_I ;
NET "txdata<4>"           LOC = "AF19" | IOSTANDARD = SSTL2_I ;
NET "txdata<3>"           LOC = "AE19" | IOSTANDARD = SSTL2_I ;
NET "txdata<2>"           LOC = "AF15" | IOSTANDARD = SSTL2_I ;
NET "txdata<1>"           LOC = "AE15" | IOSTANDARD = SSTL2_I ;
NET "txdata<0>"           LOC = "AD15" | IOSTANDARD = SSTL2_I ;
```

Related Resources

For more information about the Xilinx LogiCORE Endpoint for PCI Express PIPE, see the *Xilinx LogiCORE Endpoint 1-Lane for PCI Express PIPE User Guide*.

For information about the Philips PCI Express PHY see the Philips PX1011A-EL1 PCI Express PHY data sheet.

Chapter 3

EXP Expansion Connectors

Overview

The Spartan-3 Starter Kit Board for PCI-Express provides expansion capabilities for customized user application daughter cards and interfaces over two EXP expansion connectors. The EXP expansion connectors on the PCI Express board can support two half-card EXP modules, or a single dual slot EXP module. Both off-the-shelf EXP modules and user-developed modules can easily be plugged onto the Spartan-3 Starter Kit Board for PCI-Expressto add features and functions to the backend application of the main board.

Operation

The EXP specification defines a 132-pin connector, with 24 power, 24 grounds, and 84 user I/Os. The standard EXP configuration implemented on the Spartan-3 Board for PCI Express uses two connectors (Samtec part number QTE-060-09-F-D-A) in a dual slot EXP configuration, for a total of 168 user I/Os. Using a jumper, you can set the voltage levels for the EXP user I/O to either 2.5V or 3.3V. JP5 sets the I/O voltage for both the JX1 and JX2 EXP connectors by setting the VCCO voltage for the 4 banks of the FPGA that connect to the EXP I/O. Figure 3-1 shows the JP5 settings.

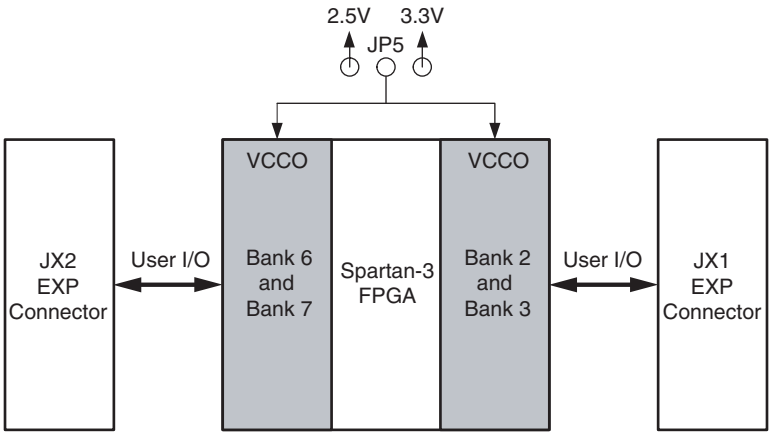

Figure 3-1: **EXP User I/O Voltage Settings**

The EXP specification defines four user signal types: Single Ended I/O, Differential I/O, Differential and Single Ended Clock Inputs, and Differential and Single Ended Clock

Outputs. Table 3-1 shows a summary of the signal categories for the standard, dual format EXP slot.

Table 3-1: **EXP User I/O Types**

Signal Category	Pins per Connector	Pins per Dual EXP Slot
Single-ended I/O	34	68
Single-ended clocks	2	4
Differential I/O pairs	22	44
Differential clock input pair	1	2
Differential clock output pair	1	2
2.5V pins (333 mA per pin)	12	24
3.3V pins (333 mA per pin)	12	24
Grounds	24	48
Total	108	216

Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the EXP specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the baseboard and EXP module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require single-ended signals only can use each differential pair as two single-ended signals, for a total of 78 single-ended I/O per connector (156 total in the dual slot configuration).

Connections

The Spartan-3 FPGA user I/O pins connect to the two EXP connectors, JX1 and JX2, as shown in the example UCF figures below. The JX1 and JX2 connectors are Samtec QTE-060-09-F-D-A high performance plugs that mate to Samtec QSE-060-01-F-D-A high-performance receptacles, located on the daughter card. Samtec also provides several high-performance ribbon cables that will mate to the JX1 and JX2 connectors.

UCF Location Constraints for the EXP Connectors JX1

```
Net JX1_SE_IO_0        LOC = M3   ; # B6GIO_0
Net JX1_SE_IO_1        LOC = J7   ; # B7GIO_0
Net JX1_SE_IO_2        LOC = M7   ; # B6GIO_1
Net JX1_SE_IO_3        LOC = J6   ; # B7GIO_1
Net JX1_SE_IO_4        LOC = N7   ; # B6GIO_2
Net JX1_SE_IO_5        LOC = H5   ; # B7GIO_2
Net JX1_SE_IO_6        LOC = M8   ; # B6GIO_3
Net JX1_SE_IO_7        LOC = H2   ; # B7GIO_3
Net JX1_SE_IO_8        LOC = N8   ; # B6GIO_4
Net JX1_SE_IO_9        LOC = J5   ; # B7GIO_4
Net JX1_SE_IO_10       LOC = P8   ; # B6GIO_5
Net JX1_SE_IO_11       LOC = J4   ; # B7GIO_5
Net JX1_SE_IO_12       LOC = P2   ; # B6GIO_6
```

```
Net JX1_SE_IO_13        LOC = K7   ; # B7GIO_6
Net JX1_SE_IO_14        LOC = P7   ; # B6GIO_7
Net JX1_SE_IO_15        LOC = K5   ; # B7GIO_7
Net JX1_SE_IO_16        LOC = R1   ; # B6GIO_8
Net JX1_SE_IO_17        LOC = L8   ; # B7GIO_8
Net JX1_SE_IO_18        LOC = P1   ; # B6GIO_9
Net JX1_SE_IO_19        LOC = L7   ; # B7GIO_9
Net JX1_SE_IO_20        LOC = R2   ; # B6GIO_10
Net JX1_SE_IO_21        LOC = H1   ; # B7GIO_10
Net JX1_SE_IO_22        LOC = R3   ; # B6GIO_11
Net JX1_SE_IO_23        LOC = L1   ; # B7GIO_11
Net JX1_SE_IO_24        LOC = T1   ; # B6GIO_12
Net JX1_SE_IO_25        LOC = L2   ; # B7GIO_12
Net JX1_SE_IO_26        LOC = T2   ; # B6GIO_13
Net JX1_SE_IO_27        LOC = L4   ; # B7GIO_13
Net JX1_SE_IO_28        LOC = V6   ; # B7GIO_14
Net JX1_SE_IO_29        LOC = U7   ; # B7GIO_15
Net JX1_SE_IO_30        LOC = W5   ; # B6GIO_14
Net JX1_SE_IO_31        LOC = V7   ; # B6GIO_15
Net JX1_SE_IO_32        LOC = R8   ; # B7GIO_17
Net JX1_SE_IO_33        LOC = R7   ; # B7GIO_18

Net JX1_SE_CLK_IN       LOC = B13  ; # B0_GCLK7
Net JX1_SE_CLK_OUT      LOC = T4   ; # B7GIO_16

Net JX1_DIFF_N_0        LOC = AB4 ;  # B6GPIOn_0
Net JX1_DIFF_N_1        LOC = W7  ;  # B7GPIOn_0
Net JX1_DIFF_N_2        LOC = AC2 ;  # B6GPIOn_1
Net JX1_DIFF_N_3        LOC = V5  ;  # B7GPIOn_1
Net JX1_DIFF_N_4        LOC = W4  ;  # B6GPIOn_2
Net JX1_DIFF_N_5        LOC = T8  ;  # B7GPIOn_2
Net JX1_DIFF_N_6        LOC = W2  ;  # B6GPIOn_3
Net JX1_DIFF_N_7        LOC = R6  ;  # B7GPIOn_3
Net JX1_DIFF_N_8        LOC = U4  ;  # B6GPIOn_4
Net JX1_DIFF_N_9        LOC = P6  ;  # B7GPIOn_4
Net JX1_DIFF_N_10       LOC = U2  ;  # B6GPIOn_5
Net JX1_DIFF_N_11       LOC = M6  ;  # B7GPIOn_5
Net JX1_DIFF_N_12       LOC = P4  ;  # B6GPIOn_6
Net JX1_DIFF_N_13       LOC = N3  ;  # B7GPIOn_6
Net JX1_DIFF_N_14       LOC = N1  ;  # B6GPIOn_7
Net JX1_DIFF_N_15       LOC = L5  ;  # B7GPIOn_7
Net JX1_DIFF_N_16       LOC = K1  ;  # B6GPIOn_9
Net JX1_DIFF_N_17       LOC = J2  ;  # B7GPIOn_8
Net JX1_DIFF_N_18       LOC = K3  ;  # B6GPIOn_10
Net JX1_DIFF_N_19       LOC = H3  ;  # B7GPIOn_9
Net JX1_DIFF_N_20       LOC = G1  ;  # B6GPIOn_11
Net JX1_DIFF_N_21       LOC = E3  ;  # B7GPIOn_10

Net JX1_DIFF_P_0        LOC = AB3 ;  # B6GPIOp_0
Net JX1_DIFF_P_1        LOC = W6  ;  # B7GPIOp_0
Net JX1_DIFF_P_2        LOC = AC1 ;  # B6GPIOp_1
Net JX1_DIFF_P_3        LOC = V4  ;  # B7GPIOp_1
Net JX1_DIFF_P_4        LOC = W3  ;  # B6GPIOp_2
Net JX1_DIFF_P_5        LOC = T7  ;  # B7GPIOp_2
Net JX1_DIFF_P_6        LOC = W1  ;  # B6GPIOp_3
Net JX1_DIFF_P_7        LOC = R5  ;  # B7GPIOp_3
Net JX1_DIFF_P_8        LOC = U3  ;  # B6GPIOp_4
Net JX1_DIFF_P_9        LOC = P5  ;  # B7GPIOp_4
Net JX1_DIFF_P_10       LOC = U1  ;  # B6GPIOp_5
```

```
Net JX1_DIFF_P_11       LOC = M5  ;  # B7GPIOp_5
Net JX1_DIFF_P_12       LOC = P3  ;  # B6GPIOp_6
Net JX1_DIFF_P_13       LOC = N4  ;  # B7GPIOp_6
Net JX1_DIFF_P_14       LOC = N2  ;  # B6GPIOp_7
Net JX1_DIFF_P_15       LOC = L6  ;  # B7GPIOp_7
Net JX1_DIFF_P_16       LOC = K2  ;  # B6GPIOp_9
Net JX1_DIFF_P_17       LOC = J3  ;  # B7GPIOp_8
Net JX1_DIFF_P_18       LOC = K4  ;  # B6GPIOp_10
Net JX1_DIFF_P_19       LOC = H4  ;  # B7GPIOp_9
Net JX1_DIFF_P_20       LOC = G2  ;  # B6GPIOp_11
Net JX1_DIFF_P_21       LOC = E4  ;  # B7GPIOp_10

Net JX1_DIFF_CLK_P_IN   LOC = D2  ;  # B6GPIOp_12
Net JX1_DIFF_CLK_N_IN   LOC = D1  ;  # B6GPIOn_12

Net JX1_DIFF_CLK_P_OUT LOC = M2  ;  # B6GPIOp_8
Net JX1_DIFF_CLK_N_OUT LOC = M1  ;  # B6GPIOn_8
```

UCF Location Constraints for the EXP Connectors JX2

```
Net JX2_SE_IO_0         LOC = M19  ; # B2GIO_0
Net JX2_SE_IO_1         LOC = P20  ; # B3GIO_0
Net JX2_SE_IO_2         LOC = M20  ; # B2GIO_1
Net JX2_SE_IO_3         LOC = T20  ; # B3GIO_1
Net JX2_SE_IO_4         LOC = K20  ; # B2GIO_2
Net JX2_SE_IO_5         LOC = P21  ; # B3GIO_2
Net JX2_SE_IO_6         LOC = J20  ; # B2GIO_3
Net JX2_SE_IO_7         LOC = R21  ; # B3GIO_3
Net JX2_SE_IO_8         LOC = H20  ; # B2GIO_4
Net JX2_SE_IO_9         LOC = P24  ; # B3GIO_4
Net JX2_SE_IO_10        LOC = J21  ; # B2GIO_5
Net JX2_SE_IO_11        LOC = P22  ; # B3GIO_5
Net JX2_SE_IO_12        LOC = H21  ; # B2GIO_6
Net JX2_SE_IO_13        LOC = R24  ; # B3GIO_6
Net JX2_SE_IO_14        LOC = H22  ; # B2GIO_7
Net JX2_SE_IO_15        LOC = R22  ; # B3GIO_7
Net JX2_SE_IO_16        LOC = J22  ; # B2GIO_8
Net JX2_SE_IO_17        LOC = T23  ; # B3GIO_8
Net JX2_SE_IO_18        LOC = J23  ; # B2GIO_9
Net JX2_SE_IO_19        LOC = T22  ; # B3GIO_9
Net JX2_SE_IO_20        LOC = L23  ; # B2GIO_10
Net JX2_SE_IO_21        LOC = U22  ; # B3GIO_10
Net JX2_SE_IO_22        LOC = M24  ; # B2GIO_11
Net JX2_SE_IO_23        LOC = T21  ; # B3GIO_11
Net JX2_SE_IO_24        LOC = T19  ; # B2GIO_12
Net JX2_SE_IO_25        LOC = V23  ; # B3GIO_12
Net JX2_SE_IO_26        LOC = N20  ; # B2GIO_13
Net JX2_SE_IO_27        LOC = V22  ; # B3GIO_13
Net JX2_SE_IO_28        LOC = W22  ; # B3GIO_14
Net JX2_SE_IO_29        LOC = U20  ; # B3GIO_16
Net JX2_SE_IO_30        LOC = AC26 ; # B2GIO_14
Net JX2_SE_IO_31        LOC = K21  ; # B2GIO_15
Net JX2_SE_IO_32        LOC = U21  ; # B3GIO_17
Net JX2_SE_IO_33        LOC = V20  ; # B3GIO_18

Net JX2_SE_CLK_IN       LOC = AE14 ; # B4_GCLK1
Net JX2_SE_CLK_OUT      LOC = V21  ; # B3GIO_15

Net JX2_DIFF_N_0        LOC = AB24 ; # B2GPIOn_0
```

```
Net JX2_DIFF_N_1        LOC = W26  ; # B3GPIOn_0
Net JX2_DIFF_N_2        LOC = Y26  ; # B2GPIOn_1
Net JX2_DIFF_N_3        LOC = U24  ; # B3GPIOn_1
Net JX2_DIFF_N_4        LOC = W24  ; # B2GPIOn_2
Net JX2_DIFF_N_5        LOC = N23  ; # B3GPIOn_2
Net JX2_DIFF_N_6        LOC = V25  ; # B2GPIOn_3
Net JX2_DIFF_N_7        LOC = N25  ; # B3GPIOn_3
Net JX2_DIFF_N_8        LOC = U26  ; # B2GPIOn_4
Net JX2_DIFF_N_9        LOC = M25  ; # B3GPIOn_4
Net JX2_DIFF_N_10       LOC = T26  ; # B2GPIOn_5
Net JX2_DIFF_N_11       LOC = L25  ; # B3GPIOn_5
Net JX2_DIFF_N_12       LOC = R26  ; # B2GPIOn_6
Net JX2_DIFF_N_13       LOC = K25  ; # B3GPIOn_6
Net JX2_DIFF_N_14       LOC = P26  ; # B2GPIOn_7
Net JX2_DIFF_N_15       LOC = J24  ; # B3GPIOn_7
Net JX2_DIFF_N_16       LOC = L19  ; # B2GPIOn_9
Net JX2_DIFF_N_17       LOC = H25  ; # B3GPIOn_8
Net JX2_DIFF_N_18       LOC = L21  ; # B2GPIOn_10
Net JX2_DIFF_N_19       LOC = E23  ; # B3GPIOn_9
Net JX2_DIFF_N_20       LOC = K23  ; # B2GPIOn_11
Net JX2_DIFF_N_21       LOC = D25  ; # B3GPIOn_10

Net JX2_DIFF_P_0        LOC = AB23 ; # B2GPIOp_0
Net JX2_DIFF_P_1        LOC = W25  ; # B3GPIOp_0
Net JX2_DIFF_P_2        LOC = Y25  ; # B2GPIOp_1
Net JX2_DIFF_P_3        LOC = U23  ; # B3GPIOp_1
Net JX2_DIFF_P_4        LOC = W23  ; # B2GPIOp_2
Net JX2_DIFF_P_5        LOC = N24  ; # B3GPIOp_2
Net JX2_DIFF_P_6        LOC = V24  ; # B2GPIOp_3
Net JX2_DIFF_P_7        LOC = N26  ; # B3GPIOp_3
Net JX2_DIFF_P_8        LOC = U25  ; # B2GPIOp_4
Net JX2_DIFF_P_9        LOC = M26  ; # B3GPIOp_4
Net JX2_DIFF_P_10       LOC = T25  ; # B2GPIOp_5
Net JX2_DIFF_P_11       LOC = L26  ; # B3GPIOp_5
Net JX2_DIFF_P_12       LOC = R25  ; # B2GPIOp_6
Net JX2_DIFF_P_13       LOC = K26  ; # B3GPIOp_6
Net JX2_DIFF_P_14       LOC = P25  ; # B2GPIOp_7
Net JX2_DIFF_P_15       LOC = J25  ; # B3GPIOp_7
Net JX2_DIFF_P_16       LOC = L20  ; # B2GPIOp_9
Net JX2_DIFF_P_17       LOC = H26  ; # B3GPIOp_8
Net JX2_DIFF_P_18       LOC = L22  ; # B2GPIOp_10
Net JX2_DIFF_P_19       LOC = E24  ; # B3GPIOp_9
Net JX2_DIFF_P_20       LOC = K24  ; # B2GPIOp_11
Net JX2_DIFF_P_21       LOC = D26  ; # B3GPIOp_10

Net JX2_DIFF_CLK_P_IN   LOC = H24  ; # B2GPIOp_12
Net JX2_DIFF_CLK_N_IN   LOC = H23  ; # B2GPIOn_12

Net JX2_DIFF_CLK_P_OUT LOC = N22  ; # B2GPIOp_8
Net JX2_DIFF_CLK_N_OUT LOC = N21  ; # B2GPIOn_8
```

Chapter 4

Clock Sources

Overview

The Spartan-3 FPGA has eight global clock input pins that can be used for high-performance, low-skew clocking. All of these clock pins are used on the Spartan-3 Board for PCI Express and are defined in this chapter.

Operation

Table 4-1 shows the eight clock inputs to the Spartan-3 FPGA. Six of the eight clocks are buffered to avoid voltage compatibility issues that could result from the adjustable voltage bank settings.

Table 4-1: **Global Clock Inputs**

Function	Clock Input	FPGA Pin	Global Clock Buffer
25.175 MHz Video Clock	VIDEO_CLK	AF14	GCLK0
JX2 Clock Input	JX2_SE_CLK_IN	AE14	GCLK1
DDR Clock Feedback	DDR_CLK_FB_IN	AD13	GCLK2
PCIe RX Clock	RXCLK	AE13	GCLK3
User Clock - SMT	CLK_SMT	C14	GCLK4
User Clock - Socket	CLK_SOCKET	B14	GCLK5
50 MHz Clock	CLK_50MHZ	A13	GCLK6
JX1 Clock Input	JX1_SE_CLK_IN	B13	GCLK7

Two user clock options are available through the user clock socket (U10) and the un-populated SMT layout at U26. Both of these locations can accept a user supplied, 3.3V compatible clock oscillator device.

Connections

UCF Example Constraints for Global Clock Inputs

```
Net CLK_50MHZ          LOC = A13   | IOSTANDARD = LVCMOS25; # U20 - 50MHz OSC
```