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Spartan-3A DSP Starter Platform User Guide

UG454 (v1.1) January 30, 2009

XILINX ®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/3/07	1.0	Initial Xilinx release.
1/30/09	1.1	Updated to v1.1.

Table of Contents

Spartan-3A DSP 1800A Board Features

Overview

The purpose of this manual is to describe the functionality and contents of the Spartan®-3A DSP Starter Platform from Xilinx. This document includes instructions for operating the board and descriptions of the hardware features.

For more information about this product, reference designs, and additional documentation, please visit the product home page found at www.xilinx.com/s3adspstarter or www.xilinx.com/s3adspmb or www.xilinx.com/s3adsp_sk.

Design Description

The Spartan-3A Starter Platform provides a platform for engineers designing with the Xilinx Spartan-3A DSP FPGA. The board provides the hardware to not only evaluate the advanced features of the Spartan-3A DSP, but also to implement complete user applications using peripherals on the Spartan-3A DSP Starter Platform and EXP modules, or both, plugged into EXP expansion connectors on the Spartan-3A DSP Starter Platform.

Features

The Spartan-3A DSP Starter Platform provides the following features:

- Xilinx 3SD1800A-FG676 FPGA
- Clocks
    - 125 MHz LVTTL SMT oscillator
    - LVTTL oscillator socket
    - 25.175 MHz LVTTL SMT oscillator (video clock)
- Memory
    - 32M x 32 (128 MB) DDR2 SDRAM
    - 16Mx8 parallel and BPI configuration flash
    - 64Mb SPI Configuration and Storage Flash (with 4 extra SPI selects)
- Interfaces
    - 10/100/1000 PHY
    - JTAG programming and configuration Port
    - RS232 Port
    - Low-cost VGA

- Buttons and switches
  - ♦ 8 User LEDs
  - ♦ 8-position user DIP switch
  - ♦ 4 User push button switches
  - ♦ Reset push button switch
- User I/O and expansion
  - ♦ Digilent 6-pin header (2)
  - ♦ EXP expansion connector (2)
- Configuration and debug
  - ♦ JTAG
  - ♦ SystemACE™ module connector
  - ♦ Eridon debug connector (SATA)

Ordering Information

Table 1 lists the evaluation kit part numbers.

Table 1: **Evaluation Kit and Hardware Ordering Information**

Part Number	Hardware
HW-SD1800A-DSP-SB-UNI-G	XtremeDSP Starter Platform - Spartan-3A DSP 1800A Edition

Functional Description

A high-level block diagram of the Spartan-3A DSP Starter Platform is shown in Figure 1. Subsequent sections provide details of the board design.

3SD1800A-FG676

Configuration and Debug	Memory
System ACE Connector	128 MB DDR2 (32M X 32)
Parallel Cable IV JTAG Port	16 MB Parallel NOR Flash (16M x 8)
Eridon Debug/Comm Port	16 Mb SPI Flash

Clock Sources

- 125 MHz LVTTL OSC
- LVTTL OSC Socket
- 25.175 MHz VGA Clock

EXP Slot (168 IO)

- Connector
- Connector

Interfaces

- 10/100/1000 PHY
- RS232 Port
- Low-cost VGA

Miscellaneous IO

- Push Switches
- Dip Switches
- User LEDs
- 2x Digilent Headers

Power

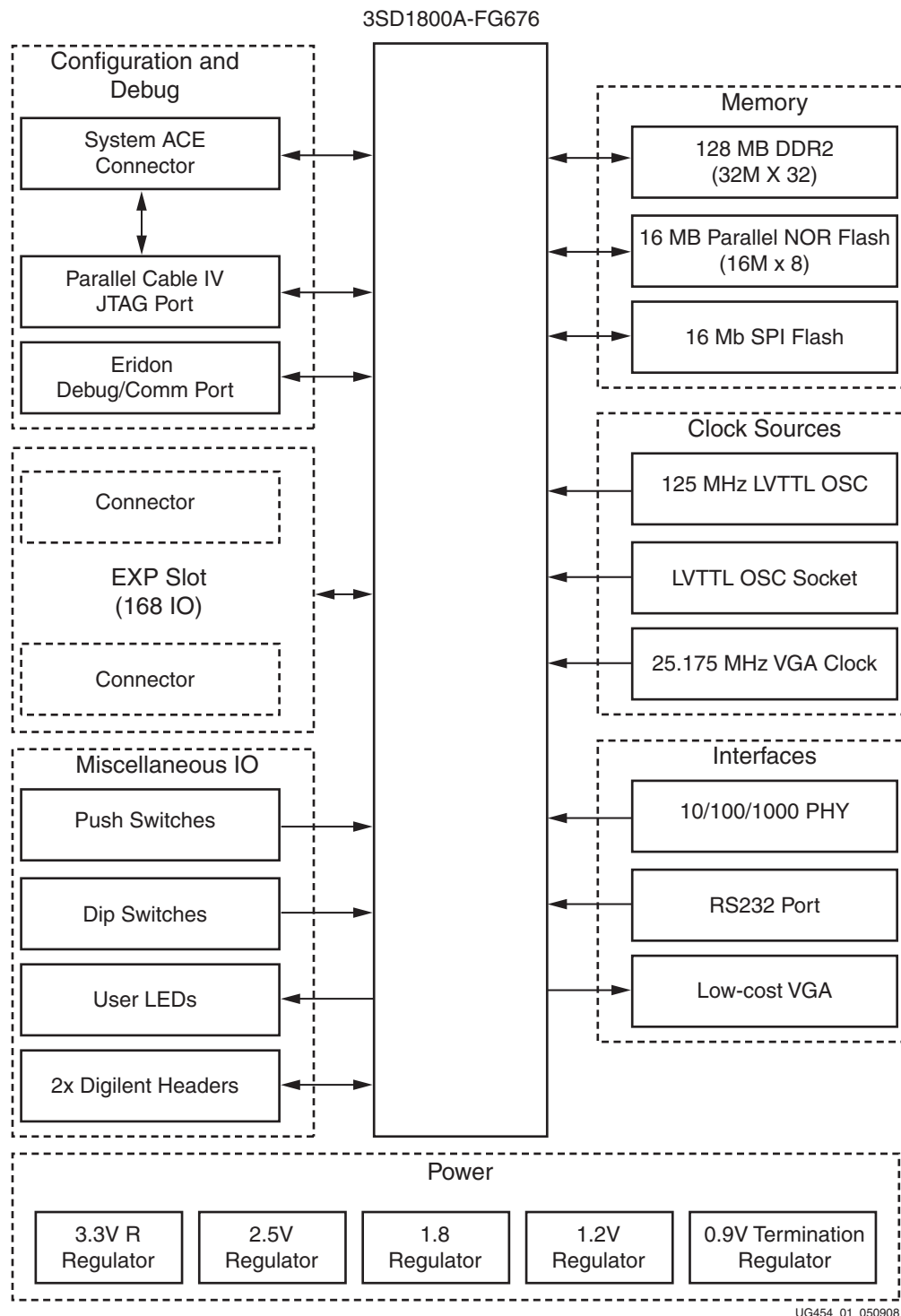| 3.3V R Regulator	2.5V Regulator	1.8 Regulator	1.2V Regulator	0.9V Termination Regulator

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Figure 1:   **Spartan-3A DSP Starter Platform Block Diagram**

Xilinx Spartan-3A DSP FPGA

The Xilinx XC3SD1800A-4FG676C device designed into the Spartan-3A DSP Starter Platform provides four I/O banks — two are fixed voltage and two are I/O voltage-selectable. The four I/O banks are described in Table 2 and detailed I/O pin usage is provided throughout this document. In some cases, voltage translation of I/O signals may be necessary in order to meet requirements of peripheral devices that are connected to a particular I/O bank, or EXP modules plugged into the EXP expansion connectors. Table 2 indicates where voltage translation will occur or, if a source is fixed at a particular voltage, even though the bank to which it is connected may be at different I/O voltage.

Table 2: **XC3SD1800A Input and Output Allocation**

I/O Bank Number	I/O Function	Number of I/O Pins	Number of Input-only Pins	Voltage Translation	Bank I/O Voltage
0	EXP Connector JX1	84	0		2.5 or 3.3 V
0	User Pushbuttons	0	4		
0	8-pos DIP Switch	0	8		
0	125 MHz Clock	1	0		
0	SMA Connector	1	0		
0	Configuration (PUDC_B)	1	0		
1	SystemACE Module	28	1		3.3 V
1	J3 Flash Memory	28	0		
1	SPI Selects (4)	4	0		
1	DAC	14	0		
1	User LEDs	8	0		
1	Digilent Connectors	8 [1]	0		
1	RS-232	2	0		
1	Eridon Debug Connector	4	0		
1	Configuration (Suspend)	1	0		
1	25.175 MHz Clock	1	0		
1	EXP Connector JX2	8	0	2.5 or 3.3 V	
2	EXP Connector JX2	76	0		2.5 or 3.3 V
2	J3 Flash Memory	8 [Ref 1]	0	2.5 or 3.3 V	
2	SPI	4[Ref 1]	0		
2	Configuration	5	0		
2	Plug-in Reset	1	0		
2	LED	1	0		
2	Power-on Reset	0	1		

Table 2: **XC3SD1800A Input and Output Allocation** *(Cont'd)*

I/O Bank Number	I/O Function	Number of I/O Pins	Number of Input-only Pins	Voltage Translation	Bank I/O Voltage
3	DDR2 Memory	73	0		1.8 V
3	Ethernet	17	13	2.5 V	

Note:

1. FLASH_DO and SPI_MISO are a common pin.

Memory

The Spartan-3A DSP Starter Platform is populated with both high-speed RAM (128Mbytes DDR2) and non-volatile ROM (16Mbytes parallel, and 64Mbit serial) to support various types of applications. Additionally, a 50-pin connector is provided for SystemACE interface (not included) that can be used to configure the Spartan-3A DSP FPGA, and to provide storage for A/V media files from removable Compact Flash cards. Figure 2 shows a high-level block diagram of the memory interfaces on this board.

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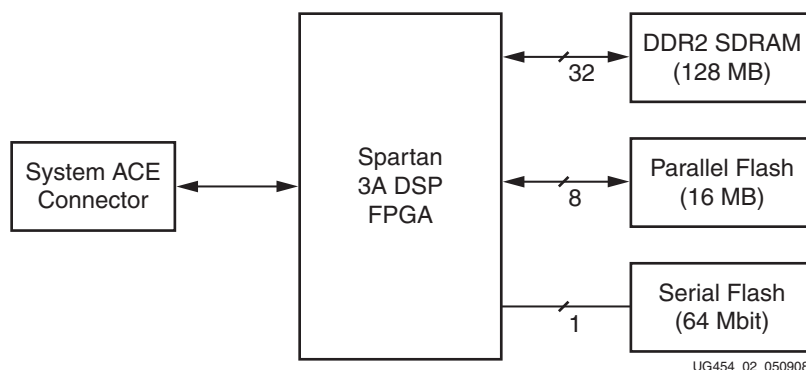
Figure 2: **Spartan-3A DSP Memory Interface**

Micron DDR2 SDRAM Interface

Two Micron MT47H32M16BM DDR2 devices provide 128Mbytes of 32-bit wide memory to the FPGA. The FPGA DDR2 interface supports SSTL18 signaling and all DDR2 signals are controlled impedance. The DDR2 data, mask, and strobe signals are matched length across all signals. Using I/O Bank 3 the DDR2 pinout on the FPGA is MIG-compliant. Pinout of the FPGA DDR2 interface is provided in Table 3 below.

SSTL18 Class I termination (series termination at the driving node and stub termination at the receiving node) is used between the FPGA and DDR on all unidirectional signals, such as Address, Control, and Clock. SSTL18 Class II termination (series and stub termination at both nodes) is used on the FPGA side of the interface for all bidirectional signals such as Data and Strobe. No board terminations are implemented for Data and Strobe on the memory side. ODT is strapped as enabled, although an FPGA I/O is still connected to allow the FPGA to drive this off. Note that stub terminations for address and control signals are not populated in production based on HyperLynx simulation and exhaustive, error-free testing of the FPGA-DDR2 interface at 133MHz.

Figure 3 shows terminator locations relative to the FPGA and the DDR2 memory devices.
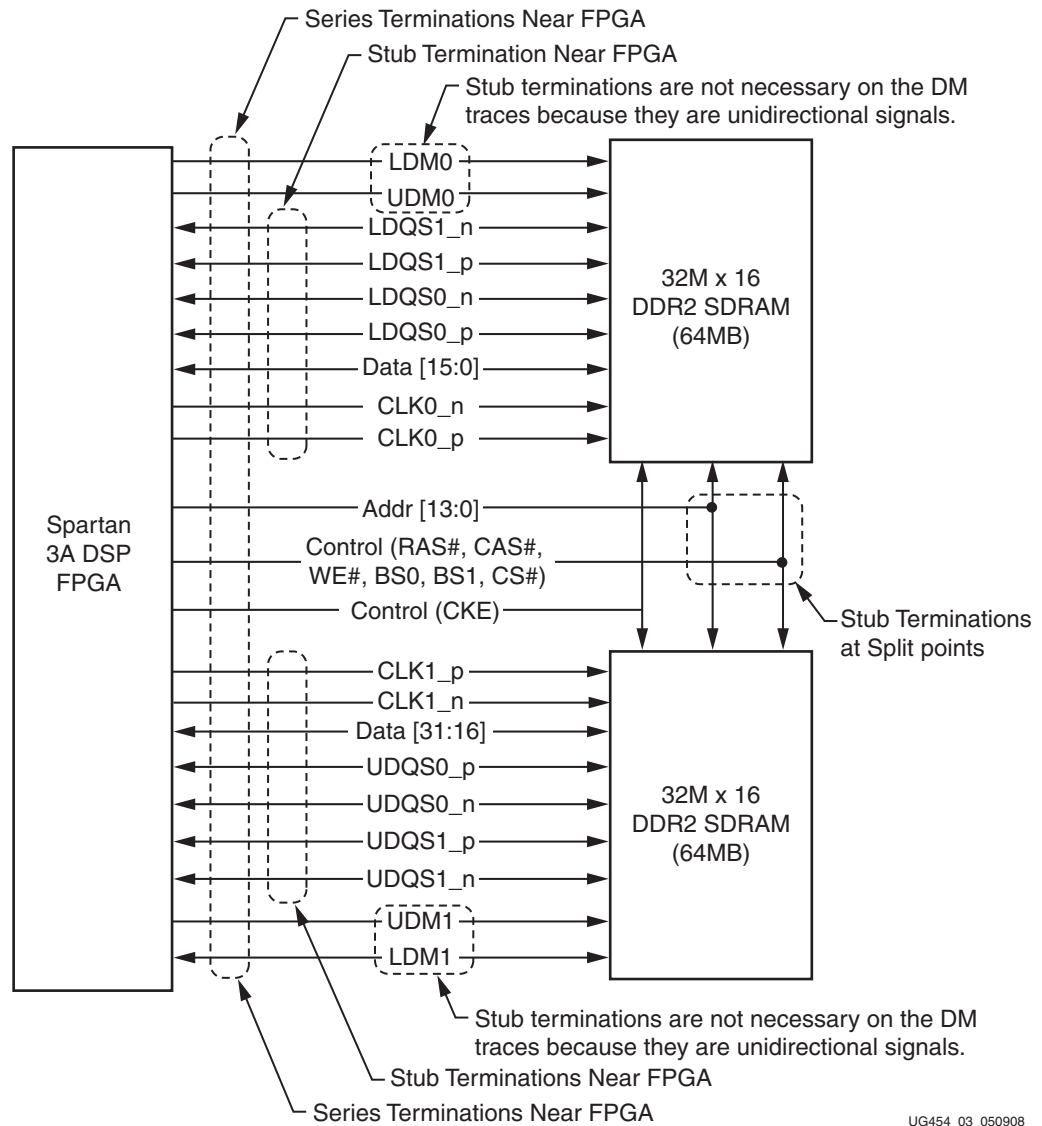
Figure 3: **DDR2 SDRAM Interface**

The following guidelines were used in the design of the DDR2 interface to the Spartan-3A DSP FPGA. These guidelines are based on Micron recommendations and board level simulation. Ideal impedance values are listed. Actual values may vary.

- Memory clocks routed differentially
- 50-ohm controlled trace impedance
- 24-ohm series termination on bidirectional signals at the FPGA
- Parallel termination following the memory device connection on all signals
- 60-ohm pull-up resistor to the termination supply (0.9V) on data and strobe signals at the FPGA

- 60-ohm pull-up resistor to the termination supply at the split-point of shared signals (control, address)
- Termination supply that can both source and sink current
- Feedback clock routed with twice the length to simulate the total flight time

All DDR2 routing is length-matched within certain tolerances; these are:

- Members of a differential pair matched to +/-10mil
- DQ, DQS, DM and CK matched to +/- 45mil
- Control matched to +/- 100mil of data interface
- RST_DQS_DIV and MB_FB_CLK matched to +/- 45mil of sum of average DQS and average CK

The DDR2 signals are connected to I/O Bank 3 of the Spartan-3 SA DSP FPGA. The output supply pins (VCCO) for Bank 3 is connected to 1.8 Volts. A Texas Instruments TPS51116 Buck Controller and ancillary circuitry provides the 1.8V DDR2 power, the 0.9V termination voltage (FPGA_0.9V_TT) and the DDR2 reference voltage (FPGA_DDR2_VREF). This power source also supplies the 1.8V core voltage to the Ethernet PHY.

Table 3: **FPGA DDR2 Interface Pinout**

DDR2 Signal	FPGA Pin Number	DDR2 Signal	FPGA Pin Number
FPGA_DDR_A0	J5	FPGA_DDR_LDM_0	V2
FPGA_DDR_A1	M8	FPGA_DDR_LDM_0	V1
FPGA_DDR_A2	M10	FPGA_DDR_LDM_1	R2
FPGA_DDR_A3	K4	FPGA_DDR_UDM_1	M6
FPGA_DDR_A4	K5	DDR2_ODT_Control	G3
FPGA_DDR_A5	K2	FPGA_DDR_D0	U9
FPGA_DDR_A6	K3	FPGA_DDR_D1	V8
FPGA_DDR_A7	L3	FPGA_DDR_D2	AB1
FPGA_DDR_A8	L4	FPGA_DDR_D3	AC1
FPGA_DDR_A9	M7	FPGA_DDR_D4	Y5
FPGA_DDR_A10	M8	FPGA_DDR_D5	Y6
FPGA_DDR_A11	M3	FPGA_DDR_D6	U7
FPGA_DDR_A12	M4	FPGA_DDR_D7	U8
FPGA_DDR_BS0	K6	FPGA_DDR_D8	AA2
FPGA_DDR_BS1	J4	FPGA_DDR_D9	AA3
FPGA_DDR_RAS#	H1	FPGA_DDR_D10	Y1
FPGA_DDR_CAS#	L10	FPGA_DDR_D11	Y2
FPGA_DDR_WE#	L9	FPGA_DDR_D12	T7
FPGA_DDR_CS#	H2	FPGA_DDR_D13	U6
FPGA_DDR_CKE	L7	FPGA_DDR_D14	U5

Table 3: **FPGA DDR2 Interface Pinout** *(Cont'd)*

DDR2 Signal	FPGA Pin Number	DDR2 Signal	FPGA Pin Number
FPGA_DDR_CLK_0	N1	FPGA_DDR_D15	V5
FPGA_DDR_CLK_0#	N2	FPGA_DDR_D16	R8
FPGA_DDR_CLK_1	N5	FPGA_DDR_D17	R7
FPGA_DDR_CLK_1#	N4	FPGA_DDR_D18	U1
MB_FB_CLK (out)	M2	FPGA_DDR_D19	U2
MB_FB_CLK (in)	N7	FPGA_DDR_D20	P8
RST_DQS_DIV (out)	T10	FPGA_DDR_D21	P9
RST_DQS_DIV (in)	T9	FPGA_DDR_D22	R5
FPGA_DDR_LDQS_0	V7	FPGA_DDR_D23	R6
FPGA_DDR_LDQS_#0	V6	FPGA_DDR_D24	P7
FPGA_DDR_LDQS_1	W3	FPGA_DDR_D25	P6
FPGA_DDR_LDQS_#_1	W4	FPGA_DDR_D26	T3
FPGA_DDR_UDQS_0	T5	FPGA_DDR_D27	T4
FPGA_DDR_UDQS_#0	U4	FPGA_DDR_D28	N9
FPGA_DDR_UDQS_1	R2	FPGA_DDR_D29	P10
FPGA_DDR_UDQS_#_1	R4	FPGA_DDR_D30	P4
		FPGA_DDR_D31	P3

Intel J3 Parallel Flash

The Flash memory consists of a single J3 Flash device in a TSOP-56 package and connected to the dedicated BPI configuration port of the FPGA. The Intel JS28F128J3D is a 128-Mbit device organized as 16-Mbit x 8. The installed J3 device supports asynchronous memory accesses at a 75 nanosecond access time. The Flash interface is split across two banks, with all but the 8 data bits connected to Bank 1 (3.3V), and the 8 data bits connected to Bank 2. Because Bank 2 may be set to either 2.5V or 3.3V, the 8 Flash data bits are interfaced to Bank 2 via a Texas Instruments SN74AVC8T245 dual-supply bus transceiver with the Flash Write Enable (FLASH_WE#) signal controlling transceiver direction and the Flash chip select signal (FLASH_CS) enabling the transceiver. The maximum propagation delay of 2.9 nanoseconds through this transceiver is not significant with the 75 nanosecond Flash access time. Jumper JP1 may be used to write-protect the Flash memory by placing a shunt across pins 2 and 3. Default setting is JP1 1:2. Table 4 details the Parallel Flash FPGA interface pinout.

Table 4: **Parallel Flash Interface Pinout**

J3 Flash Signal	FPGA Pin No.	J3 Flash Signal	FPGA Pin No.
FLASH_A0	AC23	FLASH_A18	J26
FLASH_A1	AC24	FLASH_A19	J25
FLASH_A2	R21	FLASH_A20	J21
FLASH_A3	R22	FLASH_A21	H21
FLASH_A4	T23	FLASH_A22	C26
FLASH_A5	T24	FLASH_A23	C25
FLASH_A6	R18	FLASH_WE#	Y20
FLASH_A7	R17	FLASH_OE#	AE26
FLASH_A8	R25	FLASH_CE#	AE25
FLASH_A9	R26	FLASH_Reset#	N24
FLASH_A10	M26	FLASH_D0	AF24
FLASH_A11	M25	FLASH_D1	AE18
FLASH_A12	L24	FLASH_D2	AF18
FLASH_A13	M23	FLASH_D3	Y15
FLASH_A14	N18	FLASH_D4	AE12
FLASH_A15	N17	FLASH_D5	AF12
FLASH_A16	N20	FLASH_D6	AF10
FLASH_A17	M20	FLASH_D7	AE10

Intel S33 Serial Flash

64Mbits of serial flash memory is provided by an Intel QH25F640S33B8 device interfaced to the Spartan 3A device via its dedicated SPI configuration interface. Jumper JP8 may be utilized to write-protect the device by placing a shunt across JP8 1:2 (default is open). The SPI interface signals are also connected to 0.1" 2x6 header J10 along with four additional SPI select lines (SPISEL_[1:4]); signals in Table 6 marked with an asterisk are common to both the SPI serial Flash and header J10. The built-in SPI interface is available only during configuration. The user must build the SPI controller during normal operation, or use IP available in Xilinx Platform Studio (XPS).

Table 5: **Serial (SPI) Flash Interface Pinout**

J3 Flash Signal	FPGA Pin	J3 Flash Signal	FPGA Pin
SPISEL_1	W20	* SPI_SEL#	AA7
SPISEL_1	W21	* SPI_CLK	AE24
SPISEL_1	AD26	* SPI_MOSI	AB15
SPISEL_1	AC25	* SPI_MISO	AF24

SystemACE Module (SAM) Connector

The Spartan-3A DSP Starter Platform provides a SAM 50-pin connector (J8) for SystemACE interface that can be used to configure the Spartan-3A DSP FPGA, and provide storage for A/V media files from removable Compact Flash cards. The Avnet SystemACE Module (DS-KIT-SYSTEMACE) can be used to perform both of these functions.

Further information on the Avnet SystemACE Module may be found at: www.em.avnet.com/systemace. This SystemACE module is not provided as part of this product.

Figure 4 shows the SystemACE Module connected to the header on the Spartan-3A DSP board; Table 6 provides the pinout of SAM connector J8. The clock from the SAM connector (Pin 6) is routed to GCLK1 on Bank 2 of the FPGA.
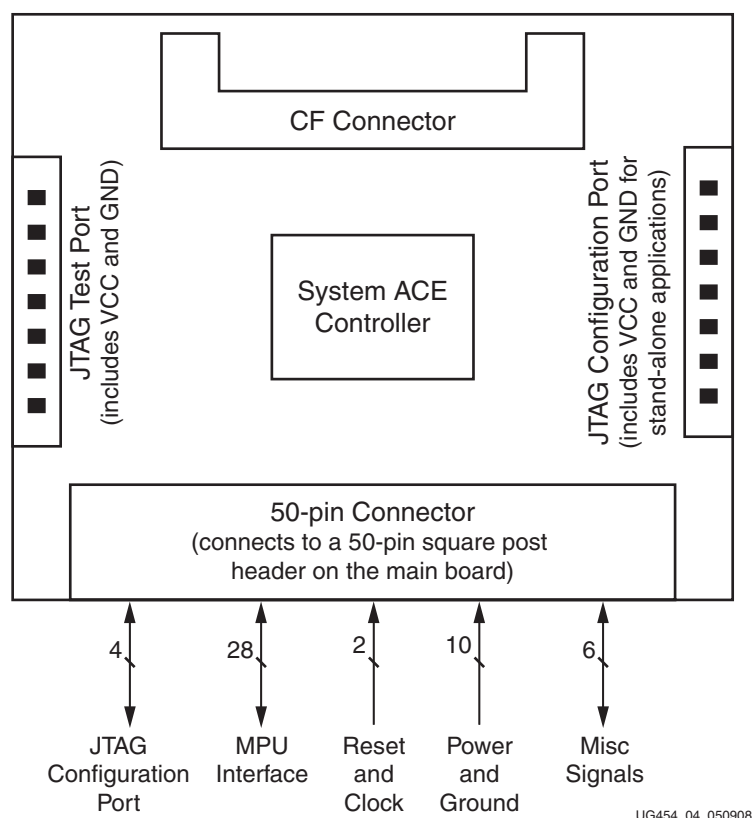

Figure 4: **SystemACE Module Interconnections**

Table 6: **SAM Interface Signals**

FPGA Pin Number	SystemACE Signal Name	SAM Connector Pin Number		SystemACE Signal Name	FPGA Pin Number
—	3.3 V	1	2	3.3 V	—
E23	JTAG_TDO	3	4	GND	—
D4	JTAG_TMS	5	6	SAM_CLK	AA14
G7	JTAG_TDI	7	8	GND	—
A2	FPGA_PROGn	9	10	JTAG_TCK	A25
—	GND	11	12	GND	—
V22	SAM_OEn	13	14	FPGA_INITn	AA15
AC26	SAM_A0	14	16	SAM_WEn	V24
AB23	SAM_A2	17	18	SAM_A1	AB26
—	2.5 V	19	20	SAM_A3	AB24
AA23	SAM_D0	21	22	2.5 V	—
U20	SAM_D2	23	24	SAM_D1	V21
AA25	SAM_D4	25	26	SAM_D3	AA24
U18	SAM_D6	27	28	SAM_D5	U19
Y23	SAM_D8	29	30	SAM_D7	Y22
T20	SAM_D10	31	32	SAM_D9	U21
Y25	SAM_D12	33	34	SAM_D11	Y24
T17	SAM_D14	35	36	SAM_D13	T18
V18	SAM_A4	37	38	SAM_D15	W23
AA22	SAM_A6	39	40	SAM_A5	V19
L23	SAM_IRQ	41	42	GND	—
V23	Sam_RESETn	43	44	SAM_CEn	V25
AB21	FPGA_DONE	45	46	SAM_BRDY	P21
AB24	FPGA_CCLK	47	48	BITSTREAM*	AF24
—	GND	49	50	NC (Key)	—

Interfaces

The Spartan-3A DSP FPGA has access to Ethernet and RS232 physical layer transceivers for communication purposes. Network access is provided by a 10/100/1000 Mb/s Ethernet PHY, which is connected to the Spartan-3A via a standard GMII interface. The PHY connects to the outside world with a standard RJ45 connector. Serial port communication to the FPGA fabric is provided through an RS232 transceiver using a DB9 DCE female connector.

Other interfaces consist of two 0.1" 6-pin headers to accept Digilent plug-in modules, a 7-pin Serial ATA connector (this is not a serial ATA interface) to connect to an Eridon debug module, and a 0.1" 2 x 6 header for SPI interface expansion.

National Semiconductor 10/100/1000 Ethernet PHY

The PHY is a National DP83865DVH Gig PHYTER" V. The DP83865 is a low power version of the National Gig PHYTER V with a 1.8V core voltage and 2.5V I/O voltage. The PHY also supports 3.3V I/O, but the 2.5V option is used on the board. The PHY is connected to a Tyco-AMP RJ-45 jack with integrated magnetics (part number: 1-6605833-1). The jack also integrates two LEDs and their corresponding resistors as well as several other passive components. External logic is used to logically OR the three link indicators for 10, 100 and 1000 Mb/s to drive a Link LED on the RJ-45 jack. The external logic is for the default strap options and may not work if the strap options are changed. Four more LEDs are provided on the board for status indication. These LEDs indicate Link at 10 Mb/s, Link at 100 Mb/s, Link at 1000 Mb/s and Full Duplex operation. The PHY clock is generated from its own 25 MHz crystal (FOX FX325BS).

Figure 5 shows a high-level block diagram of the interface to the DP83865 Tri-mode Ethernet PHY. The PHY signal connections at the FPGA are listed in Table 7. These signals are connected to FPGA Bank 3 which is fixed at +1.8V I/O voltage, necessitating voltage translation between +1.8V and +2.5V to match the PHY I/O voltage requirements.
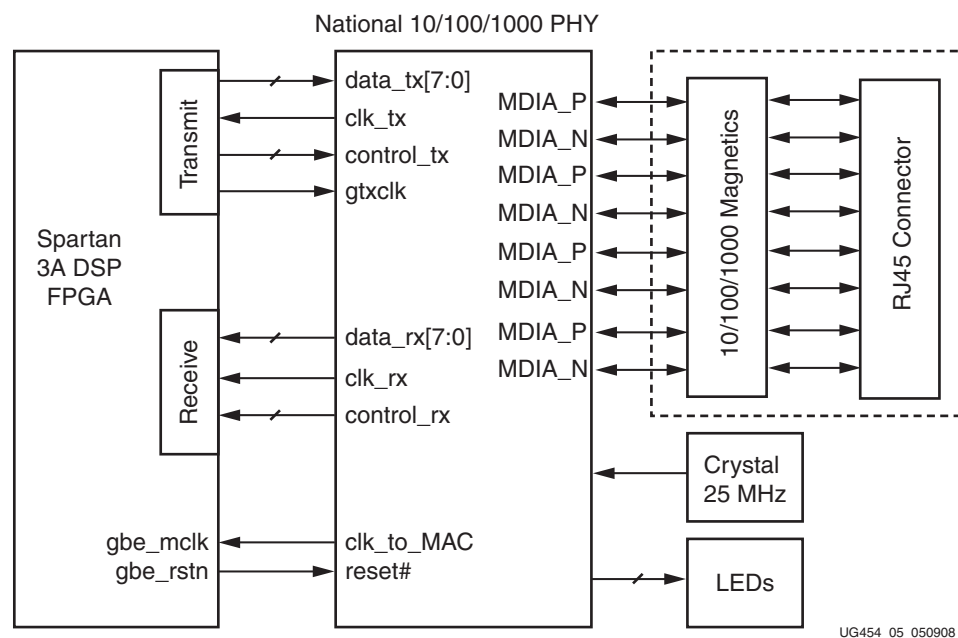

Figure 5:   **10/100/1000 Mb/s Ethernet Interface**

Table 7: **Ethernet PHY Interface Signals**

Ethernet PHY Signal	FPGA Pin	Ethernet PHY Signal	FPGA Pin
ETH_Tx_D	J8	ETH_COL	Y3
ETH_Tx_D	J9	ETH_INT#	J1
ETH_Tx_D	B2	ETH_Rx_DV	D1
ETH_Tx_D	B1	ETH_Rx_ER	J3
ETH_Tx_D	G6	ETH_MCLK	N6
ETH_Tx_D	H7	ETH_Rx_CLK	P1
ETH_Tx_D	K9	ETH_Tx_CLK	P2
ETH_Tx_D	K8	ETH_Rx_D0	C2
ETH_Tx_EN	D3	ETH_Rx_D1	G2
ETH_Tx_ER	E4	ETH_Rx_D2	G5
ETH_GTX_CLK	E3	ETH_Rx_D3	D2
ETH_MDC	F4	ETH_Rx_D4	Ab3
ETH_MDIO	F5	ETH_Rx_D5	Aa4
ETH_RST#	G4	ETH_Rx_D6	Ab4
ETH_CRS	G1	ETH_Rx_D7	Y4

The PHY address is set to 0b00001 by default. PHY address 0b00000 is reserved for a test mode and should not be used. Three-pad resistor jumpers are used to set the strapping options. These jumper pads provide the user with the ability to change the settings by moving the resistors. The dual-function pins that are used for both a strapping option and to drive an LED have a set of two jumpers per pin. The dual-function pins are indicated by an asterisk in the table.

The default options as indicated in Table 8 are Auto-Negotiation enabled, Full Duplex mode, Speed advertised as 10/100/1000 Mb/s, PHY address 0b00001, IEEE Compliant and Non-compliant support, straight cable in non-MDIX mode, auto-MDIX mode enabled, Single node (NIC) and CLK_TO_MAC enabled. These and other settings are enabled by three-pad jumpers with a resistor connecting either pads 1 and 2 or pads 2 and 3.

Table 8: **Ethernet PHY Hardware Strapping Options**

Function	Jumper Installation	Resistor	Mode Enabled
Auto Negotiation	JT8: Pins 1-2	0 Ohm	Auto-negation enabled (default)
	JT9: Pins 1-2		
	JT8: Pins 2-3	0 Ohm	Auto-negation disabled
	JT9: Pins 2-3		
Full/Half Duplex*	JT10: Pins 1-2	0 Ohm	Full Duplex (default)
	JT10: Pins 1-2		
	JT10: Pins 2-3	0 Ohm	Half Duplex
	JT11: Pins 2-3		
Speed 1*	JT12: Pins 1-2 JT13: Pins 1-1 (Speed1 – 0)	0 ohm	Speed Selection: (Auto-Neg enabled) Speed1 Speed0 Speed Advertised 1 1 1000BASE-T, 10BASE-T 1 0 1000BASE-T 0 1 1000BASE-T, 100BASE-Tx 0 0 10BASE-T Default: 1000BASE-T, 100BASE-TX, 10BASE-T
Speed 0*	JT6: Pins 1-2 JT7: Pins 1-1 (Speed0 – 0)	0 Ohm	
PHY address 0*	JT14: Pins 1-2	0 Ohm	PHY Address 0b00001 (default)
	JT15: Pins 1-2		
	JT24: Pins 2-3		PHY Address 0b00000
	JT25: Pins 2-3		
Non-IEEE Compliant Mode	JT1: Pins 1-2	1 K	Compliant and non-compliant operation (default)
	JT1: Pins 2-3		Inhibits non-compliant operation
Manual MDIX Setting	JT39: Pins 1-2	1 K	Straight Mode (default)
	JT2: Pins 2-3		Cross-over Mode
Auto MDIX Setting	JT4: Pins 1-2	1 K	Automatic Pair Swap – MDIX (default)
	JT4: Pins 2-3		Set to manual preset – Manual MDIX Setting (JT12)
Multiple Node Enable	JT3: Pins 1-2	1 K	Single node – NIC (default)
	JT3: Pins 2-3		Multiple node priority – switch/hub
Clock to MAC Enable	JT5: Pins 1-2	1 K	CLK_TO_MAC output enabled (default)
	JT5: Pins 2-3		CLK_TO_MAC output disabled

The auto-MDIX mode provides automatic swapping of the differential pairs. This allows the PHY to work with either a straight-through cable or crossover cable. Use a CAT-5e or CAT-6 Ethernet cable when operating at 1000 Mb/s (Gigabit Ethernet). The boundary-scan Test Access Port (TAP) controller of the DP83865 must be in reset for normal operation. This active low reset pin of the TAP (TRST) is pulled low through a 1K resistor on the board.

RS232

The RS232 transceiver is a Texas Instruments MAX3221 device. This transceiver operates at 3.3V with an internal charge pump to create the RS232 compatible output levels. The RS232 interface is brought out on DB9 connector P2. This RS232 interface supports only null-modem serial cables. A male-to-female serial cable should be used to plug J11 into a standard PC serial port (male DB9). Table 9 shows the FPGA pin-out for the RS232 interface.

Table 9: **RS232 Signals**

Net Name	Description	FGPA Pin Number
FPGA_RS232_Rx	Receive data, RD	N21
FPGA_RS232_Tx	Transmit data, TD	P22

SPI Expansion

A 0.1" 2 x 6 header (J10) provides an expansion of the FPGA SPI interface. In addition to the SPI signals SPI_SEL#, SPI_CLK, SPI_MOSI and SPI_MISO, four additional SPI select signals are provides (SPISEL_1, SPISEL_2, SPISEL_3, and SPISEL_4). All SPI select signals have 4.7K pull-ups, SPI_CLK has a 4.7K pull-down. 3.3V power and Ground are also provided on J10. Table 10 lists and describes the J10 connections.

Table 10: **SPI Connector (J10)**

FPGA Pin Number	Signal	J10 Pin Number	J10 Pin Number	Signal	FPGA Pin Number
W20	SPISEL_1	2	1	SPI_SEL#	AA7
W21	SPISEL_2	4	3	SPI_MOSI	Ab15
AD26	SPISEL_3	6	5	SPI_MISO	AF24
AC25	SPISEL_4	8	7	SPI_CLK	AE24
—	GND	10	9	GND	—
—	3.3 V	12	11	3.3 V	—

Digilent Headers

Two right-angle, 6 pin (1 x 6 female) Digilent headers (J6, J7) are provided on the Spartan-3A DSP Starter Platform. Each header provides 3.3V power, Ground, and four I/Os. It has the *appearance* of an SPI port, or can be used as 4 general purpose I/Os. Figure 6 shows the pinout of the Digilent headers; Table 11 provides the FPGA pinout.

For Digilent modules, see:
http://www.digilentinc.com/Products/Catalog.cfm?Nav1=Products&Nav2=Peripheral&Cat=Peripheral.
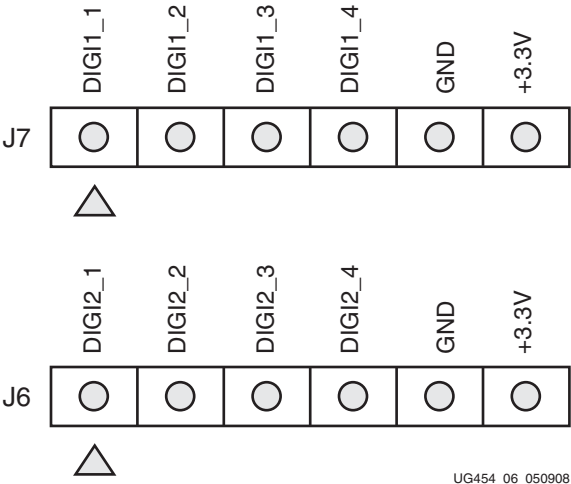
Figure 6: **Digilent Header Pinout**

Table 11: **Digilent Header Connections**

J6 Signal	FPGA Pin	J7 Signal	FPGA Pin
DIGI2_1	K19	DIGI1_1	L18
DIGI2_2	K18	DIGI1_2	L17
DIGI2_3	F22	DIGI1_3	E24
DIGI2_4	G22	DIGI1_4	F23

Debug Connector (This is not a Serial ATA Connector)

A Serial ATA connector (J3) provides a high-speed interface for use as a serial debug port (not Serial ATA), but may be used as a general-purpose communication interface. Two 3.3V LVDS differential pairs, nominally one transmit pair (DBG_Tx_p/DBG_Tx_n) and one receive pair (DBG_Rx_p/DBG_Rx_n), provide this high-speed communication channel. Common-mode of the transmit pair is set to 1.25V by resistor R11 to 3.3V and resistor R8 to Ground. 100-ohm differential termination of the receive pair is provided by resistor R10. Nominal trace impedance is 50-ohms, with 49.9-ohm series resistors placed close to the FPGA. Table 12 identifies the connection of the J3 signals to the FPGA.

Table 12: **Debug Connector (J3)**

J3 Pin Number	Signal Name	FPGA Pin
1	GND	—
2	DBG_Tx_n	D26
3	DBG_Tx_p	E26

Table 12: **Debug Connector (J3)**

J3 Pin Number	Signal Name	FPGA Pin
4	GND	—
5	DBG_Rx_n	J20
6	DBG_Rx_p	J10
7	GND	—

VGA Output

The Spartan-3A DSP Starter Platform includes a VGA video output using a resistor-divider network and 4-bits per RGB color as shown in Figure 7. This resistor-divider network is 510, 1K, 2K, & 4K ohms for each color. The outputs of the three resistor-divider networks are presented to DB15 connector P1. Horizontal and Vertical synchronization signals are also generated by the FPGA and provided to P1. Additionally, a 25.175 MHz clock (VGA-resolution) is added to the board, feeding directly to the FPGA at RHCLK2 (P26) on Bank 1. This clock should be used in the FPGA controller for timing the output and generating the image and syncs. The VGA pin assignments are listed in Table 13.

UG454_07_050908
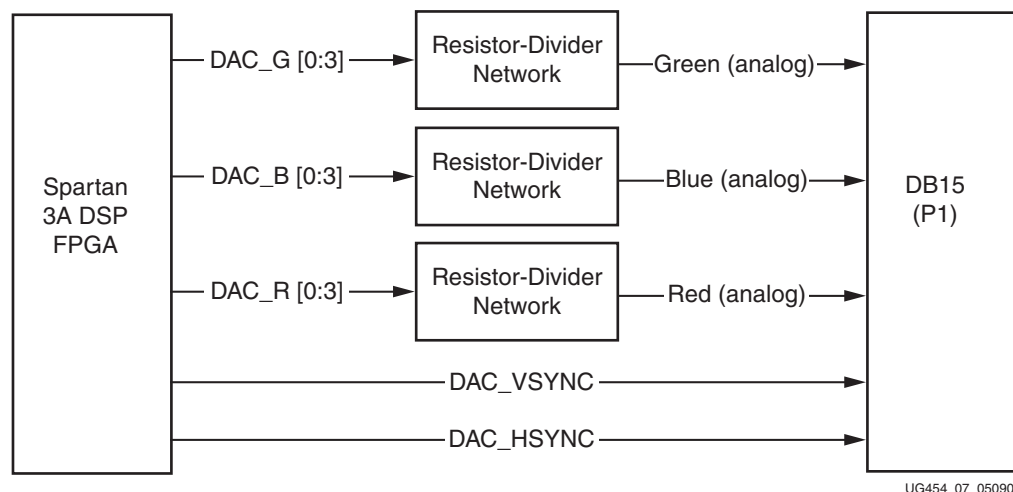
Figure 7: **VGA Output**

Table 13: **VGA Pin Assignments**

VGA Signal	FPGA Pin	VGA Signal	FPGA Pin
DAC_G0	M19	DAC_R0	L20
DAC_G1	M18	DAC_R1	K20
DAC_G2	J23	DAC_R2	F25
DAC_G3	J22	DAC_R3	F24
DAC_B0	L22	DAC_VSYNC	K25
DAC_B1	K21	DAC_HSYNC	K26

Table 13: **VGA Pin Assignments**

VGA Signal	FPGA Pin		VGA Signal	FPGA Pin
DAC_B2	G23		CLK_25.175MHz	P26
DAC_B3	G24			

Miscellaneous I/O

An 8-position DIP switch, 4 user Pushbuttons, and 8 user LEDs are provided on the Spartan-3A DSP Starter Platform. The connection of these devices to the FPGA is detailed in Table 14. The DIP switch is connected to FPGA Bank 0 and each switch is pulled low in the "OFF" position. Turning the switch "ON" causes the corresponding FPGA pin to be pulled to 2.5V or 3.3V, depending on the setting of the Bank 0 I/O voltage (VCCO_0). Like the DIP switch, the four user pushbuttons are also pulled low and depressing any button will cause the corresponding FPGA pin to be driven to the value of VCCO_0. Driving a "High" to the LEDs will cause them to light.

Table 14: **Devices and Pin Assignments**

Device	Name	FPGA Pin
DIP Switch	SW3.1	A7
	SW3.2	G16
	SW3.3	E9
	SW3.4	D15
	SW3.5	D19
	SW3.6	B24
	SW3.7	A5
	SW3.8	A23
Push Buttons	SW5 (SWITCH_PB1)	J17
	SW6 (SWITCH_PB2)	J15
	SW7 (SWITCH_PB3)	J13
	SW8 (SWITCH_PB4)	J10
LEDs	LED1 (D14)	P18
	LED2 (D13)	P25
	LED3 (D12)	N19
	LED4 (D11)	K22
	LED5 (D10)	H20
	LED6 (D9)	G21
	LED7 (D8)	D24
	LED8 (D7)	D25

Expansion Connectors

The Spartan-3A DSP Starter Platform provides expansion capabilities for customized user application daughter cards and interfaces over two EXP expansion connectors. The EXP expansion connectors on the board can support two half-card EXP modules or a single dual slot EXP module. Both off-the-shelf EXP modules and user-developed modules can easily be plugged onto the Spartan-3A DSP Starter Platform to add features and functions to the backend application of the main board.

EXP Interfaces

The EXP specification defines a 132-pin connector, with 24 power I/Os, 24 grounds I/Os, and 84 user I/Os. The standard EXP configuration implemented on the Spartan-3A DSP Starter Platform uses two connectors (Samtec part number QTE-060-09-F-D-A) in a dual slot EXP configuration, for a total of 168 user I/Os. Using a jumper, the voltage levels for the EXP user I/O can be set to either 2.5V or 3.3V. As shown in Figure 8, JP2 and JP3 set the I/O voltage for the EXP connectors labeled JX1 and JX2 respectively, by setting the VCCO voltage for the banks of the FPGA that connect to the EXP I/O. Table 15 provides an overview of the EXP signals; Tables 17 and 18 provide the FPGA pinouts for EXP connectors JX1 and JX2, respectively. Table 16 and Table 17 do not show the connector ground blades (numbered 122 through 131 on the schematic and PCB) that are positioned in the center of the connector. Technically, these are not *pins* and are not identified as such in this document. For more information on the EXP open specification from Avnet, see www.em.avnet.com/exp.
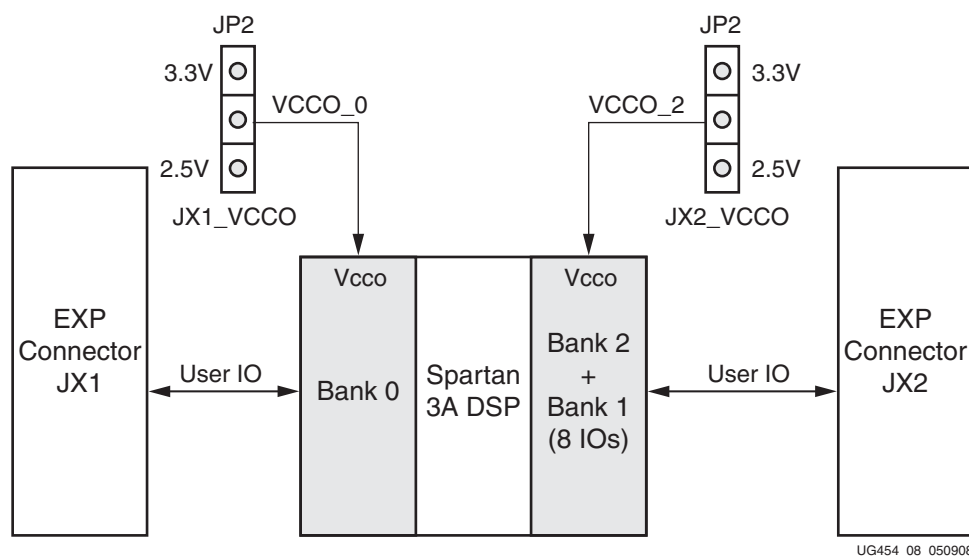

Figure 8: **EXP I/O Voltage Settings**

The EXP specification defines four user signal types:

Single Ended I/O, Differential I/O, Differential, Single Ended Clock Inputs, and Differential and Single Ended Clock Outputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the EXP

specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the baseboard and EXP module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require single-ended signals only can use each differential pair as two single-ended signals, for a total of 84 single-ended I/O per connector (168 total in the dual slot configuration).

Table 15: **EXP Connector Signals**

Net Names	Signal Description	Quantity	Quantity per Dual Slot
EXPx_SE_IO	Single-ended I/O	34	68
EXPx_SE_CLK_IN	Single-ended clock inputs	2	4
EXPx_DIFF_p/n	Differential I/O pairs	22	44
EXPx_DIFF_CLK_IN_p/n	Differential clock input pair, global	1	2
EXPx_DIFF_CLK_OUT_p/n	Differential clock output pairs	1	2
Total		64	168

The Spartan-3A DSP FPGA user I/O pins that connect to the two EXP connectors are shown in the following tables. The Samtec QTE connector plugs on the Spartan-3A DSP Starter Platform (part number: QTE-060-09-F-D-A) mate with the Samtec QSE high-performance receptacles (part number: QSE-060-01-F-D-A), located on the daughter card. Samtec also provides several high-performance ribbon cables that will mate to the JX1 and JX2 connectors.

Table 16: **EXP Connector JX1 Pinout**

FPGA Pin No.	Net Name	EXP Connector Pin No. (JX1)		Net Name	FPGA Pin No.
C22	EXP1_SE_IO_0	2	1	EXP1_SE_IO_1	G20
A22	EXP1_SE_IO_2	4	3	EXP1_SE_IO_3	G19
-	2.5V	6	5	2.5V	-
C21	EXP1_SE_IO_4	8	7	EXP1_SE_IO_5	E21
B21	EXP1_SE_IO_6	10	9	EXP1_SE_IO_7	D23
-	2.5V	12	11	2.5V	-
C20	EXP1_SE_IO_8	14	13	EXP1_SE_IO_9	B23
B20	EXP1_SE_IO_10	16	15	EXP1_SE_IO_11	C23
-	2.5V	18	17	2.5V	-
A20	EXP1_SE_IO_12	20	19	EXP1_SE_IO_13	D22
D20	EXP1_SE_IO_14	22	21	EXP1_SE_IO_15	D21
-	2.5V	24	23	2.5V	-
-	2.5V	24	23	2.5V	-

Table 16: **EXP Connector JX1 Pinout** *(Cont'd)*

FPGA Pin No.	Net Name	EXP Connector Pin No. (JX1)		Net Name	FPGA Pin No.
B19	EXP1_SE_IO_16	26	25	EXP1_SE_IO_17	F20
A19	EXP1_SE_IO_18	28	27	EXP1_SE_IO_19	H17
-	2.5V	30	29	2.5V	-
C18	EXP1_SE_IO_20	32	31	EXP1_SE_IO_21	F19
B18	EXP1_SE_IO_22	34	33	EXP1_SE_IO_23	G17
-	2.5V	36	35	2.5V	-
A18	EXP1_SE_IO_24	38	37	EXP1_SE_IO_25	K16
C17	EXP1_SE_IO_26	40	39	EXP1_SE_IO_27	F17
B14	EXP1_DIFF_CLK_IN_p	42	41	EXP1_SE_IO_28	D18
A14	EXP1_DIFF_CLK_IN_n	44	43	EXP1_SE_CLK_IN	J14
-	GND	46	45	GND	-
D17	EXP1_SE_IO_30	48	47	EXP1_SE_IO_29	E17
B17	EXP1_SE_IO_31	50	49	EXP1_SE_CLK_OUT	G10
	GND	52	51	GND	-
D16	EXP1_DIFF_p20	54	53	EXP1_DIFF_p21	B15
C15	EXP1_DIFF_n20	56	55	EXP1_DIFF_n21	A15
-	GND	58	57	GND	-
D13	EXP1_DIFF_p18	60	59	EXP1_SE_IO_32	C16
C12	EXP1_DIFF_n18	62	61	EXP1_SE_IO_33	J16
-	GND	64	63	GND	-
A12	EXP1_DIFF_p16	66	65	EXP1_DIFF_p19	F15
B12	EXP1_DIFF_n16	68	67	EXP1_DIFF_n19	E15
-	GND	70	69	GND	-
A4	EXP1_DIFF_CLK_OUT_p	72	71	EXP1_DIFF_p17	E14
B4	EXP1_DIFF_CLK_OUT_n	74	73	EXP1_DIFF_n17	F14
-	GND	76	75	GND	-
C11	EXP1_DIFF_p14	78	77	EXP1_DIFF_p15	G15
D11	EXP1_DIFF_n14	80	79	EXP1_DIFF_n15	H15
C10	EXP1_DIFF_p12	82	81	EXP1_DIFF_p13	G12
D10	EXP1_DIFF_n12	84	83	EXP1_DIFF_n13	H12
-	3.3V	86	85	3.3V	-
-	3.3V	86	85	3.3V	-