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# XtremeDSP™ Development Platform: Spartan-3A DSP 3400A Edition

## User Guide

**UG498 (v2.2) November 17, 2008**

XILINX®

# Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 6/2007 | 0.1 | Preliminary version. |
| 7/2007 | 0.2 | Added appendix. |
| 7/2007 | 0.3 | Updated version for final review. |
| 8/2007 | 1.0 | • Updated FMC information.<br>• Updated support information.<br>• Added FPGA pin assignments for DDR2 interface.<br>• Added FPGA pin assignments for USB/System ACE interface. |
| 9/2007 | 1.1 | Added Known Issues section: Limitation of DDR2 clock rate to 133 MHz; Soft Touch connector not compliant with Agilent probes; FMC connector is in violation of some rules of the standard. |
| 10/2007 | 1.2 | • Updated Table 20 (Serial Port FPGA Pin Assignments) and modified layout to reflect change in corporate image.<br>• Updated for XtremeDSP Spartan-3A DSP Development Board Revision D. |
| 10/2007 | 2.0 | Updated for XtremeDSP Spartan-3A DSP Development Board Revision. |
| 1/2008 | 2.1 | Updated with new clock generator configuration. |
| 11/17/08 | 2.2 | • Ported to Xilinx template.<br>• Updated Table 12 (FMC Pin G3 is attached to net 1_CLK0_C2M_N).<br>• Updated to account for PS6 being the power supply used for FMC 2 adjustable voltage. |

# Table of Contents

# Schedule of Figures

## Chapter 1: Introduction



## Chapter 2: Configuration Options



## Chapter 3: Programming the IDT Clock Chip

# Schedule of Tables

## Chapter 1: Introduction

# About This Guide

The *XtremeDSP™ Development Platform: Spartan-3A DSP 3400A Edition User Guide* provides instructions for designing and accelerating the development of new products. The XtremeDSP Development Platform: Spartan-3A DSP 3400A Edition board is an excellent medium for consumer-oriented wireless and multimedia video applications, where cost-efficient solutions are essential. Throughout the remainder of this guide, the development board may be referred to as both the XtremeDSP Development Platform: Spartan-3A DSP 3400A Edition board and the Spartan-3A DSP 3400A Edition board.

## Guide Contents

The User Guide contains the following chapters:

- Preface, "About this Guide" introduces the organization and purpose of the User Guide and the conventions used in this document.
- Chapter 1, "Introduction," identifies the major components, parts, and functionality of the Spartan-3A DSP 3400A Edition board.
- Chapter 2, "Configuration Options," provides an overview of the four configuration methods available on the FPGA on the Spartan-3A DSP 3400A Edition board.
- Chapter 3, "Programming the IDT Clock Chip," provides step-by-step instructions for using the IDT software to generate a combination of clock frequencies and implement them on the development board.
- Appendix, "Technical Specifications," identifies the Spartan-3A DSP 3400A Edition board technical specifications.

## Additional Resources

To find additional documentation, see the Xilinx website at:

www.xilinx.com/support/documentation

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

# Conventions

This document uses the following conventions. An example illustrates each convention.

## Typographical

The following typographical conventions are used in this document:

| Convention | Meaning or Use | Example |
|---|---|---|
| `Courier font` | Messages, prompts, and program files that the system displays | `speed grade: - 100` |
| **`Courier bold`** | Literal commands that you enter in a syntactical statement | **`ngdbuild`** *design_name* |
| *Italic font* | References to other manuals | See the *Development System Reference Guide* for more information. |
| | Emphasis in text | If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected. |
| Square brackets `[ ]` | An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required. | **`ngdbuild`** `[`*`option_name`*`]` *`design_name`* |
| Braces `{ }` | A list of items from which you must choose one or more | **`lowpwr =`**`{`**`on`**`\|`**`off`**`}` |
| Vertical bar `\|` | Separates items in a list of choices | **`lowpwr =`**`{`**`on`**`\|`**`off`**`}` |
| Vertical ellipsis<br>.<br>.<br>. | Repetitive material that has been omitted | `IOB #1: Name = QOUT'`<br>`IOB #2: Name = CLKIN'`<br>.<br>.<br>. |
| Horizontal ellipsis `...` | Repetitive material that has been omitted | **`allow block`** *block_name loc1 loc2 ... locn;* |

## Online Document

The following conventions are used in this document:

| Convention | Meaning or Use | Example |
|---|---|---|
| Blue text | Cross-reference link to a location in the current document | See the section "Additional Resources" for details.<br>Refer to "Title Formats" in Chapter 1 for details. |

| Convention | Meaning or Use | Example |
|---|---|---|
| Red text | Cross-reference link to a location in another document | See Figure 2-5 in the *Virtex-II Platform FPGA User Guide.* |
| Blue, underlined text | Hyperlink to a website (URL) | Go to http://www.xilinx.com for the latest speed files. |

Chapter 1

# Introduction

This chapter identifies the major components, parts, and functionality of the Spartan-3A DSP 3400A Edition board.

## Spartan-3A DSP 3400A Edition Board Overview

Figure 1-1 displays a block diagram of the Spartan-3A DSP 3400A Edition board.

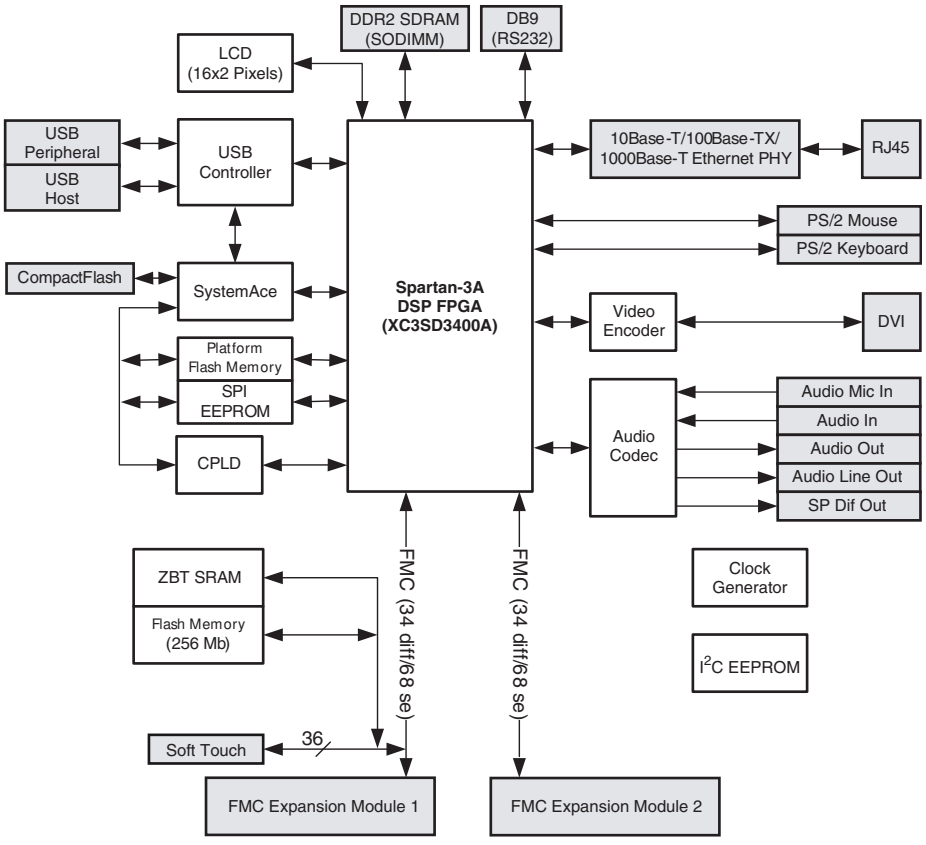


*Figure 1-1:* **Spartan-3A DSP 3400A Edition Board Block Diagram**

# Spartan-3A DSP 3400A Edition Board Hardware

## Board Parts: Top

Figure 1-2 illustrates the parts on the top of the Spartan-3A DSP 3400A Edition board. Each numbered item in the diagram is followed by a numbered description.

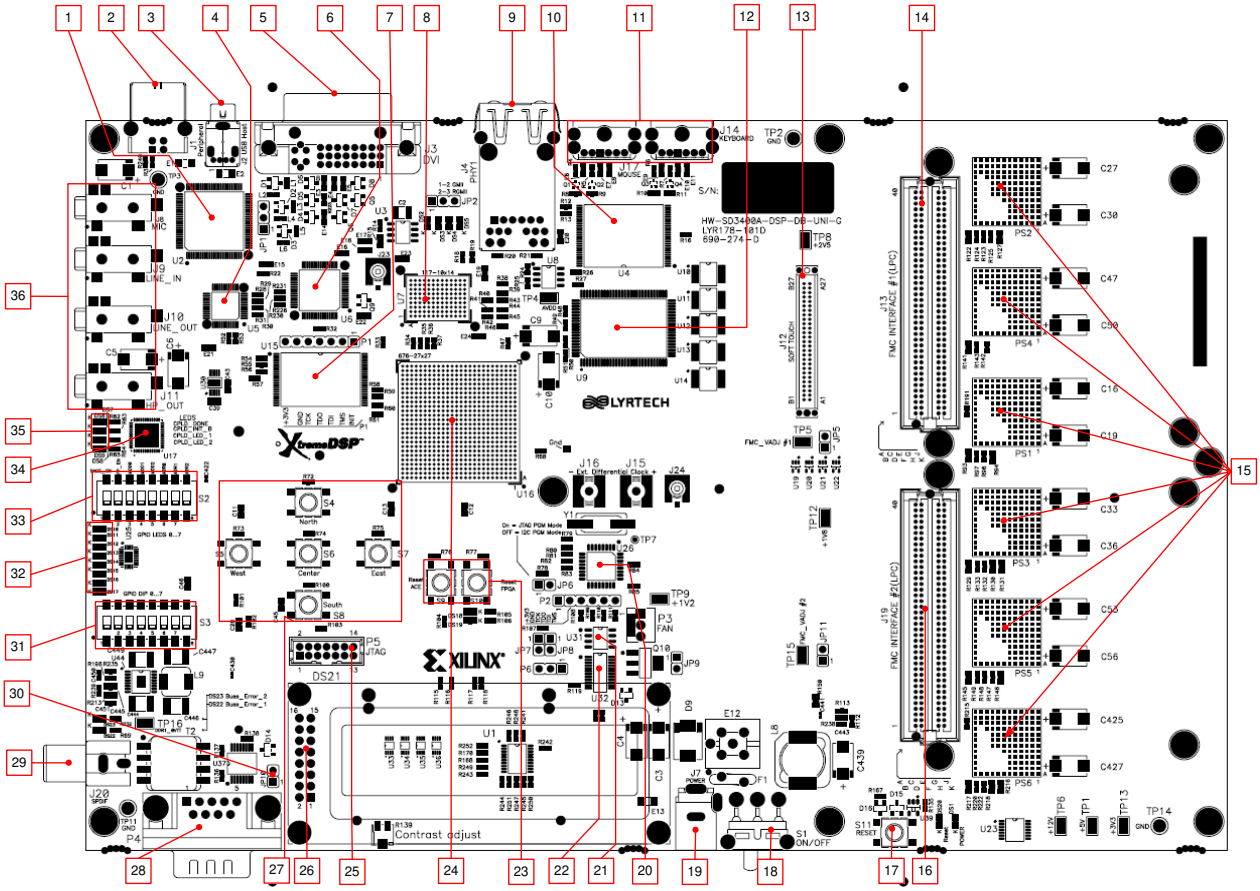


*Figure 1-2:* **Top View of Spartan-3A DSP 3400A Edition Board**

## Individual Board Parts

### 1. USB Controller

The Cypress CY7C67300 embedded USB host controller provides high-speed USB connectivity for the board, and supports host and peripheral modes of operation (see "2. USB Peripheral Port" and "3. USB Host Port"). The USB controller also has two Serial Interface Engines (SIE) that can be used independently. SIE1 is connected to the USB host port ("3. USB Host Port"), and SIE2 is connected to the USB peripheral port ("2. USB Peripheral Port").

The USB controller is equipped with an internal microprocessor to assist in processing USB commands. The firmware for this processor can be stored in its dedicated $I^2C$ EEPROM (U41) or downloaded from a host computer through the USB peripheral port (below). Jumper JP1 can be installed (shorting pins 1 and 2) to prevent the USB controller from executing firmware stored in the $I^2C$ EEPROM. The FPGA pins used for the USB interface are shared with the System ACE interface, as identified in Table 1-1.

*Table 1-1:* **USB/System ACE Interface Pin Assignments**

| FPGA Pin | Description | FPGA Pin | Description |
|---|---|---|---|
| AE13 | sysace_clk_in (System ACE only) | Y17 | sace_usb_d_0 |
| AE23 | sace_mpce (System ACE only) | AD21 | sace_usb_d_1 |
| AA18 | sysace_mpbready (System ACE only) | AA17 | sace_usb_d_2 |
| AB18 | sysace_mpirq (System ACE only) | AE21 | sace_usb_d_3 |
| W17 | usb_csn (USB only) | V16 | sace_usb_d_4 |
| AA9 | usb_int (USB only) | AC20 | sace_usb_d_5 |
| AD22 | usb_reset (USB only) | AD20 | sace_usb_d_6 |
| AC21 | sace_usb_oen | U16 | sace_usb_d_7 |
| V17 | sace_usb_wen | AF20 | sace_usb_d_8 |
| AF4 | sace_usb_a_0 | AE20 | sace_usb_d_9 |
| W9 | sace_usb_a_1 | AC19 | sace_usb_d_10 |
| Y9 | sace_usb_a_2 | AF19 | sace_usb_d_11 |
| AE3 | sace_usb_a_3 | AE19 | sace_usb_d_12 |
| AF3 | sace_usb_a_4 | AD19 | sace_usb_d_13 |
| V15 | sace_usb_a_5 | AC16 | sace_usb_d_14 |
| U15 | sace_usb_a_6 | AB16 | sace_usb_d_15 |

### 2. USB Peripheral Port

Type B connector, used to connect peripheral USB devices to the Spartan-3A DSP 3400A Edition board.

### 3. USB Host Port

Type A connector, used to connect a host device to the Spartan-3A DSP 3400A Edition board.

### 4. AC'97 SoundMAX Codec

Analog Devices AD1981B. The device supports 16-bit stereo audio and sampling rates up to 48 kHz. The sampling rate for recording and playback can also be different. Table 1-2 defines the pin assignments.

*Table 1-2:* **AC'97 SoundMAX Codec Interface Pin Assignments**

| FPGA Pin | Description |
|---|---|
| AC14 | CODEC_BIT_CLK |
| AC15 | CODEC_RESET_B |
| AB6 | CODEC_SDATA_IN |
| AD14 | CODEC_SDATA_OUT |
| W15 | CODEC_SYNC |

### 5. DVI Connector

Used to connect an external video monitor (DVI or VGA) to the Spartan-3A DSP 3400A Edition board. Table 1-3 defines the pin assignments.

**Note**: The VGA monitor can be connected to the development board with a DVI-to-VGA adaptor (sold separately).

*Table 1-3:* **DVI Interface Pin Assignments**

| FPGA Pin | Description | FPGA Pin | Description |
|---|---|---|---|
| AE7 | DVI_D_0 | V10 | DVI_D_10 |
| AE6 | DVI_D_1 | U11 | DVI_D_11 |
| AC8 | DVI_D_2 | AD17 | DVI_DE |
| AD7 | DVI_D_3 | AF25 | DVI_GPOI1 |
| AB7 | DVI_D_4 | AC11 | DVI_H |
| AF5 | DVI_D_5 | AD15 | DVI_RESET_B |
| AA10 | DVI_D_6 | AD11 | DVI_V |
| W10 | DVI_D_7 | AC12 | DVI_XCLK_N |
| Y10 | DVI_D_8 | AB12 | DVI_XCLK_P |
| V11 | DVI_D_9 | | |

### 6. Display Controller Device

The DVI circuitry uses a Chrontel CH7301C capable of 24-bit color and 1600 × 1200-pixel resolution. The display controller device drives the digital and analog signals to the DVI connector ("5. DVI Connector"). The display controller device is controlled through the $I^2C$ bus.

The DVI connector supports the $I^2C$ protocol, allowing the development board to read monitor configuration parameters, which can then be read by the FPGA through the $I^2C$ bus. See "I2C Bus Addressing," page 42 for detailed information.

### 7. Board Flash PROM

Xilinx XCF32P. This flash PROM is used to program the development board FPGA. The flash PROM can hold up to two distinct configuration images (up to four compressed configuration images) that can be accessed through the configuration DIP switches. Requires that you use the same configuration DIP switches to configure the FPGA from the platform flash PROM. See "33. Configuration DIP Switches" for detailed information.

### 8. Ethernet PHY

Marvell Alaska 88E1111 PHY device. This PHY supports 10Base-T, 100Base-TX, and 1000Base-T (Gigabit) Ethernet. The PHY is connected to the board's Ethernet connector ("9. Ethernet Port"). The Ethernet PHY is initialized under its default configuration when the development board is turned on or reset. Jumper JP2 selects whether the PHY's default is RGMII mode (pins 2-3) or GMII mode (pins 1-2). Table 1-4 defines the default configuration of the Ethernet PHY, which can be modified through software. Table 1-5 identifies the FPGA pin assignments for building new FPGA files.

*Table 1-4:* **Default Ethernet PHY Configuration**

| Configuration Pin | Board Connection | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|
| CONFIG0 | $V_{cc}$ 2.5 V | PHYADR[2] = 1 | PHYADR[1] = 1 | PHYADR[0] = 1 |
| CONFIG1 | Ground | ENA_PAUSE = 0 | PHYADR[4] = 0 | PHYADR[3] = 0 |
| CONFIG2 | $V_{cc}$ 2.5 V | ANEG[3] = 1 | ANEG[2] = 1 | ANEG[1] = 1 |
| CONFIG3 | $V_{cc}$ 2.5 V | ANEG[0] = 1 | ENA_XC = 1 | DIS_125 = 1 |
| CONFIG4 | $V_{cc}$ 2.5 V or LED_DUPLEX | HCWCFG_MODE [2] = 0 or 1 | HCWCFG_MODE [1] = 1 | HCWCFG_MODE [0] = 1 |
| CONFIG5 | $V_{cc}$ 2.5 V | DIS_FC = 1 | DIS_SLEEP = 1 | HCWCFG_MODE [3] = 1 |
| CONFIG6 | LED_RX | SEL_BDT = 0 | INT_POL = 1 | 50/75 ohm = 0 (50 ohm termination) |

*Table 1-5:* **Ethernet Interface Pin Assignments**

| FPGA Pin | Description | FPGA Pin | Description |
|---|---|---|---|
| AB13 | PHY_COL | AA14 | PHY_RX_CLK |
| AC10 | PHY_CRS | AC13 | PHY_RX_ER |
| AC6 | PHY_INT | AE17 | PHY_TXCTL_TXEN |
| AE4 | PHY_MDC | W13 | PHY_TXC_GTXCLK |
| AD6 | PHY_MDIO | V12 | PHY_TXD_0 |
| AE9 | PHY_RESET_N | AB9 | PHY_TXD_1 |
| AC17 | PHY_RXCTL_RXDV | W12 | PHY_TXD_2 |
| AF17 | PHY_RXD_0 | AC9 | PHY_TXD_3 |
| AD9 | PHY_RXD_1 | AA12 | PHY_TXD_4 |

*Table 1-5:* **Ethernet Interface Pin Assignments *(Cont'd)***

| FPGA Pin | Description | FPGA Pin | Description |
|---|---|---|---|
| AD12 | PHY_RXD_2 | AF9 | PHY_TXD_5 |
| AD16 | PHY_RXD_3 | AE8 | PHY_TXD_6 |
| AD10 | PHY_RXD_4 | AF8 | PHY_TXD_7 |
| AC22 | PHY_RXD_5 | Y14 | PHY_TX_CLK |
| AF22 | PHY_RXD_6 | V13 | PHY_TX_ER |
| AF15 | PHY_RXD_7 | | |

### 9. Ethernet Port

10Base-T, 100Base-TX, and 1000Base-T (Gigabit) Ethernet port. Connected to the Ethernet PHY ("8. Ethernet PHY").

### 10. Flash Memory

Intel StrataFlash embedded memory JS28F256P30B95; provides the development board with 32-MB flash memory. This memory provides non-volatile storage for data, software, or bitstreams. The device is 16-bits wide. This flash memory can also be used to program the FPGA. To use the Flash and ZBT memories, the memory enable pin must be set in the FPGA. Table 1-6 identifies the pin assignment.

**Note**: The FMC module 1 cannot be used when using ZBT or flash memory. Make sure that the FMC adjustable power supply no. 1 is configured for 3.3V to use the ZBT or flash memory. See FMC expansion connector for information about how to configure the adjustable power supply. The Flash memory shares the same address/data bus as the ZBT synchronous SRAM ("12. ZBT Synchronous SRAM").

*Table 1-6:* **Memory Enable Pin Assignment**

| FPGA Pin | Signal | Description |
|---|---|---|
| R9 | MEM_EN_B | 0: memory is accessible<br>1: memory is not accessible |

### 11. PS/2 Connectors

The Spartan-3A DSP 3400A Edition board is equipped with two PS/2 connectors, one each for a keyboard and mouse. Bi-directional level shifting transistors allow the 1.8-V I/O to interface with the 5-V I/O of the PS/2 connectors, which are powered directly from the 5-V power source of the development board. Connector J17 is used to connect a mouse, and connector J14 is used to connect a keyboard. Table 1-7 identifies the pin assignments.

**Note**: Be sure that the power load of the connected PS/2 devices does not overload the AC adapter of the development board.

*Table 1-7:* **PS/2 Pin Assignments**

| FPGA Pin | Description |
|---|---|
| R17 | KEYBOARD_CLK |
| R18 | KEYBOARD_DATA |
| H21 | MOUSE_CLK |
| J21 | MOUSE_DATA |

## 12. ZBT Synchronous SRAM

ISSI IS61NLP25636A-200TQL. The ZBT synchronous SRAM is high-speed, low-latency external memory for the FPGA. The memory is organized as 256K × 36 bits, providing a 32-bit data bus supporting four parity bits. The ZBT synchronous SRAM shares the same data bus as the flash memory (“10. Flash Memory”).

**Note**: FMC module #1 cannot be used when using ZBT synchronous SRAM. Make sure that FMC #1 adjustable power supply is configured for 3.3V to use the memory. See “14. FMC Expansion Connector #1” for information about configuring the adjustable power supply.

## 13. Soft Touch Connector

The Soft Touch connector (J12) lets you monitor signals between the FPGA and the FMC expansion connector #1. Table 1-8 defines the pin assignments.

*Table 1-8:* **Soft Touch Connector Pin Assignments**

| Soft Touch Pin | FPGA Pin | Description |
|---|---|---|
| A1 | H2 | FMC_LA03_P |
| A2 | H1 | FMC_LA03_N |
| A3 | NC | GND |
| A4 | J5 | FMC_LA14_P |
| A5 | J4 | FMC_LA14_N |
| A6 | NC | GND |
| A7 | L4 | FMC_LA06_P |
| A8 | L3 | FMC_LA06_N |
| A9 | NC | GND |
| A10 | P8 | FMC_LA32_P |
| A11 | P9 | FMC_LA32_N |
| A12 | NC | GND |
| A13 | U1 | FMC_LA28_P |
| A14 | U2 | FMC_LA28_N |

*Table 1-8:* **Soft Touch Connector Pin Assignments *(Cont'd)***

| Soft Touch Pin | FPGA Pin | Description |
|---|---|---|
| A15 | NC | GND |
| A16 | M10 | FMC_LA21_P |
| A17 | M9 | FMC_LA21_N |
| A18 | NC | GND |
| A19 | T5 | FMC_LA27_P |
| A20 | U4 | FMC_LA27_N |
| A21 | NC | GND |
| A22 | P7 | FMC_LA25_P |
| A23 | P6 | FMC_LA25_N |
| A24 | NC | GND |
| A25 | U5 | FMC_LA31_P |
| A26 | V5 | FMC_LA31_N |
| A27 | NC | GND |
| B1 | NC | GND |
| B2 | M8 | FMC_LA08_P |
| B3 | M7 | FMC_LA08_N |
| B4 | NC | GND |
| B5 | K3 | FMC_LA18_P |
| B6 | K2 | FMC_LA18_N |
| B7 | NC | GND |
| B8 | K5 | FMC_LA10_P |
| B9 | K4 | FMC_LA10_N |
| B10 | NC | GND |
| B11 | P4 | FMC_LA00_P_CC |
| B12 | P3 | FMC_LA00_N_CC |
| B13 | NC | GND |
| B14 | R8 | FMC_LA30_P |
| B15 | R7 | FMC_LA30_N |
| B16 | NC | GND |
| B17 | K6 | FMC_LA24_P |
| B18 | L7 | FMC_LA24_N |
| B19 | NC | GND |
| B20 | V1 | FMC_LA19_P |

*Table 1-8:* **Soft Touch Connector Pin Assignments *(Cont'd)***

| Soft Touch Pin | FPGA Pin | Description |
|---|---|---|
| B21 | V2 | FMC_LA19_N |
| B22 | NC | GND |
| B23 | R5 | FMC_LA29_P |
| B24 | R6 | FMC_LA29_N |
| B25 | NC | GND |
| B26 | T10 | FMC_LA33_P |
| B27 | T9 | FMC_LA33_N |

## 14. FMC Expansion Connector #1

Samtec ASP-134603-01. The FMC expansion connector #1 (J13) follows the VITA 57.1 FMC standard and is used in low pin count (LPC) format. It can either be used to accommodate a single width FMC Module or one dual FMC Module when used in conjuncture with FMC expansion connector #2 (J19). See FMC expansion connector for details. To use the Flash and ZBT memories, the memory enable pin needs to be set in the FPGA (see Table 1-6). Table 1-9 defines the FMC Expansion Connector #1 pin assignments.

**Note**: The Flash memory and ZBT synchronous SRAM cannot be used when using FMC module #1. The FMC connector #1 has its own adjustable power supply to provide the appropriate voltage to the FPGA bank used to communicate with the FMC module. Be sure that the FMC adjustable power supply is configured for the voltage specified by the FMC module. See FMC expansion connector for instructions about how to configure the adjustable power supplies.

*Table 1-9:* **FMC #1 Expansion Connector Pin Assignments (1)**

| FMC Pin | FPGA Pin | Signal | FMC Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| C1 | NC | GND | D1 | M2 | PGC2M |
| C2 | NC | DP0C2MP | D2 | NC | GND |
| C3 | NC | DP0C2MN | D3 | NC | GND |
| C4 | NC | GND | D4 | NC | GBTCLK0M2CP |
| C5 | NC | GND | D5 | NC | GBTCLK0M2CN |
| C6 | NC | DP0M2CP | D6 | NC | GND |
| C7 | NC | DP0M2CN | D7 | NC | GND |
| C8 | NC | GND | D8 | P1 | 0_LA01_P_CC |
| C9 | NC | GND | D9 | P2 | 0_LA01_N_CC |
| C10 | L4 | 0_LA06_P | D10 | NC | GND |
| C11 | L3 | 0_LA06_N | D11 | D3 | 0_LA05_P |
| C12 | NC | GND | D12 | E4 | 0_LA05_N |
| C13 | NC | GND | D13 | NC | GND |

*Table 1-9:* **FMC #1 Expansion Connector Pin Assignments (1) *(Cont'd)***

| FMC Pin | FPGA Pin | Signal | FMC Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| C14 | K5 | 0_LA10_P | D14 | E3 | 0_LA09_P |
| C15 | K4 | 0_LA10_N | D15 | F4 | 0_LA09_N |
| C16 | NC | GND | D16 | NC | GND |
| C17 | NC | GND | D17 | K7 | 0_LA13_P |
| C18 | J5 | 0_LA14_P | D18 | J6 | 0_LA13_N |
| C19 | J4 | 0_LA14_N | D19 | NC | GND |
| C20 | NC | GND | D20 | N9 | 0_LA17_P_CC |
| C21 | NC | GND | D21 | P10 | 0_LA17_N_CC |
| C22 | K3 | 0_LA18_P | D22 | NC | GND |
| C23 | K2 | 0_LA18_N | D23 | N5 | 0_LA23_P |
| C24 | NC | GND | D24 | N4 | 0_LA23_N |
| C25 | NC | GND | D25 | NC | GND |
| C26 | T5 | 0_LA27_P | D26 | N1 | 0_LA26_P |
| C27 | U4 | 0_LA27_N | D27 | N2 | 0_LA26_N |
| C28 | NC | GND | D28 | NC | GND |
| C29 | NC | GND | D29 | A25 | TCK |
| C30 | AF23(1) | SCL | D30 | E23 | TDI |
| C31 | AE25(1) | SDA | D31 | NC | TDO |
| C32 | NC | GND | D32 | NC | 3P3VAUX |
| C33 | NC | GND | D33 | D4 | TMS |
| C34 | NC | GA0 (ground) | D34 | NC | TRSTL |
| C35 | NC | 12P0V | D35 | NC | GA1 (GND) |
| C36 | NC | GND | D36 | NC | 3P3V |
| C37 | NC | 12P0V | D37 | NC | GND |
| C38 | NC | GND | D38 | NC | 3P3V |
| C39 | NC | 3P3V | D39 | NC | GND |
| C40 | NC | GND | D40 | NC | 3P3V |

1. $I^2C$ bus connected to FPGA through $I^2C$ mux (U1). Mux needs to be configured for the proper channel

*Table 1-10:* **FMC #1 Expansion Connector Pin Assignments (2)**

| FMC Pin | FPGA Pin | Signal | FMC Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| G1 | NC | GND | H1 | NC | VREFAM2C |
| G2 | T3 | 0_CLK0_C2M_P | H2 | G1 | PRSNTM2CL |
| G3 | T4 | 0_CLK0_C2M_N | H3 | NC | GND |
| G4 | NC | GND | H4 | N6 | 0_CLK0_M2C_P |
| G5 | NC | GND | H5 | N7 | 0_CLK0_M2C_N |
| G6 | P4 | 0_LA00_P_CC | H6 | NC | GND |
| G7 | P3 | 0_LA00_N_CC | H7 | F5 | 0_LA02_P |
| G8 | NC | GND | H8 | G4 | 0_LA02_N |
| G9 | H2 | 0_LA03_P | H9 | NC | GND |
| G10 | H1 | 0_LA03_N | H10 | B2 | 0_LA04_P |
| G11 | NC | GND | H11 | B1 | 0_LA04_N |
| G12 | M8 | 0_LA08_P | H12 | NC | GND |
| G13 | M7 | 0_LA08_N | H13 | E1 | 0_LA07_P |
| G14 | NC | GND | H14 | F2 | 0_LA07_N |
| G15 | J7 | 0_LA12_P | H15 | NC | GND |
| G16 | H6 | 0_LA12_N | H16 | J8 | 0_LA11_P |
| G17 | NC | GND | H17 | J9 | 0_LA11_N |
| G18 | K9 | 0_LA16_P | H18 | NC | GND |
| G19 | K8 | 0_LA16_N | H19 | G3 | 0_LA15_P |
| G20 | NC | GND | H20 | F3 | 0_LA15_N |
| G21 | M4 | 0_LA20_P | H21 | NC | GND |
| G22 | M3 | 0_LA20_N | H22 | V1 | 0_LA19_P |
| G23 | NC | GND | H23 | V2 | 0_LA19_N |
| G24 | G6 | 0_LA22_P | H24 | NC | GND |
| G25 | H7 | 0_LA22_N | H25 | M10 | 0_LA21_P |
| G26 | NC | GND | H26 | M9 | 0_LA21_N |
| G27 | P7 | 0_LA25_P | H27 | NC | GND |
| G28 | P6 | 0_LA25_N | H28 | K6 | 0_LA24_P |
| G29 | NC | GND | H29 | L7 | 0_LA24_N |
| G30 | R5 | 0_LA29_P | H30 | NC | GND |
| G31 | R6 | 0_LA29_N | H31 | U1 | 0_LA28_P |
| G32 | NC | GND | H32 | U2 | 0_LA28_N |
| G33 | U5 | 0_LA31_P | H33 | NC | GND |