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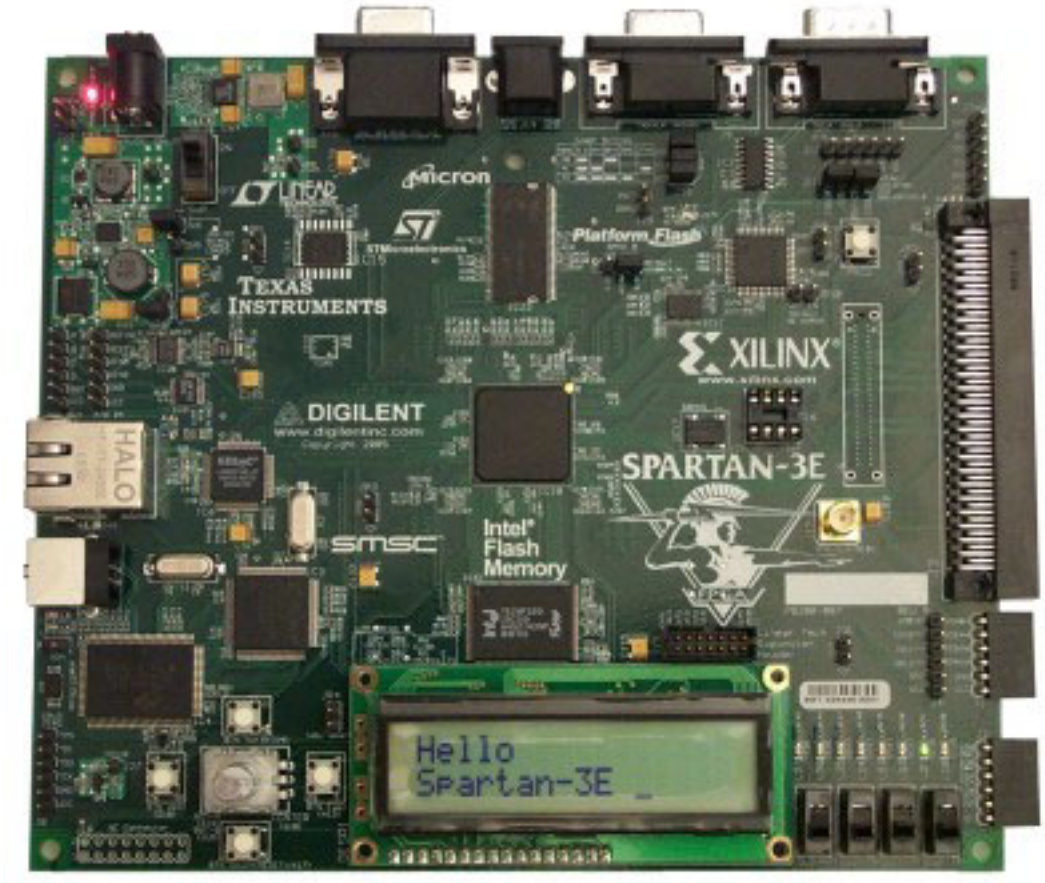
Spartan-3E FPGA Starter Kit Board User Guide

UG230 (v1.2) January 20, 2011



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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/09/06	1.0	Initial release.
06/20/08	1.1	Clarified DTE connections in Figure 7-1. Updated links.
01/20/11	1.2	Corrected Platform Flash disable polarity. Updated links.

Table of Contents

Chapter 4: FPGA Configuration Options

Chapter 5: Character LCD Screen

Appendix B: Example User Constraints File (UCF)

About This Guide

This user guide provides basic information on the Spartan-3E FPGA Starter Kit board capabilities, functions, and design. It includes general information on how to use the various peripheral functions included on the board. For detailed reference designs, including VHDL or Verilog source code, please visit the following web link.

- Spartan®-3E FPGA Starter Kit Board Reference Page
  http://www.xilinx.com/s3estarter

Acknowledgements

Xilinx wishes to thank the following companies for their support of the Spartan-3E FPGA Starter Kit board:

- Intel Corporation for the 128 Mbit StrataFlash memory
- Linear Technology for the SPI-compatible A/D and D/A converters, the programmable pre-amplifier, and the power regulators for the non-FPGA components
- Micron Technology, Inc. for the 32M x 16 DDR SDRAM
- SMSC for the 10/100 Ethernet PHY
- STMicroelectronics for the 16M x 1 SPI serial Flash PROM
- Texas Instruments Incorporated for the three-rail TPS75003 regulator supplying most of the FPGA supply voltages
- Xilinx, Inc. Configuration Solutions Division for the XCF04S Platform Flash PROM and their support for the embedded USB programmer
- Xilinx, Inc. for the XC2C64A CoolRunner™-II CPLD

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction and Overview," provides an overview of the key features of the Spartan-3E FPGA Starter Kit board.
- Chapter 2, "Switches, Buttons, and Knob," defines the switches, buttons, and knobs present on the Spartan-3E FPGA Starter Kit board.
- Chapter 3, "Clock Sources," describes the various clock sources available on the Spartan-3E FPGA Starter Kit board.
- Chapter 4, "FPGA Configuration Options," describes the configuration options for the FPGA on the Spartan-3E FPGA Starter Kit board.

- Chapter 5, "Character LCD Screen," describes the functionality of the character LCD screen.
- Chapter 6, "VGA Display Port," describes the functionality of the VGA port.
- Chapter 7, "RS-232 Serial Ports," describes the functionality of the RS-232 serial ports.
- Chapter 8, "PS/2 Mouse/Keyboard Port," describes the functionality of the PS/2 mouse and keyboard port.
- Chapter 9, "Digital to Analog Converter (DAC)," describes the functionality of the DAC.
- Chapter 10, "Analog Capture Circuit," describes the functionality of the A/D converter with a programmable gain pre-amplifier.
- Chapter 11, "Intel StrataFlash Parallel NOR Flash PROM," describes the functionality of the StrataFlash PROM.
- Chapter 12, "SPI Serial Flash," describes the functionality of the SPI Serial Flash memory.
- Chapter 13, "DDR SDRAM," describes the functionality of the DDR SDRAM.
- Chapter 14, "10/100 Ethernet Physical Layer Interface," describes the functionality of the 10/100Base-T Ethernet physical layer interface.
- Chapter 15, "Expansion Connectors," describes the various connectors available on the Spartan-3E FPGA Starter Kit board.
- Chapter 16, "XC2C64A CoolRunner-II CPLD" describes how the CPLD is involved in FPGA configuration when using Master Serial and BPI mode.
- Chapter 17, "DS2432 1-Wire SHA-1 EEPROM" provides a brief introduction to the SHA-1 secure EEPROM for authenticating or copy-protecting FPGA configuration bitstreams.
- Appendix A, "Schematics," lists the schematics for the Spartan-3E FPGA Starter Kit board.
- Appendix B, "Example User Constraints File (UCF)," provides example code from a UCF.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Chapter 1

Introduction and Overview

Thank you for purchasing the Xilinx Spartan®-3E FPGA Starter Kit. You will find it useful in developing your Spartan-3E FPGA application.

Choose the Starter Kit Board for Your Needs

Depending on specific requirements, choose the Xilinx development board that best suits your needs.

Spartan-3E FPGA Features and Embedded Processing Functions

The Spartan-3E Starter Kit board highlights the unique features of the Spartan-3E FPGA family and provides a convenient development board for embedded processing applications. The board highlights these features:

- Spartan-3E FPGA specific features
  - Parallel NOR Flash configuration
  - MultiBoot FPGA configuration from Parallel NOR Flash PROM
  - SPI serial Flash configuration
- Embedded development
  - MicroBlaze™ 32-bit embedded RISC processor
  - PicoBlaze™ 8-bit embedded controller
  - DDR memory interfaces

Advanced Spartan-3 Generation Development Boards

The Spartan-3E Starter Kit board demonstrates the basic capabilities of the MicroBlaze embedded processor and the Xilinx Embedded Development Kit (EDK). For more advanced development consider the capable boards offered by Xilinx partners:

- Spartan-3 Generation Board Interactive Search
  http://www.xilinx.com/products/boards_kits/spartan.htm

Key Components and Features

The key features of the Spartan-3E Starter Kit board are:

- Xilinx XC3S500E Spartan-3E FPGA
  - Up to 232 user-I/O pins
  - 320-pin FBGA package
  - Over 10,000 logic cells
- Xilinx 4 Mbit Platform Flash configuration PROM
- Xilinx 64-macrocell XC2C64A CoolRunner™ CPLD
- 64 MByte (512 Mbit) of DDR SDRAM, x16 data interface, 100+ MHz
- 16 MByte (128 Mbit) of parallel NOR Flash (Intel StrataFlash)
  - FPGA configuration storage
  - MicroBlaze code storage/shadowing
- 16 Mbits of SPI serial Flash (STMicro)
  - FPGA configuration storage
  - MicroBlaze code shadowing
- 2-line, 16-character LCD screen
- PS/2 mouse or keyboard port
- VGA display port
- 10/100 Ethernet PHY (requires Ethernet MAC in FPGA)
- Two 9-pin RS-232 ports (DTE- and DCE-style)
- On-board USB-based FPGA/CPLD download/debug interface
- 50 MHz clock oscillator
- SHA-1 1-wire serial EEPROM for bitstream copy protection
- Hirose FX2 expansion connector
- Three Digilent 6-pin expansion connectors
- Four-output, SPI-based Digital-to-Analog Converter (DAC)
- Two-input, SPI-based Analog-to-Digital Converter (ADC) with programmable-gain pre-amplifier
- ChipScope™ SoftTouch debugging port
- Rotary-encoder with push-button shaft
- Eight discrete LEDs
- Four slide switches
- Four push-button switches
- SMA clock input
- 8-pin DIP socket for auxiliary clock oscillator

Design Trade-Offs

A few system-level design trade-offs were required in order to provide the Spartan-3E Starter Kit board with the most functionality.

Configuration Methods Galore!

A typical FPGA application uses a single non-volatile memory to store configuration images. To demonstrate new Spartan-3E FPGA capabilities, the starter kit board has three different configuration memory sources that all need to function well together. The extra configuration functions make the starter kit board more complex than typical Spartan-3E FPGA applications.

The starter kit board also includes an on-board USB-based JTAG programming interface. The on-chip circuitry simplifies the device programming experience. In typical applications, the JTAG programming hardware resides off-board or in a separate programming module, such as the Xilinx Platform USB cable.

Voltages for all Applications

The Spartan-3E Starter Kit board showcases a triple-output regulator developed by Texas Instruments, the TPS75003 specifically to power Spartan-3 and Spartan-3E FPGAs. This regulator is sufficient for most stand-alone FPGA applications. However, the starter kit board includes DDR SDRAM, which requires its own high-current supply. Similarly, the USB-based JTAG download solution requires a separate 1.8V supply.

Related Resources

- Xilinx MicroBlaze Soft Processor
  http://www.xilinx.com/microblaze
- Xilinx PicoBlaze Soft Processor
  http://www.xilinx.com/picoblaze
- Xilinx Embedded Development Kit
  http://www.xilinx.com/tools/platform.htm
- Xilinx software tutorials
  http://www.xilinx.com/support/techsup/tutorials/
- Texas Instruments TPS75003
  http://focus.ti.com/docs/prod/folders/print/tps75003.html

Chapter 2

Switches, Buttons, and Knob

Slide Switches

Locations and Labels

The Spartan®-3E FPGA Starter Kit board has four slide switches, as shown in Figure 2-1. The slide switches are located in the lower right corner of the board and are labeled SW3 through SW0. Switch SW3 is the left-most switch, and SW0 is the right-most switch.

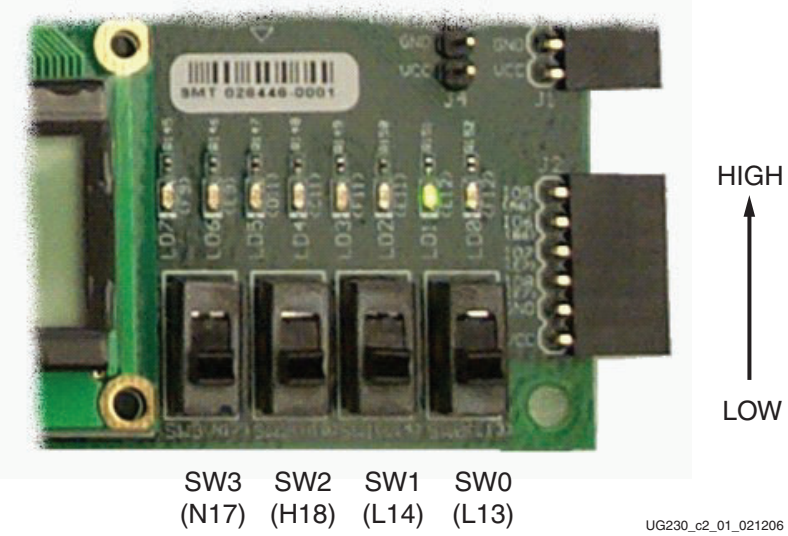


Figure 2-1: **Four Slide Switches**

Operation

When in the UP or ON position, a switch connects the FPGA pin to 3.3V, a logic High. When DOWN or in the OFF position, the switch connects the FPGA pin to ground, a logic Low. The switches typically exhibit about 2 ms of mechanical bounce and there is no active debouncing circuitry, although such circuitry could easily be added to the FPGA design programmed on the board.

UCF Location Constraints

Figure 2-2 provides the UCF constraints for the four slide switches, including the I/O pin assignment and the I/O standard used. The PULLUP resistor is not required, but it defines the input value when the switch is in the middle of a transition.

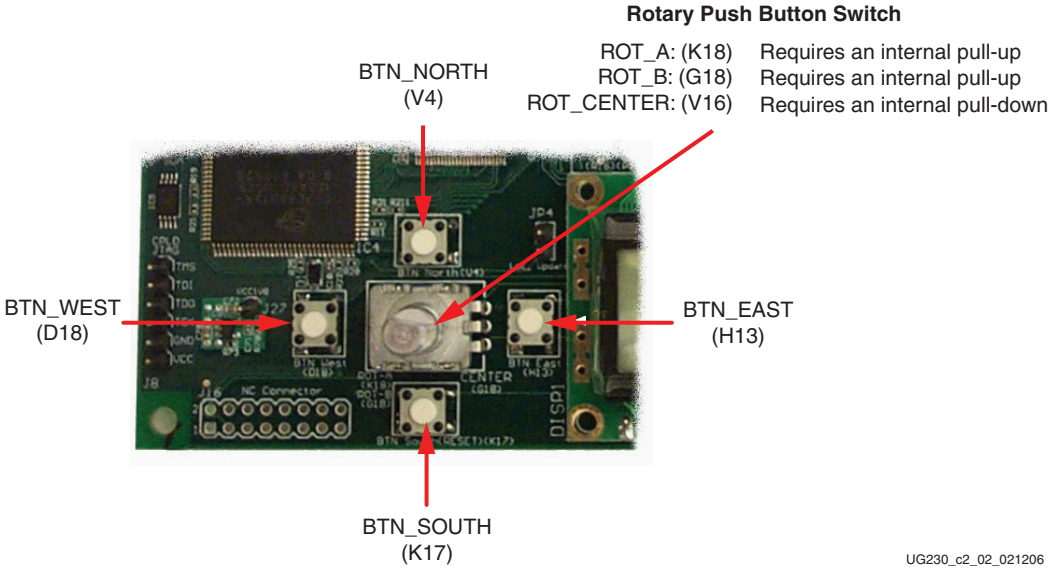
```
NET "SW<0>" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<1>" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<2>" LOC = "H18" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<3>" LOC = "N17" | IOSTANDARD = LVTTL | PULLUP ;
```

Figure 2-2: **UCF Constraints for Slide Switches**

Push-Button Switches

Locations and Labels

The Spartan-3E FPGA Starter Kit board has four momentary-contact push-button switches, shown in Figure 2-3. The push buttons are located in the lower left corner of the board and are labeled BTN_NORTH, BTN_EAST, BTN_SOUTH, and BTN_WEST. The FPGA pins that connect to the push buttons appear in parentheses in Figure 2-3 and the associated UCF appears in Figure 2-5.



Notes:

1. All BTN_* push-button inputs require an internal pull-down resistor.
2. BTN_SOUTH is also used as a soft reset in some FPGA applications.

Figure 2-3: **Four Push-Button Switches Surround Rotary Push-Button Switch**

Operation

Pressing a push button connects the associated FPGA pin to 3.3V, as shown in Figure 2-4. Use an internal pull-down resistor within the FPGA pin to generate a logic Low when the button is not pressed. Figure 2-5 shows how to specify a pull-down resistor within the UCF. There is no active debouncing circuitry on the push button.

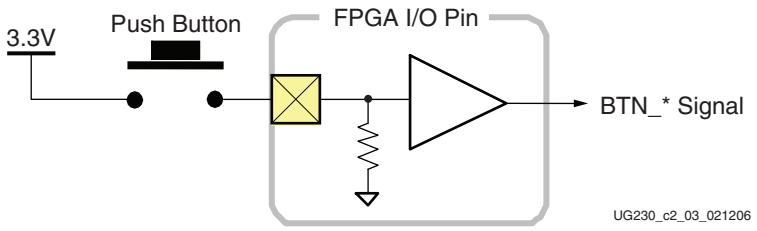


Figure 2-4: **Push-Button Switches Require an Internal Pull-Down Resistor in FPGA Input Pin**

In some applications, the BTN_SOUTH push-button switch is also a soft reset that selectively resets functions within the FPGA.

UCF Location Constraints

Figure 2-5 provides the UCF constraints for the four push-button switches, including the I/O pin assignment and the I/O standard used, and defines a pull-down resistor on each input.

```
NET "BTN_EAST"  LOC = "H13" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_NORTH" LOC = "V4"  | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_SOUTH" LOC = "K17" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_WEST"  LOC = "D18" | IOSTANDARD = LVTTL | PULLDOWN ;
```

Figure 2-5: **UCF Constraints for Push-Button Switches**

Rotary Push-Button Switch

Locations and Labels

The rotary push-button switch is located in the center of the four individual push-button switches, as shown in Figure 2-3. The switch produces three outputs. The two shaft encoder outputs are ROT_A and ROT_B. The center push-button switch is ROT_CENTER.

Operation

The rotary push-button switch integrates two different functions. The switch shaft rotates and outputs values whenever the shaft turns. The shaft can also be pressed, acting as a push-button switch.

Push-Button Switch

Pressing the knob on the rotary/push-button switch connects the associated FPGA pin to 3.3V, as shown in Figure 2-6. Use an internal pull-down resistor within the FPGA pin to generate a logic Low. Figure 2-9 shows how to specify a pull-down resistor within the UCF. There is no active debouncing circuitry on the push button.

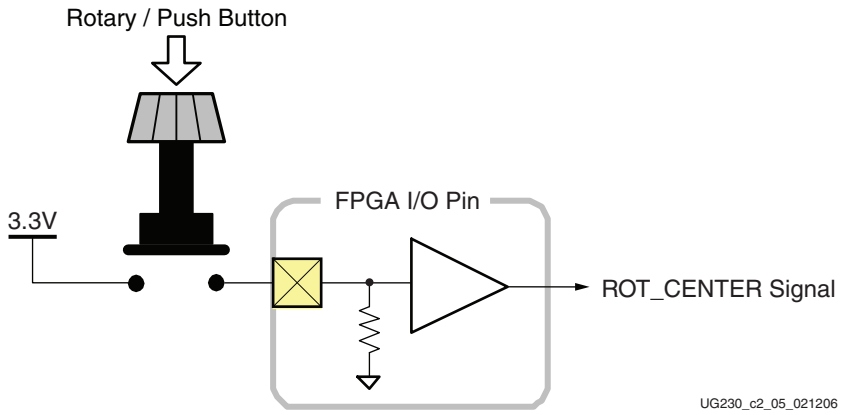


Figure 2-6: **Push-Button Switches Require Internal Pull-up Resistor in FPGA Input Pin**

Rotary Shaft Encoder

In principal, the rotary shaft encoder behaves much like a cam, connected to central shaft. Rotating the shaft then operates two push-button switches, as shown in Figure 2-7. Depending on which way the shaft is rotated, one of the switches opens before the other. Likewise, as the rotation continues, one switch closes before the other. However, when the shaft is stationary, also called the *detent* position, both switches are closed.

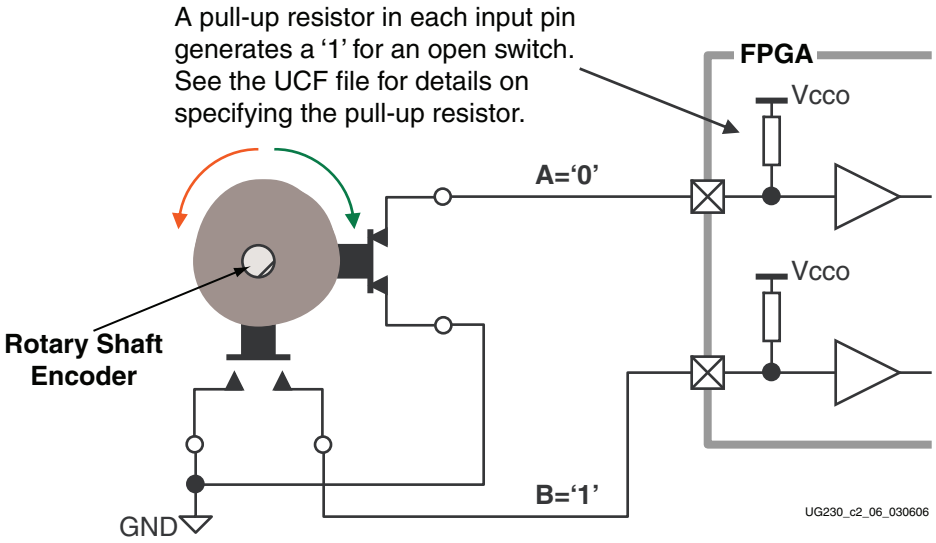


Figure 2-7: **Basic example of rotary shaft encoder circuitry**

Closing a switch connects it to ground, generating a logic Low. When the switch is open, a pull-up resistor within the FPGA pin pulls the signal to a logic High. The UCF constraints in Figure 2-9 describe how to define the pull-up resistor.

The FPGA circuitry to decode the 'A' and 'B' inputs is simple, but must consider the mechanical switching noise on the inputs, also called chatter. As shown in Figure 2-8, the chatter can falsely indicate extra rotation events or even indicate rotations in the opposite

direction! See the Rotary Encoder Interface reference design in"Related Resources" for an example.

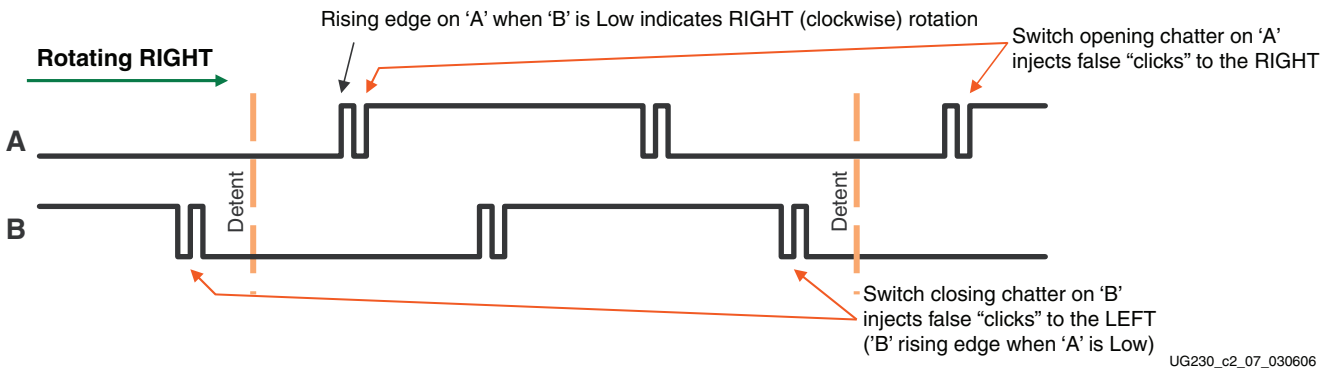


Figure 2-8: **Outputs from Rotary Shaft Encoder May Include Mechanical Chatter**

UCF Location Constraints

Figure 2-9 provides the UCF constraints for the four push-button switches, including the I/O pin assignment and the I/O standard used, and defines a pull-down resistor on each input.

```
NET "ROT_A"      LOC = "K18" | IOSTANDARD = LVTTL | PULLUP   ;
NET "ROT_B"      LOC = "G18" | IOSTANDARD = LVTTL | PULLUP   ;
NET "ROT_CENTER" LOC = "V16" | IOSTANDARD = LVTTL | PULLDOWN ;
```

Figure 2-9: **UCF Constraints for Rotary Push-Button Switch**

Discrete LEDs

Locations and Labels

The Spartan-3E FPGA Starter Kit board has eight individual surface-mount LEDs located above the slide switches as shown in Figure 2-10. The LEDs are labeled LED7 through LED0. LED7 is the left-most LED, LED0 the right-most LED.

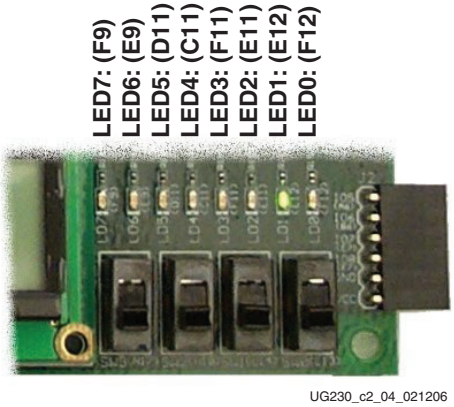


Figure 2-10: **Eight Discrete LEDs**

Operation

Each LED has one side connected to ground and the other side connected to a pin on the Spartan-3E device via a 390Ωcurrent limiting resistor. To light an individual LED, drive the associated FPGA control signal High.

UCF Location Constraints

Figure 2-11 provides the UCF constraints for the four push-button switches, including the I/O pin assignment, the I/O standard used, the output slew rate, and the output drive current.

```
NET "LED<7>" LOC = "F9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<6>" LOC = "E9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<5>" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<4>" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<3>" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<2>" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<1>" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<0>" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
```

Figure 2-11: **UCF Constraints for Eight Discrete LEDs**

Related Resources

- Rotary Encoder Interface for Spartan-3E Starter Kit (Reference Design)
  http://www.xilinx.com/s3estarter

Chapter 3

Clock Sources

Overview

As shown in Figure 3-1, the Spartan®-3E FPGA Starter Kit board supports three primary clock input sources, all of which are located below the Xilinx logo, near the Spartan-3E logo.

- The board includes an on-board 50 MHz clock oscillator.
- Clocks can be supplied off-board via an SMA-style connector. Alternatively, the FPGA can generate clock signals or other high-speed signals on the SMA-style connector.
- Optionally install a separate 8-pin DIP-style clock oscillator in the supplied socket.

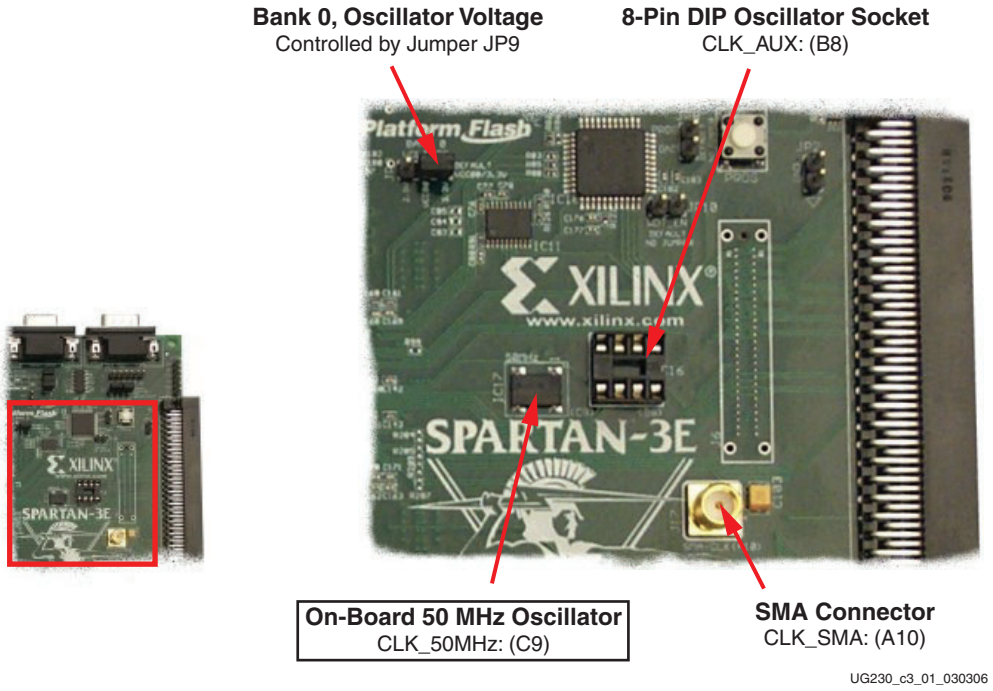


Figure 3-1: **Available Clock Inputs**

Clock Connections

Each of the clock inputs connect directly to a global buffer input in I/O Bank 0, along the top of the FPGA. As shown in Table 3-1, each of the clock inputs also optimally connects to an associated DCM.

Table 3-1: **Clock Inputs and Associated Global Buffers and DCMs**

Clock Input	FPGA Pin	Global Buffer	Associated DCM
CLK_50MHZ	C9	GCLK10	DCM_X0Y1
CLK_AUX	B8	GCLK8	DCM_X0Y1
CLK_SMA	A10	GCLK7	DCM_X1Y1

Voltage Control

The voltage for all I/O pins in FPGA I/O Bank 0 is controlled by jumper JP9. Consequently, these clock resources are also controlled by jumper JP9. By default, JP9 is set for 3.3V. The on-board oscillator is a 3.3V device and might not perform as expected when jumper JP9 is set for 2.5V.

50 MHz On-Board Oscillator

The board includes a 50 MHz oscillator with a 40% to 60% output duty cycle. The oscillator is accurate to ±2500 Hz or ±50 ppm.

Auxiliary Clock Oscillator Socket

The provided 8-pin socket accepts clock oscillators that fit the 8-pin DIP footprint. Use this socket if the FPGA application requires a frequency other than 50 MHz. Alternatively, use the FPGA's Digital Clock Manager (DCM) to generate or synthesize other frequencies from the on-board 50 MHz oscillator.

SMA Clock Input or Output Connector

To provide a clock from an external source, connect the input clock signal to the SMA connector. The FPGA can also generate a single-ended clock output or other high-speed signal on the SMA clock connector for an external device.

UCF Constraints

The clock input sources require two different types of constraints. The location constraints define the I/O pin assignments and I/O standards. The period constraints define the clock period—and consequently the clock frequency—and the duty cycle of the incoming clock signal.

Location

Figure 3-2 provides the UCF constraints for the three clock input sources, including the I/O pin assignment and the I/O standard used. The settings assume that jumper JP9 is set for 3.3V. If JP9 is set for 2.5V, adjust the IOSTANDARD settings accordingly.

```
NET "CLK_50MHZ" LOC = "C9"  | IOSTANDARD = LVCMOS33 ;
NET "CLK_SMA"   LOC = "A10" | IOSTANDARD = LVCMOS33 ;
NET "CLK_AUX"   LOC = "B8"  | IOSTANDARD = LVCMOS33 ;
```

Figure 3-2: **UCF Location Constraints for Clock Sources**

Clock Period Constraints

The Xilinx ISE® development software uses timing-driven logic placement and routing. Set the clock PERIOD constraint as appropriate. An example constraint appears in Figure 3-3 for the on-board 50 MHz clock oscillator. The CLK_50MHZ frequency is 50 MHz, which equates to a 20 ns period. The output duty cycle from the oscillator ranges between 40% to 60%.

```
# Define clock period for 50 MHz oscillator
NET "CLK_50MHZ" PERIOD = 20.0ns HIGH 40%;
```

Figure 3-3: **UCF Clock PERIOD Constraint**

Related Resources

- Epson SG-8002JF Series Oscillator Data Sheet (50 MHz Oscillator)

Chapter 4

FPGA Configuration Options

The Spartan®-3E FPGA Starter Kit board supports a variety of FPGA configuration options:

- Download FPGA designs directly to the Spartan-3E FPGA via JTAG, using the on-board USB interface. The on-board USB-JTAG logic also provides in-system programming for the on-board Platform Flash PROM and the Xilinx XC2C64A CPLD. SPI serial Flash and StrataFlash programming are performed separately.
- Program the on-board 4 Mbit Xilinx XCF04S serial Platform Flash PROM, then configure the FPGA from the image stored in the Platform Flash PROM using Master Serial mode.
- Program the on-board 16 Mbit ST Microelectronics SPI serial Flash PROM, then configure the FPGA from the image stored in the SPI serial Flash PROM using SPI mode.
- Program the on-board 128 Mbit Intel StrataFlash parallel NOR Flash PROM, then configure the FPGA from the image stored in the Flash PROM using BPI Up or BPI Down configuration modes. Further, an FPGA application can dynamically load two different FPGA configurations using the Spartan-3E FPGA's MultiBoot mode. See the Spartan-3E data sheet (DS312) for additional details on the MultiBoot feature.

Figure 4-1 indicates the position of the USB download/programming interface and the on-board non-volatile memories that potentially store FPGA configuration images.Figure 4-2 provides additional details on configuration options.