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ML410 Embedded Development Platform

User Guide

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XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/06/06	1.0	Initial Xilinx release.
02/10/06	1.1	Corrected pinouts in Table 2-20, page 53.
05/26/06	1.2	Corrected pinouts in Table 2-5, page 33 and Table 2-21, page 54. Expanded “PCI Express” section.
09/25/06	1.2.1	Updated PHY address in Table 2-7, page 38 and Table 2-9, page 41. Miscellaneous typographical edits.
10/26/06	1.3	Updated “Clock Generation,” page 26, “Serial ATA,” page 73, and “High-Speed I/O,” page 84 for RoHS-compliant revision E boards. Added Appendix A, “Board Revisions.”
11/01/06	1.4	Corrected Table 2-19, page 51.
12/22/06	1.5	Added note to “RocketIO Transceivers,” page 17. Added board revision details to Table A-1, page 97.
03/06/07	1.6	Updated Table 2-19, page 51 and Table A-1, page 97.
04/06/07	1.6.1	Fixed typo in Figure 2-19, page 71.
09/28/07	1.7	Corrected pinouts in Table 2-15, page 46 for SYSACE_FPGA_CLK, SYSACE_MPD[15], SYSACE_MPCE, and SYSACE_MPWE signals.
03/05/08	1.7.1	Fixed typo in Table 2-8, page 40. Updated trademark statements and copyright date.
12/11/08	1.7.2	Minor edits to Table A-1, page 97. Removed support for unbuffered DIMMs.

Table of Contents

Appendix A: Board Revisions

Appendix B: References

Schedule of Figures

Chapter 1: Introduction to Virtex-4, ISE, and EDK

Chapter 2: ML410 Embedded Development Platform

Appendix A: Board Revisions

Appendix B: References

Schedule of Tables

Chapter 1: Introduction to Virtex-4, ISE, and EDK

Chapter 2: ML410 Embedded Development Platform

Appendix A: Board Revisions

Appendix B: References

About This Guide

This manual accompanies the ML410 series of Embedded Development Platforms and contains information about the ML410 hardware and software tools.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction to Virtex-4, ISE, and EDK," provides an overview of the hardware and software features
- Chapter 2, "ML410 Embedded Development Platform," provides an overview of the embedded development platform and details the components and features of the ML410 board
- Appendix A, "Board Revisions" details the differences between board revisions in the ML410 series
- Appendix B, "References"

Additional Resources

To find additional documentation, see the Xilinx® website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets `[ ]`	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** `[option_name]` *`design_name`*
Braces `{ }`	A list of items from which you must choose one or more	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`
Vertical bar `|`	Separates items in a list of choices	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis `...`	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.

Convention	Meaning or Use	Example
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Platform FPGA User Guide.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Chapter 1

Introduction to Virtex-4, ISE, and EDK

Virtex-4 FPGAs

Virtex®-4 domain-optimized FPGAs provide an ideal mix of features and the greatest choice of devices of any FPGA product line on the market today, with a column-based architecture unique to the programmable logic industry. Virtex-4 FPGAs contain three platforms: LX, FX, and SX. Choice and feature combinations are offered for all complex applications. A wide array of hard-IP core blocks complete the system solution. These cores include the PowerPC® processors (with a new APU interface), Tri-Mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks. The basic Virtex-4 building blocks allow migration of existing Virtex series designs. Virtex-4 devices are produced by a state-of-the-art 90 nm copper process, using 300 mm (12 inch) wafer technology. Combining a wide variety of flexible features, the Virtex-4 family enhances programmable logic design capabilities and is a powerful alternative to ASIC technology.

Summary of Virtex-4 FX Features

The Virtex-4 family has an impressive collection of both programmable logic and hard IP, historically the domain of ASICs. The Virtex-4 FX FPGAs used on ML410 platforms are high-performance, full-featured solutions for embedded platform applications.

- Xesium™ clock technology
  - Digital clock manager (DCM) blocks
  - Additional phase-matched clock dividers (PMCD)
  - Differential global clocks
- XtremeDSP™ slice
  - 18 x 18, two's complement, signed multiplier
  - Optional pipeline stages
  - Built-in accumulator (48-bits) and adder/subtracter
- Smart RAM memory hierarchy
  - Distributed RAM
  - Dual-port 18 Kb RAM blocks
    - Optional pipeline stages
    - Optional programmable FIFO logic - Automatically remaps RAM signals as FIFO signals
  - High-speed memory interface support: DDR and DDR2
- SDRAM, QDR II, RLDRAM II, and FCRAM II SelectIO technology
  - 1.5V to 3.3V I/O operation

  - Built-in ChipSync™ source-synchronous technology
  - Digitally-controlled impedance (DCI) active termination
  - Fine grained I/O banking (configuration in one bank)
- Flexible logic resources
- Secure Chip AES bitstream encryption
- 90 nm copper CMOS process
- 1.2V core voltage
- Flip-Chip packaging
- RocketIO™ 622 Mb/s to 6.5 Gb/s multi-gigabit transceivers (MGT)
- IBM PowerPC RISC processor core
  - PowerPC 405 (PPC405) core
  - Auxiliary processor unit interface (user coprocessor)
- Multiple Tri-Mode Ethernet MACs

Table 1-1: **Virtex-4 FX Family Members**

Device	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
Logic Cells	12,312	19,224	41,904	56,880	94,896	142,128
PPC405	1	1	2	2	2	2
MGTs	N/A	8	12	16	20	24
Block RAM (Kb)	648	1,224	2,592	4,176	6,768	9,936
XtremeDSP Multipliers	32	32	48	128	160	192

PowerPC™ 405 Core

- 32-bit Harvard architecture core
- Five-stage execution pipeline
- Integrated 16 KB level 1 instruction cache and 16 KB level 1 data cache
  - Integrated level 1 cache parity generation and checking
- CoreConnect™ bus architecture
- Efficient, high-performance on-chip memory (OCM) interface to block RAM
- PLB synchronization logic (enables non-integer CPU-to-PLB clock ratios)
- Auxiliary Processor Unit (APU) interface and integrated APU controller
  - Optimized FPGA-based coprocessor connection
  - Automatic decode of PowerPC floating-point instructions
  - Allows custom instructions (decode for up to eight instructions)
  - Extremely efficient microcontroller-style interfacing

RocketIO Transceivers

- Full-duplex serial transceiver (SERDES) capable of running 622 Mb/s - 6.5 Gb/s

  Note: Only Revision E boards support 6.5 Gb/s. See Appendix A, "Board Revisions" for more details.
- Full clock and data recovery
- 32-bit or 40-bit datapath support
- Optional 8B/10B, 64B/66B, or FPGA-based encode/decode
- Integrated FIFO/elastic buffer
- Support for channel bonding
- Embedded 32-bit CRC generation/checking
- Integrated comma-detect or programmable A1/A2, A1A1/A2A2 detection
- Programmable pre-emphasis (AKA transmitter equalization)
- Programmable receiver equalization
- Embedded support for:
  - Out of band (OOB) signaling: Serial ATA
  - Beaconing and electrical idle: PCI Express®
- On-chip bypassable AC coupling for receiver

ISE Foundation

ISE Foundation is the industry's most complete programmable logic design environment. With ISE Foundation, you have everything you need to target today's most advanced CPLDs and FPGAs, including the new Virtex-4 family of FPGAs. ISE Foundation includes the industry's most advanced timing driven implementation tools available for programmable logic design, along with design entry, synthesis and verification capabilities. With its ultra-fast runtimes, an average 40% faster than the nearest competitive FPGA offering, ProActive Timing Closure technologies, and seamless integration with the industry's most advanced verification products, ISE Foundation offers a great design environment in which to create a complete programmable logic design solution.

Foundation Features

Design Entry

ISE greatly improves time-to-market, productivity, and design quality with robust design entry features. ISE provides support for today's most popular methods for design capture including HDL and schematic entry, integration of IP cores, and robust support for reuse of your own IP.

ISE's architecture wizards allow easy access to device features like the DCM and multi-gigabit I/O technology.

ISE also includes a tool called PACE (Pinout Area Constraint Editor) that includes a front-end pin assignment editor, a design hierarchy browser, and an area constraint editor. By using PACE, designers are able to observe and describe information regarding the connectivity and resource requirements of a design, resource layout of a target FPGA, and the mapping of the design onto the FPGA via location/area.

This rich mixture of design entry capabilities provides the easiest to use design environment available today for your logic design.

Synthesis

Synthesis is one of the most essential steps in your design methodology. It takes your conceptual Hardware Description Language (HDL) design definition and generates the logical or physical representation for the targeted silicon device.

A state-of-the-art synthesis engine is required to produce highly optimized results with a fast compile and turnaround time. To meet this requirement, the synthesis engine needs to be tightly integrated with the physical implementation tool and have the ability to proactively meet the design timing requirements by driving the placement in the physical device. In addition, cross probing between the physical design report and the HDL design code further improves the turnaround time.

Xilinx ISE provides the seamless integration with the leading synthesis engines from Mentor Graphics, Synopsys, and Synplicity. You can use the synthesis engine of our choice. In addition, ISE includes Xilinx proprietary synthesis technology, XST. You have options to use multiple synthesis engines to obtain the best-optimized result of your programmable logic design.

Implementation and Configuration

Programmable logic design implementation assigns the logic created during design entry and synthesis into specific physical resources of the target device.

The term “place and route” has historically been used to describe the implementation process for FPGA devices and “fitting” has been used for CPLDs. Implementation is followed by device configuration, where a bitstream is generated from the physical place and route information and downloaded into the target programmable logic device.

To ensure designers get their product to market quickly, Xilinx ISE software provides several key technologies required for design implementation:

- Ultra-fast runtimes enable multiple “turns” per day
- ProActive™ Timing Closure drives high-performance results
- Timing-driven place and route combined with pushbutton ease
- Incremental Design

Board-Level Integration

Xilinx understands the critical issues such as complex board layout, signal integrity, high-speed bus interface, high-performance I/O bandwidth, and electromagnetic interference for system-level designers.

To ease the system level designers' challenge, ISE provides support to all Xilinx leading FPGA technologies:

- System IO
- XCITE
- Digital clock management for system timing
- EMI control management for electromagnetic interference

To ensure that your programmable logic design works in the context of your entire system, Xilinx provides complete pin configurations, packaging information, tips on signal integration, and various simulation models for your board-level verification including:

- IBIS models
- HSPICE models
- STAMP models

Embedded Development Kit

The Embedded Development Kit (EDK) is a series of software tools for designing embedded processor systems on programmable logic and supports the IBM PowerPC hard processor core and the MicroBlaze™ soft processor core. This pre-configured kit includes the Platform Studio Tool Suite.

EDK Components

The Embedded Development Kit is distributed as a single media installable CD image.

The components of the Xilinx EDK are:

- Hardware IP for the Xilinx embedded processors and its peripherals
- Drivers, libraries, and a microkernel for embedded software development
- Platform Studio tools
- Software Development Kit (Eclipse-based IDE)
- GNU compiler and debugger for C development for MicroBlaze and PowerPC
- Documentation
- Sample projects

Platform Studio Features

The Xilinx Platform Studio (XPS) is a graphical user interface technology that integrates all of the processes from design entry to design debug and verification. XPS streamlines development with the embedded features of the Xilinx Virtex-4 FX family of devices, featuring the industry's only immersed dual PowerPC processors and innovative Auxiliary Processor Unit (APU) controller for accelerating processing functions.

XPS automates the configuration of user-defined hardware co-processing modules used to replace application-specific software algorithms. These hardware accelerator functions operate as extensions to the PowerPC 405 processor, thereby offloading the CPU from demanding computational tasks. Utilizing the direct processor-FPGA coupling presented by the APU controller and its high throughput interfaces, flexible design partitioning with synchronization of hardware and software is greatly simplified and overall system performance is improved. The suite also includes system profiling and analysis tools to help optimize performance and target design functions for acceleration in FPGA hardware.

Chapter 2

ML410 Embedded Development Platform

Overview

The ML410 series of Embedded Development Platforms offer designers a versatile Virtex-4 FX platform for rapid prototyping and system verification. In addition to the more than 30,000 logic cells, over 2,400 kb of block RAM, dual IBM PowerPC 405 (PPC405) processors, and RocketIO transceivers available in the FPGA, the ML410 provides an onboard Ethernet MAC PHY, DDR memory, multiple PCI bus slots, and standard front panel interface ports within an ATX form factor motherboard. An integrated System ACE™ CompactFlash (CF) controller is deployed to perform board bring-up and to load applications from the CompactFlash card.

The ML410 website contains up-to-date documentation and files, including tutorials, device data sheets, reference designs, and utilities. The EDK *Processor IP User Guide* [Ref 2] should be reviewed as well as the data sheets corresponding to the devices listed in "Detailed Description."

The setup and quickstart documentation highlights the functionality of the ML410, using the applications contained on the CompactFlash card. The reference designs were produced using the Xilinx Embedded Development Kit (EDK), ISE, and Answer Browser solution records. Tutorials, in coordination with Xilinx documentation for EDK, ISE, and the Answer Browser, describe how the reference designs and applications were produced. These tutorials can be used to re-create the provided applications and also as a basis for the development of new designs. Xilinx EDK provides for the development of basic board-specific systems, beginning with Base System Builder (BSB), to highly customized systems that leverage the flexibility of Xilinx Platform Studio (XPS) and the EDK intellectual property (IP).

Features

The list below is a superset of features in the ML410 series. Appendix A, "Board Revisions" describes the differences between the ML410-P and ML410 model boards.

- ATX form factor motherboard and ATX-compliant power supply
- 32-bit component DDR memory and 64-bit DDR2 DIMM*
- 512 MB CompactFlash (CF) card and System ACE CF controller for configuration*
- Two onboard 10/100/1000 Ethernet PHYs with RJ-45 connectors
- PCI Express interface and MIC2592B PCI Express power controller
- Two UARTs with RS-232 connectors
- VGA graphics interface

- LEDs, LCD*, and switches
- 32/33 PCI subsystem
  - Two 3.3V slots and two 5V slots
  - ALi South Bridge SuperIO controller
    - PS/2 mouse and keyboard connectors
    - 3.5mm headphone and microphone connectors
    - Two USB peripheral ports and one parallel port
    - General purpose I/O (GPIO)
    - Flash memory interface
- Two serial ATA connectors
- Xilinx Personality Module (XPM) interface for access to:
  - RocketIO transceivers
  - SPI4.2
  - GPIO
  - Power
- JTAG and trace debug ports
- Encryption battery
- Fan controller
- Onboard power regulators for all necessary voltages
- IIC/SMBus interface*
  - LTC1694 SMBus accelerator
  - RTC8566 Real Time Clock (RTC)
  - 64 kb 24LC64 EEPROM
  - LM87 voltage/temp monitor
  - DDR2 DIMM SPD EEPROM
- SPI EEPROM*
- High-speed I/O through RocketIO transceivers

Note: * Compatible with EDK supported IP and software drivers

Block Diagram

Figure 2-1 shows a high-level block diagram of the ML410 and its peripherals.

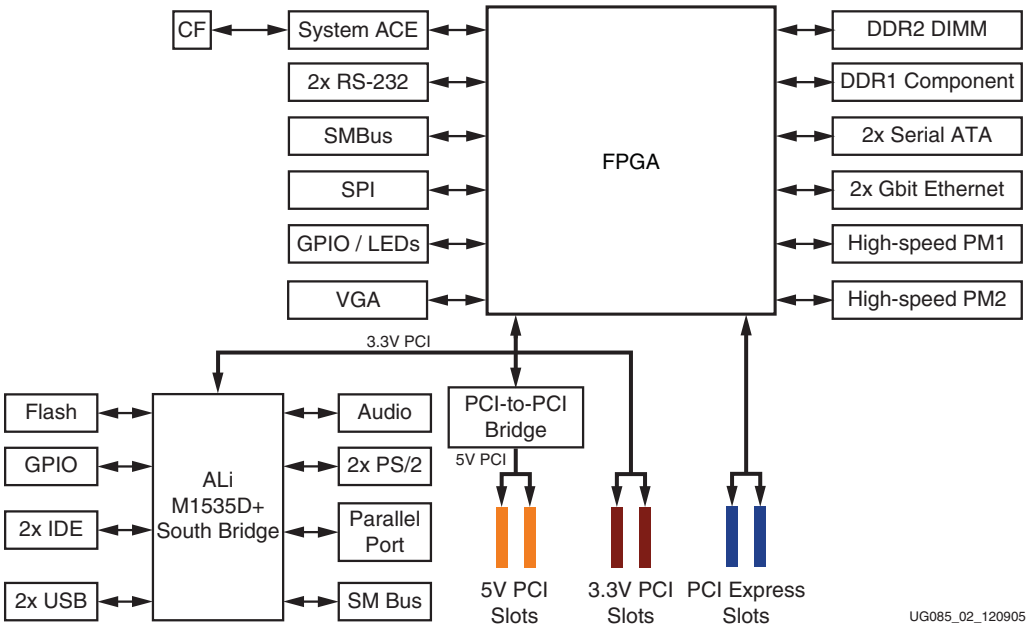

Figure 2-1: **ML410 High-Level Block Diagram**

Related Xilinx Documents

Prior to using the ML410 Embedded Development Platform, users should be familiar with Xilinx resources. See Appendix B, "References" for direct links to Xilinx documentation. See the following locations for additional documentation on Xilinx tools and solutions:

- EDK: www.xilinx.com/edk
- ISE: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Virtex-4 FPGAs: www.xilinx.com/virtex-4

Detailed Description

The ML410, shown in Figure 2-2, is an example of the ML410 series described in this user guide.

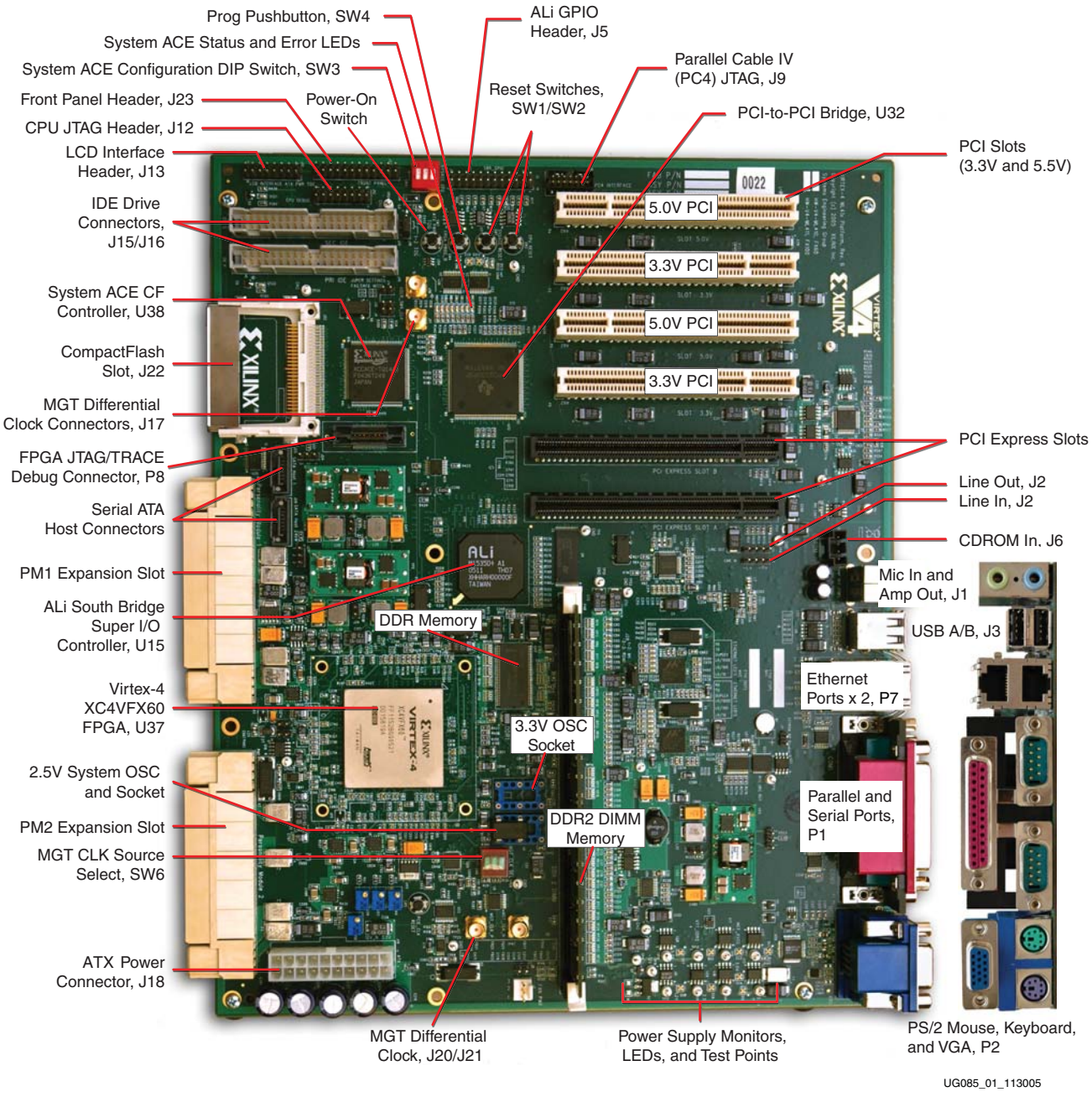

Figure 2-2: **ML410 Board and Front Panel Detail**

Configuration

ML410 platforms support configuration in JTAG mode only. Configuration can be accomplished by using a Xilinx download cable (such as Parallel Cable IV or Platform Cable USB) or by using the onboard System ACE CompactFlash solution. See "System ACE CF Controller," page 44.

I/O Voltage Rails

The FPGA requires different banking voltages that are set based on the I/O voltage interface requirements of each device directly connected to the FPGA. The Virtex-4 FPGA I/O can be configured to use different I/O standards such as SSTL18 as required on the DDR2 DIMM interface. See the *Virtex-4 Data Sheet* [Ref 3] for more information regarding I/O standards.

The voltage applied to the FPGA I/O banks used by the ML410 platforms is summarized in Table 2-1.

Table 2-1: **I/O Voltage Rail of FPGA Banks**

FPGA Bank	I/O Voltage Rail	Description
1	2.5V	PCI Express controls and DDR1
2	2.5V	LCD and SPI
3	2.5V	Clocks and miscellaneous signals
4	2.5V	Clocks and miscellaneous signals
5	2.5V	DDR
6	3.0V	VGA, PHY, and both UARTs
7	2.5V	PMIO, CPU debug, and ATD
8	2.5V	PMIO and trace port
9	1.8V	DDR2
10	3.0V	PCI
11	1.8V	DDR2
12	3.0V	System ACE, PMIO_3V, and LEDs **Note:** User selectable as 3.0V (default) or 2.5V. See schematic sheet 46 (R486–R488 and R489–R491).

Digitally Controlled Impedance (DCI)

Some FPGA banks can support the DCI feature in Virtex-4 FPGAs. Support for DCI is summarized in Table 2-2.

Table 2-2: **DCI Capability of FPGA Bank**

FPGA Bank	DCI Capability	FPGA Bank	DCI Capability
1	Not supported.	7	Yes, 49.9Ω resistors are installed.
2	Not supported.	8	Yes, 49.9Ω resistors are installed.
3	Not supported.	9	Yes, 49.9Ω resistors are installed.