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Video Starter Kit

User Guide

UG217 (v1.5) October 26, 2006

XILINX®

Revision History

Video Starter Kit
UG217 (v1.5) October 26, 2006

The following table shows the revision history for this document.

Date	Version	Revision
12/22/05	1.0	Initial Xilinx release.
02/13/06	1.1	Edits throughout the document.
03/14/06	1.2	Minor edits in Chapter 6. Replaced Figure 6-5.
06/27/06	1.3	Minor edits.
10/10/06	1.4	Edits and additions to Chapter 5, “VSK Diagnostics and Support Tool Kit” and Chapter 7, “Compiling the VIODC FPGA Design.”
10/26/06	1.5	Updated Figure 5-6 and Figure 5-9. Added new Table 5-5.

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About This Guide

This user guide provides a description of the Video Starter Kit (VSK) contents, features, hardware, and software. The Video Starter Kit hardware consists of a ML402 FPGA development platform with a Video Input and Output Daughter Card (VIODC) and an LVDS video camera. The Video Starter Kit can be used with System Generator to develop EDK processing cores that process live video streams.

Guide Contents

This user guide contains the following chapters:

- Chapter 1, "Video Starter Kit Overview" – provides a kit overview with a brief description of the ML402 development platform, the VIODC, and the LVDS video camera.
- Chapter 2, "Developing Video Applications In System Generator" – The Video Starter Kit provides for both simulation and real-time operation for each of the components in a video system.
- Chapter 3, "EDK Integration" – details the design-flow for incorporating a MicroBlaze™ processor into MVI framework. In particular, it describes using the EDK processor block in System Generator and the automatically generated software drivers to read and write data to the System Generator design.
- Chapter 4, "Hardware Co-Simulation"– provides a description of the hardware co-simulation interfaces that make it possible to compile a System Generator diagram into an FPGA bitstream and associate this bitstream with a new run-time hardware co-simulation block.
- Chapter 5, "VSK Diagnostics and Support Tool Kit"– describes how the VSK diagnostics program serves to tie together the components of the VSK development toolkit into a program for configuring the ML402 and VIODC boards for video processing applications and for providing simple loopback and video processing functions. The VSK support toolkit consists of both hardware and software modules.
- Chapter 6, "VSK Tutorial"– illustrates the process of creating a video *processing core* or pcore which is compatible with systems constructed with the Xilinx Embedded Development Kit (EDK). EDK pcores are reusable peripherals which can be imported into any EDK project.
- Chapter 7, "Compiling the VIODC FPGA Design"– describes how to compile the System Generator `vsk_viodc_xxx.mdl` design to a bitstream (*xxx* is the version number).
- Appendix A, "VSK I/O Connector Location Pictures" – contains pictures showing connection locations on the VIODC, LVDS video camera, the ML402 board, and the ML402 Evaluation Platform.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support Web Case, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** `[`*`option_name`*`]` *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`

Convention	Meaning or Use	Example

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Handbook.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Chapter 1

Video Starter Kit Overview

Key Features

- Standard Video Development Platform for Xilinx FPGAs
- Real Time HD video simulation using Xilinx System Generator's *Hardware in the Loop*
- Video Starter Kit (VSK) includes:
  - Video I/O Daughter Card (VIODC) supports common video interfaces and standards
  - ML402 board with FPGA development platform (Xilinx XC4VSX35 FPGA)
  - LVDS Camera featuring Micron MTV022 automotive CMOS image sensor
  - Xilinx System Generator Software (8.2) for VSK
  - Xilinx ISE Software (v8.2) for VSK
  - XIlinx EDK Software (v8.2) for VSK
  - Application demos
  - Video cables and power supply
- VIODC features:
  - High Definition Component video input and output including 1080I, 720P, and 525P
  - Standard Definition S-video and Composite video input and output
  - Digital Video Interface (DVI) input and output up to 165 MHz
  - VGA analog input and output up to UXGA
  - SDI Serial Digital video interface input with cable equalizer and output cable driver. (The VSK is a demonstration platform only. For HD-SDI verification and compliance, Xilinx recommends using the Cook Technologies SDV board).
  - LVDS camera input
- Software development features:
  - System Generator Blockset for Mathwork's Simulink
  - High-Speed Ethernet Hardware-in-the-Loop co-simulation provides near real-time video simulation
  - High performance Multi-Port DDR memory controller
  - Automatically create MicroBlaze™ video peripherals with memory mapped I/O
  - Import MicroBlaze projects into System Generator models

VSK Hardware Overview

The Video Starter Kit hardware consists of a ML402 FPGA development platform with a VIODC and an LVDS video camera.

ML402 Development Platform

The VSK is based on the Virtex™-4 ML402 XtremeDSP Evaluation Platform. The ML402 board contains a programmable XC4VSX35 FPGA and a number of standard peripheral interfaces, such as Ethernet, RS232, and DDR memory.

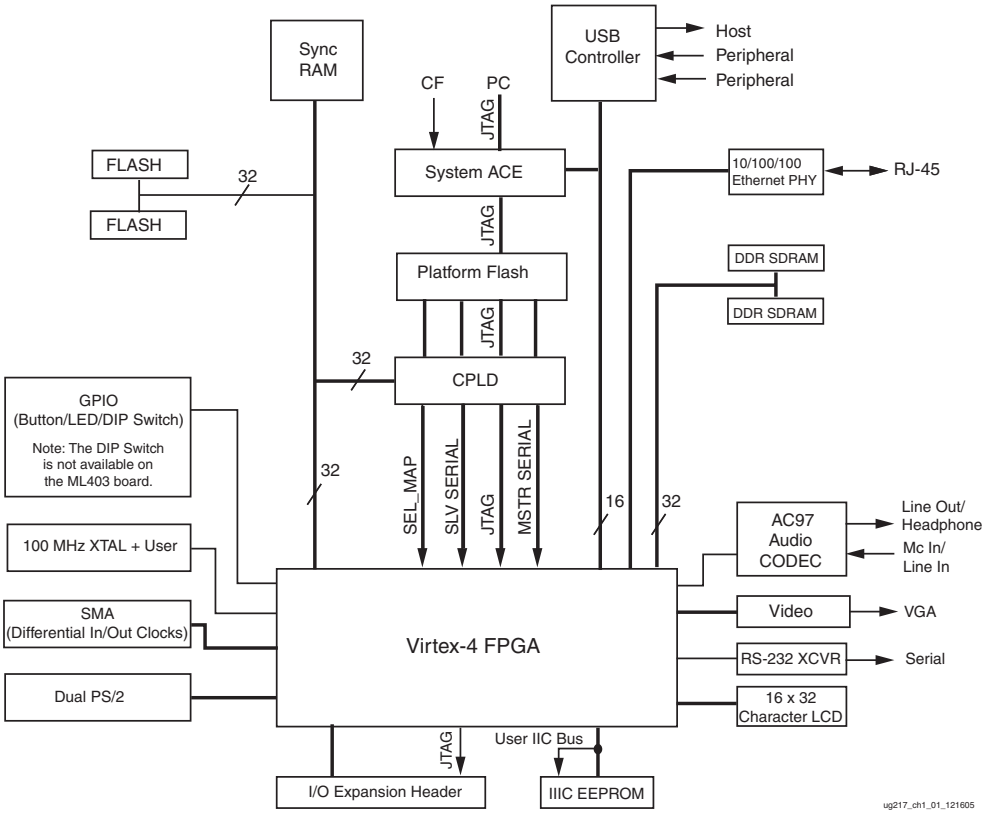

Figure 1-1: **ML402 Block Diagram**

XC4VSX35 FPGA

At the heart of the ML402 board is the XC4VSX35 FPGA, which contains both substantial logic resources (15,360 logic slices), dual port memory (192 x 18-Kbit block RAMs) and very high performance DSP blocks (192 DSP48 slices). In addition to high performance processing capability, the XC4VSX35 FPGA provides access to the VIODC card and the various external interfaces on the ML402 board.

Gigabit Ethernet

The 10/100/1 Gigabit Ethernet port provides a link between the VSK and a PC for high speed video rate simulation. This high-speed simulation capability is known as Hardware-in-the-Loop Co-Simulation. Simulation rates up to 600 Mb/s are achievable.

RS-232 Port

The RS-232 port provides a link to a PC terminal program, such as HyperTerminal. Used for debugging and controlling a MicroBlaze™ embedded processor. It must be connected to the PC using a NULL modem cable.

DDR Memory

A 267 MHz 32-bit wide DDR memory is used to store video frames.

System Ace Controller

The System Ace controller provides access to Compact Flash memory cards which are used to hold demos and bootable FPGA configurations.

I/O Expansion Header

The 64-signal pin expansion header is used to connect to the VIODC. For more information on the ML402 board, refer to the ML402 webpage on the Xilinx website.

Video Input and Output Daughter Card

The VIODC is a standard video interface card for Xilinx development platforms. It is compatible with the ML401, ML402, ML403 boards and other future Xilinx development platforms.

The VIODC is shown in Figure 1-2 with the video ports labeled. The VIODC provides access to high definition and standard definition video streams as well as computer graphics video interfaces, such as VGA over DVI and SDI interfaces. The following interfaces are supported.

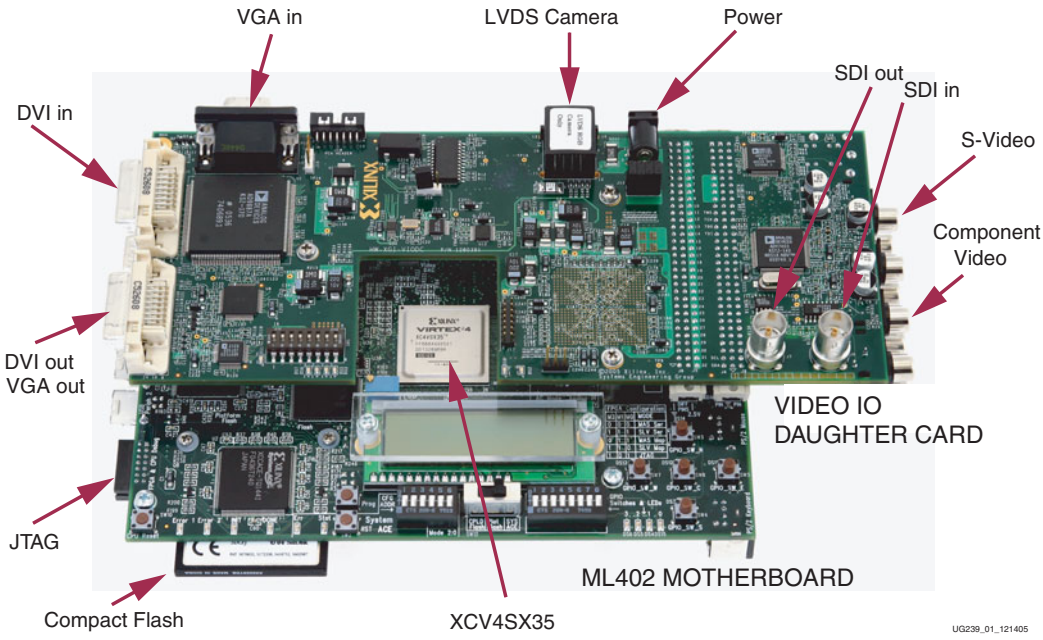

Figure 1-2: **VIODC and ML402 Board with Video Interface Ports Labeled**

LVDS Camera Input

The LVDS camera input port supports the Irvine Sensors LVDS RGB Camera with a Micron MT9V022 1/3 inch CMOS image sensor. The camera provides 752 x 480 pixels at 60 Hz progressive scan. It features low noise and very high dynamic range. The interface is implemented using LVDS signaling over standard Cat-6 Ethernet cables. Note that the LVDS camera interface is not compatible with Ethernet.

Component Video I/O

The Component Video I/O uses standard RCA connectors to provide High Definition (HD) video to the VIODC. Component Video is encoded as YPbPr video channels. The Component Video input on the VIODC supports 1080I, 720P, and 525P video standards. The Component Video interface devices on the VIODC support 10-bit digital video.

DVI Digital Video I/O

The VIODC supports DVI video input and output. DVI is commonly used to interface to flat panel displays and computer graphics cards. The VIODC DVI interfaces support up to 165 MHz pixel clocks. In addition to computer graphics, DVI is also used to carry HD video and is commonly found in high-end consumer video equipment, such as plasma displays, and can be found on some DVD players. The DVI ports can also be connected to HDMI interfaces by using a simple adapter.

S-Video and Composite Video

The VIODC supports S-Video inputs and outputs. These interfaces can be configured to support NTSC, PAL, and virtually any other Standard Definition (SD) video format.

SDI Video Interface

A complete SDI video interface capable of supporting both SD and HD SDI is included with the VIODC. The SDI standard is a high-speed serial interface used to carry video over coax cable. It is generally used in a studio environment. The SDI system includes cable equalizers and genlock circuitry. (The VSK is a demonstration platform only. For HD-SDI verification and compliance, Xilinx recommends using the Cook Technologies SDV board).

XCV2P7 FPGA

The VSK also includes a Xilinx XCV2P7 FPGA, which is used to interface to the various video interfaces, as well as the ML402 main board. It features Multi-Gigabit Transceivers (MGTs), which are used to support the SDI interface. It also enables the VIODC to be used in a stand-alone fashion.

VSK Demo Application

Several demo applications are included with the VSK. One demo (Figure 1-3) shows how the VSK can be configured as a video processor. This demo application is included in the VSK_diagnostics design included in the VSK examples directory. It can be used to apply some common video filters to the video from the RGB LVDS camera or other video sources.

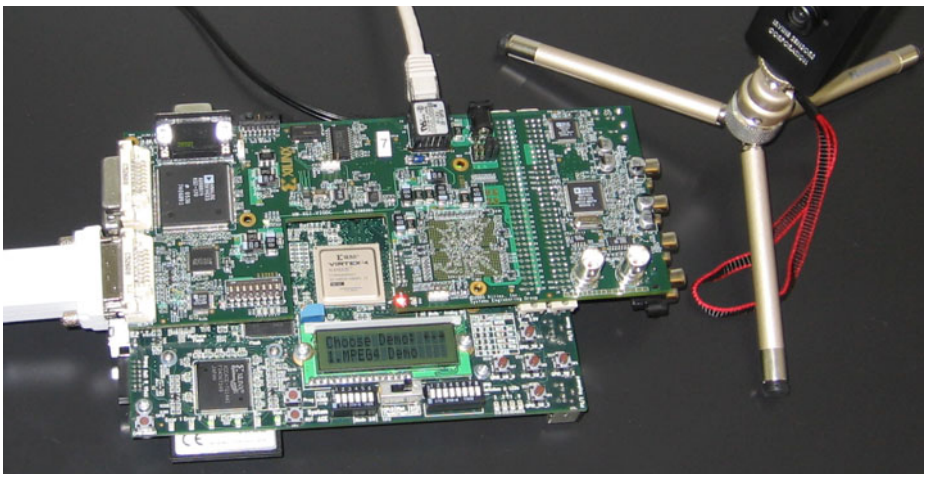

Figure 1-3: **RGB Camera Demo Setup**

Figure 1-4 illustrates a common video processing pipeline. The design implements a sequence of video operations including gamma correction, Bayer filtering, and color space correction. It is implemented using the System Generator blockset for MATLAB Simulink. System Generator is used to export this design as an EDK pcore, which is a standard Xilinx peripheral for embedded processors. After a pcore is created, it can be used in any Xilinx EDK project. Any EDK project can use a pcore, even if they are targeted to other development boards or FPGAs.

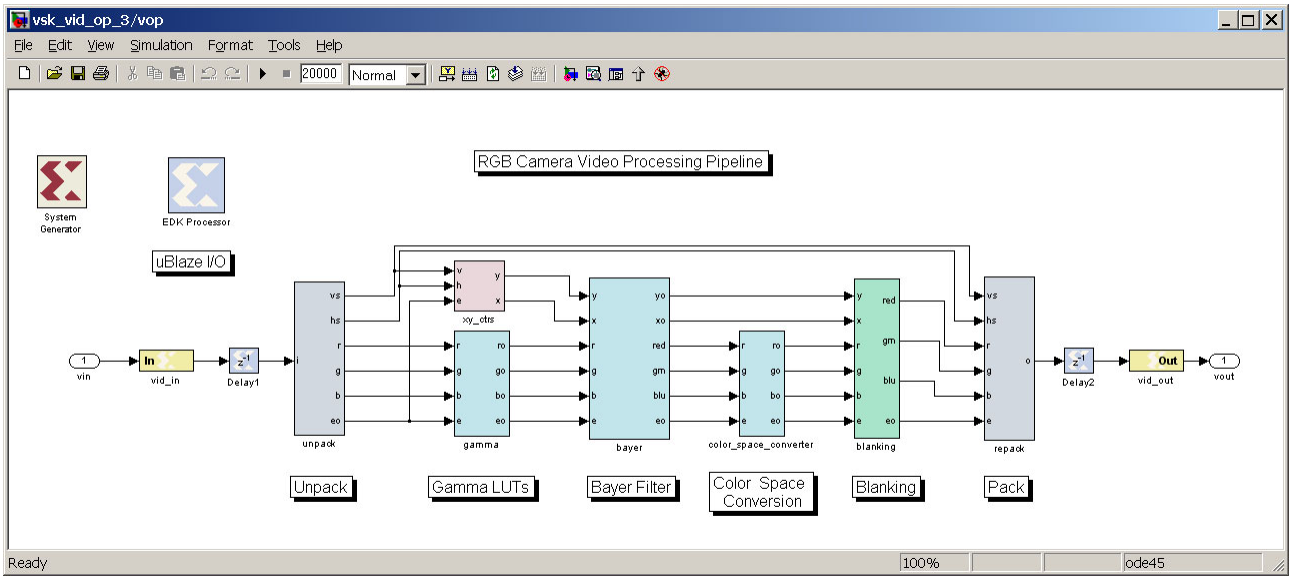

Figure 1-4: **RGB Camera Video Processing Pipeline**

The RGB camera processing pipeline design has a video input and a video output port. In the complete application, these video buses are connected to other pcores implementing

video processing, memory or I/O to the VIODC. The block diagram of the VSK diagnostics program is shown in Figure 1-5.

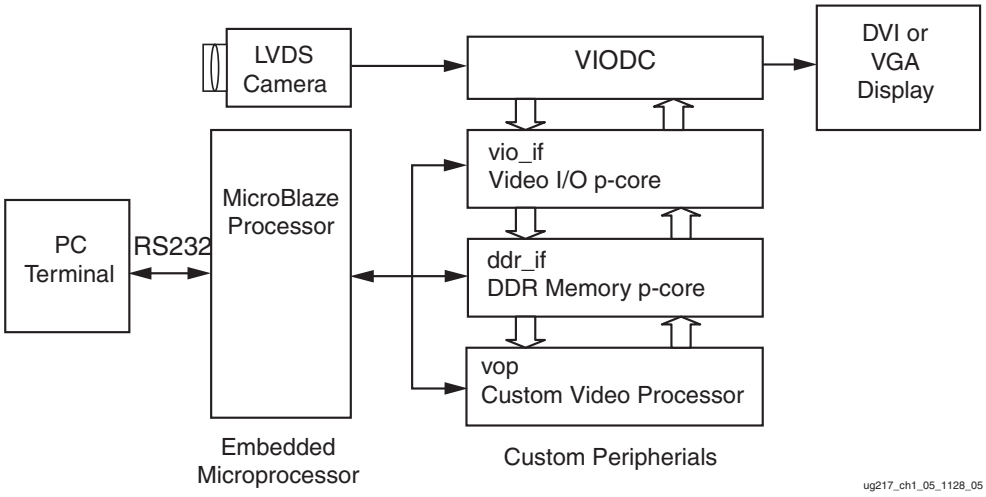

Figure 1-5: **Block Diagram of VSK RGB Camera Demo Included in the VSK**

For this application, the embedded MicroBlaze processor is used to configure the video processing pipeline. It communicates with memories and registers in the video pcores via System Generator shared memory primitives. The hardware logic and software drivers required by MicroBlaze to communicate with the shared memories in the pcore are automatically generated by System Generator during compilation.

The video processing demo is included in a pcore named vop for Video Op. The Sysgen design is named vsk_vid_op_6.mdl. This demo is part of the VSK diagnostic program and can be found in the VSK examples directory. For more information, refer to Chapter 5, "VSK Diagnostics and Support Tool Kit."

Software and Application Updates Available Online

VSK software and applications are supported by a VSK web page and the latest software and applications versions can be found there. The software support is integrated into System Generator and will be upgraded as new System Generator versions are released. New applications for the VSK will be posted on the VSK web page as they are developed.

Software Support Package Overview

The VSK includes hardware, software, and applications. Xilinx software is used to create applications which run on the VSK and Xilinx FPGAs. Three basic software flows are supported. These are illustrated in Figure 1-6, Figure 1-7, and Figure 1-8.

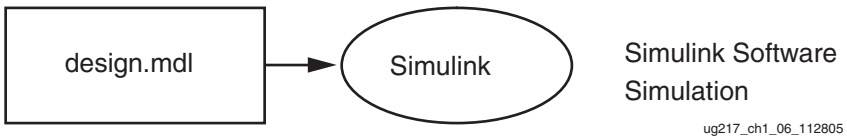

Figure 1-6: **Software Simulation Flow**

Software Simulation

In the first flow, called software simulation, Simulink designs that are constructed from the System Generator blocks are compiled and run in MATLAB Simulink. Figure 1-6 shows the software flow for software simulation. This flow is quick and easy to develop and offers good performance using the built-in MATLAB floating-point matrix operations. Larger systems, however, slow down significantly, and it is difficult to use this approach with live video streams. Additionally, problems occur when the design is implemented in fixed-point blocks for FPGA implementation. This can result in very low pixel rates due to poor simulation performance, often requiring hours per frame of video.

Hardware Implementation

The second software flow (Figure 1-7) compiles the user's design to hardware and runs the hardware on the VSK video development platform. This allows the video IP to be tested using live video streams.

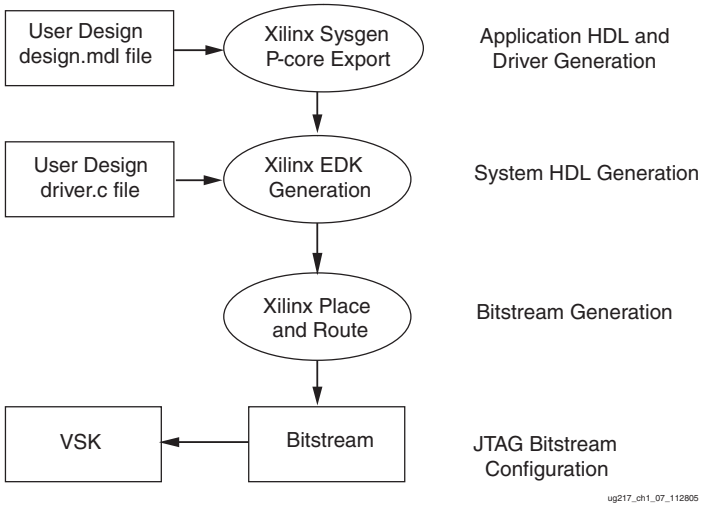

Figure 1-7: **Real-Time Deployment Flow**

Hardware Co-Simulation

The third type of software flow (Figure 1-8) is a hybrid of the software simulation and hardware deployment called Hardware-in-the-Loop co-simulation. In it, the bulk of the design is generated as in the real-time deployment flow. However, hardware data streams can be routed to the Simulink software simulation using the Xilinx System Generator Hardware co-sim engine.

The advantage of this mode is that small video filters which are part of a larger video processing system can be run in simulation, while the bulk of the video system is implemented in real time hardware. If buffering is employed, the software simulation can operate on stored video frames from the video stream at a reduced frame rate. Using the Ethernet Co-Simulation, near real-time video rates can be achieved. This translates to a few frames per second using 640 x 480 video.

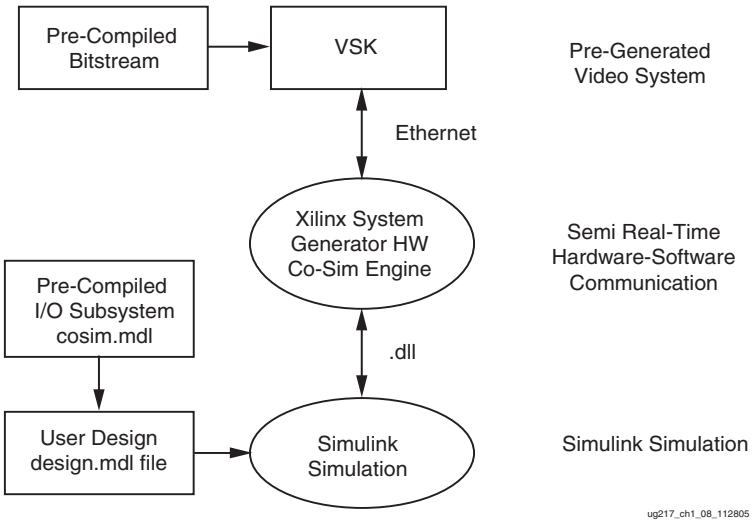

Figure 1-8: **Hardware-in-the-Loop Flow**

The pre-generated bitstream and co-sim subsystem can be generated from another system generator diagram or it can be an existing EDK project. The user can use the EDK import feature in System Generator to import an EDK project as a co-sim block.

VIODC HDL Support Package

While the above software flows leverage the advantages of developing video IP in System Generator/MATLAB/Simulink, users may prefer to use traditional HDL design flows.The Video Starter Kit also includes two demonstrations written in Verilog. These examples exercise all the video functions on the VIODC and are generally self-explanatory. In addition, these demos can run on a stand-alone VIODC board.

Refer to the *DVI, VGA, and Component Video Demonstration User Guide* and the *SDI Video Demonstration User Guide* for further information.

System Generator Support

System Generator includes several features that are useful for developing video applications with the Video Starter Kit. These are outlined below and additional documentation for each of these features can be found in the VSK document package. In addition, tutorials are included in the examples directory to assist in learning to use these powerful features.

DDR Memory Controller

The VSK includes a capable multi-port memory controller. The controller supports the DDR memory on the ML402 board. It can also be targeted to other boards and is fully configurable for port size and number of ports. The controller contains a simulation model and can be run in HDL co-simulation mode, or compiled to run in real time and as part of hardware co-simulation block.

Pcore Export and EDK Import

Pcore export is a new method of generation from Simulink diagrams that allows the user diagram to be imported into any EDK project as a Pcore. Conversely, EDK import allows EDK projects to be imported into System Generator diagrams. Pcore export is used to generate the three pcores in the VSK diagnostic demo from System Generator diagrams.

Multiple Subsystem Generator

The Multiple Subsystem Generator flow allows System Generator models to include multiple clock domains. This flow is used to generate the design for the VIODC FPGA, which is included in the VSK diagnostics program.

Ethernet Co-Sim

High-speed Ethernet co-sim and point-to-point Ethernet co-sim are supported by the System Generator for the VSK. To achieve near real-time video rates, reusable buffer blocks are included in the Ethernet demos that are included in the VSK.

Diagnostics

A diagnostics program called the vsk_diagnostics is included with the VSK. Refer to Chapter 5, "VSK Diagnostics and Support Tool Kit" for more information. The diagnostics include System Generator designs for the VIODC FPGA, and three pcores integrated into an EDK project for the ML402 FPGAs. They also include software routines to configure the video interface chips on the VIODC and to control the video processing pcore, video interface pcore, and DDR memory pcore.

Demonstrations

Several demonstration designs are included with the VSK.

MPEG Decoding Demo

The VSK diagnostics include an MPEG-4 demo, which can be run from the Compact Flash. Refer to the *Video Starter Kit Quick Start Guide (UG239)* and the *MPEG-4 Demonstration User Guide (UG234)* for more details.

VSK Diagnostics Camera Demo

The VSK diagnostics also include a camera demo, which can be run from the Compact Flash. Refer to *Video Starter Kit Quick Start Guide (UG239)* and Chapter 5, "VSK Diagnostics and Support Tool Kit" for more details.

SDI Demo

A demo featuring the SDI interface and written in Verilog is available for the VIODC. Refer to the documents *SDI Video Demonstration User Guide* in the VSK document package for further information.