



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Video Starter Kit

User Guide

UG217 (v1.5) October 26, 2006





Xilinx is disclosing this Document and Intellectual Property (hereinafter “the Design”) to you for use in the development of designs to operate on, or interface with Xilinx FPGAs. Except as stated herein, none of the Design may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Any unauthorized use of the Design may violate copyright laws, trademark laws, the laws of privacy and publicity, and communications regulations and statutes.

Xilinx does not assume any liability arising out of the application or use of the Design; nor does Xilinx convey any license under its patents, copyrights, or any rights of others. You are responsible for obtaining any rights you may require for your use or implementation of the Design. Xilinx reserves the right to make changes, at any time, to the Design as deemed desirable in the sole discretion of Xilinx. Xilinx assumes no obligation to correct any errors contained herein or to advise you of any correction if such be made. Xilinx will not assume any liability for the accuracy or correctness of any engineering or technical support or assistance provided to you in connection with the Design.

THE DESIGN IS PROVIDED “AS IS” WITH ALL FAULTS, AND THE ENTIRE RISK AS TO ITS FUNCTION AND IMPLEMENTATION IS WITH YOU. YOU ACKNOWLEDGE AND AGREE THAT YOU HAVE NOT RELIED ON ANY ORAL OR WRITTEN INFORMATION OR ADVICE, WHETHER GIVEN BY XILINX, OR ITS AGENTS OR EMPLOYEES. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DESIGN, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOST DATA AND LOST PROFITS, ARISING FROM OR RELATING TO YOUR USE OF THE DESIGN, EVEN IF YOU HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE TOTAL CUMULATIVE LIABILITY OF XILINX IN CONNECTION WITH YOUR USE OF THE DESIGN, WHETHER IN CONTRACT OR TORT OR OTHERWISE, WILL IN NO EVENT EXCEED THE AMOUNT OF FEES PAID BY YOU TO XILINX HEREUNDER FOR USE OF THE DESIGN. YOU ACKNOWLEDGE THAT THE FEES, IF ANY, REFLECT THE ALLOCATION OF RISK SET FORTH IN THIS AGREEMENT AND THAT XILINX WOULD NOT MAKE AVAILABLE THE DESIGN TO YOU WITHOUT THESE LIMITATIONS OF LIABILITY.

The Design is not designed or intended for use in the development of on-line control equipment in hazardous environments requiring fail-safe controls, such as in the operation of nuclear facilities, aircraft navigation or communications systems, air traffic control, life support, or weapons systems (“High-Risk Applications”). Xilinx specifically disclaims any express or implied warranties of fitness for such High-Risk Applications. You represent that use of the Design in such High-Risk Applications is fully at your risk.

© 2005, 2006 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

Revision History

Video Starter Kit

UG217 (v1.5) October 26, 2006

The following table shows the revision history for this document.

Date	Version	Revision
12/22/05	1.0	Initial Xilinx release.
02/13/06	1.1	Edits throughout the document.
03/14/06	1.2	Minor edits in Chapter 6. Replaced Figure 6-5.
06/27/06	1.3	Minor edits.
10/10/06	1.4	Edits and additions to Chapter 5, “VSK Diagnostics and Support Tool Kit” and Chapter 7, “Compiling the VIODC FPGA Design.”
10/26/06	1.5	Updated Figure 5-6 and Figure 5-9 . Added new Table 5-5 .

Contents

Preface: About This Guide

Guide Contents	13
Additional Resources	14
Conventions	14
Typographical	14
Online Document	15

Chapter 1: Video Starter Kit Overview

Key Features	17
VSK Hardware Overview	18
ML402 Development Platform	18
XC4VSX35 FPGA	18
Gigabit Ethernet	18
RS-232 Port	19
DDR Memory	19
System Ace Controller	19
I/O Expansion Header	19
Video Input and Output Daughter Card	19
LVDS Camera Input	20
Component Video I/O	20
DVI Digital Video I/O	20
S-Video and Composite Video	20
SDI Video Interface	20
XCV2P7 FPGA	20
VSK Demo Application	21
Software and Application Updates Available Online	22
Software Support Package Overview	22
Software Simulation	23
Hardware Implementation	23
Hardware Co-Simulation	23
VIODC HDL Support Package	24
System Generator Support	24
DDR Memory Controller	24
Pcore Export and EDK Import	25
Multiple Subsystem Generator	25
Ethernet Co-Sim	25
Diagnostics	25
Demonstrations	25
MPEG Decoding Demo	25
VSK Diagnostics Camera Demo	25
SDI Demo	25
Video Demo in Verilog	26

Chapter 2: Developing Video Applications In System Generator

Overview	27
Real-Time Operation	27
Hardware-in-the-Loop Video Simulation	28
Hardware-in the Loop Co-Simulation	28
Software Simulation Modes	29
Hardware-Software Systems	30
Generating a Video Processor as an EDK Pcore	30
Hardware-Software Communication	31
Memory Mapped Hardware	31
MicroBlaze Processor Communicating with a Shared Memory	31
Hardware-Software Co-Simulation	32
EDK Co-Simulation	32
VSK Video Processor Development System	32
ML402 FPGA	33
MicroBlaze Subsystem	33
VIODC FPGA	33

Chapter 3: EDK Integration

Overview	35
MicroBlaze Processor Interface	35
EDK Pcore Export Mode	36
EDK Import Mode	36
Adding a Processor to a System Generator Design	36
The EDK Processor Block	36
Interfacing the EDK Processor to User Logic	36
Exporting the Design as a Pcore	37
Importing an EDK Project into System Generator	39
Writing Software Code	41

Chapter 4: Hardware Co-Simulation

Hardware Co-Simulation Overview	45
Co-Simulation Communication Primitives	45
Ports	45
Shared Register	46
Shared Memory	46
FIFO	47
Pad	48
Shared Memory Read/Write Blocks	49
Co-Simulation Interfaces	50
JTAG	50
PCI	50
Network-Based Ethernet Co-Simulation	50
Point to Point Ethernet Co-Simulation	51
Third Party Co-Simulation	51
Building a Co-Sim Project	52
Choosing a Compilation Target	52

Invoking the Code Generator	52
Hardware Co-Simulation Blocks	54
Ethernet Co-Sim Setup	55
System ACE Setup	56
Prepare the System ACE Compact Flash Card	56
Assign an Ethernet MAC Address and IPv4 Address	57
Adjust On-Board Settings for System ACE	57
System ACE Troubleshooting	58
Verify System ACE Settings	58
Verify Ethernet Interface And Connection Status	58
Ensuring a Correct Setup	59
Choose the Configuration Method	60
Configure the Ethernet Interface Settings	61
Co-Simulating the Design	63
Frame Based Co-Simulation Tutorial	64

Chapter 5: VSK Diagnostics and Support Tool Kit

Overview	65
VIODC Design	66
IIC Interface	68
VIODC-ML402 Serial Port	68
VIODC Serial Port Interface	68
VIODC Registers	70
Clock Routing	73
VIO Design	73
VIO Mask	76
Compile Type	76
Input Type	77
Output Type	77
Mask Modifications	77
EDK Pcore	77
Bitstream	78
VIO I/O Buses	79
VIO Registers	80
DDR Design	80
VOP Design	81
Running the Diagnostics	82
Hardware Setup	83
Software Setup	84
Configure the ML402 Board to Run the Diagnostics	84
Running the VSK Diagnostics	85
RGB Camera Test	85
Component Video Input Test	85
DVI Input Test	86
VGA Input Test	86
Composite Input Test	86
S-Video Input Test	86
Additional Diagnostics and Controls	87
VIO Diagnostics Peek and Poke Facility	87
VIO Diagnostics - Device Configure Facility	88
Troubleshooting	88

Chapter 6: VSK Tutorial

Overview	89
Creating a Video Gain and Offset Peripheral	89
Gain and Offset Theory	90
System Architecture	90
Video Stream Format	90
Pixel Enable	91
Tutorial Files	91
Building the Gain Offset Pcore in System Generator	91
Testing the Video Function in System Generator	95
Generating the Pcore	95
Importing the Pcore into an EDK Project	96
Importing the Pcore Software Drivers	98
Controlling the Pcore from a Demo Menu	99
Running the Tutorial with Live Video	99

Chapter 7: Compiling the VIODC FPGA Design

Tutorial Overview	101
Overview of VIODC Design Compilation Process	101
VIODC Design Components	101
Incrementing the VIODC Version ID	102
Generating the Design Using the Multiple Subsystem Generator	102
Using ISE Project Navigator to Add a VHDL Wrapper	104
Loading the VIODC Design to the XCV2P7 FPGA on the VIODC Board	105
Verifying the VIODC Operation	105
Modifying the VSK Diagnostic Software EDK Project	106

Appendix A: VSK I/O Connector Location Pictures

VIODC Connectors	107
LVDS Camera	110
ML402 Board	111

Schedule of Figures

Chapter 1: Video Starter Kit Overview

Figure 1-1: ML402 Block Diagram	18
Figure 1-2: VIODC and ML402 Board with Video Interface Ports Labeled	19
Figure 1-3: RGB Camera Demo Setup	21
Figure 1-4: RGB Camera Video Processing Pipeline.	21
Figure 1-5: Block Diagram of VSK RGB Camera Demo Included in the VSK	22
Figure 1-6: Software Simulation Flow	22
Figure 1-7: Real-Time Deployment Flow.	23
Figure 1-8: Hardware-in-the-Loop Flow	24

Chapter 2: Developing Video Applications In System Generator

Figure 2-1: Video System Diagram	27
Figure 2-2: Real-Time Video Processing	28
Figure 2-3: Hardware-in-the-Loop Video Processing	28
Figure 2-4: Simulink Diagram Implementing a Gain and Offset Function Using Xilinx System Generator Blocks	29
Figure 2-5: Gain and Offset Function Compiled to a Hardware Co-Sim Token	29
Figure 2-6: Software Simulation Using Live Video Signals with Simulink	30
Figure 2-7: MicroBlaze Processor with Peripherals and Three Custom Video Peripherals	30
Figure 2-8: System Generator Shared Memory Blocks	31
Figure 2-9: MicroBlaze Processor Communicating with a Shared Memory.	31
Figure 2-10: EDK Import with Registered IO	32
Figure 2-11: ML402 FPGA	33

Chapter 3: EDK Integration

Figure 3-1: Memory-Mapped User Logic	35
Figure 3-2: EDK Processor Block	36
Figure 3-3: EDK Processor GUI	37
Figure 3-4: Export as a Pcore to EDK	38
Figure 3-5: Launching Import Wizard	39
Figure 3-6: EDK Import Wizard.	39
Figure 3-7: Hardware Co-Simulation Options	40
Figure 3-8: Software Tab	40
Figure 3-9: Xilinx Platform Studio - Assembly View	41
Figure 3-10: Memory Map Documentation	42

Chapter 4: Hardware Co-Simulation

Figure 4-1: Ports	45
Figure 4-2: Shared Register Pair	46
Figure 4-3: Shared Memory	47
Figure 4-4: Shared FIFO Pair	47
Figure 4-5: Shared Memory Read and Write Blocks	49
Figure 4-6: Status Bar	51
Figure 4-7: Hardware Co-Simulation Targets	52
Figure 4-8: Code Generator Generate Button	52
Figure 4-9: Compilation Status	53
Figure 4-10: Example of a Run-time Hardware Co-Simulation Block Inserted in the Original Model	54
Figure 4-11: Port Interface of a Run-time Co-Simulation Block Matches the Port Interface of the Original Design	55
Figure 4-12: ML402 Board Diagram	56
Figure 4-13: On-Board Settings	57
Figure 4-14: Board LCD Screen	58
Figure 4-15: Ethernet Status LEDs	58
Figure 4-16: FPGA Processing Subsystem	59
Figure 4-17: Select Free Running Clock Source Mode	60
Figure 4-18: Check the Has Video I/O Daughter Card (VIO DC)	60
Figure 4-19: Choose the Configuration Method	61
Figure 4-20: Configure the Ethernet Interface Settings	61
Figure 4-21: Ensure the Appropriate Interface is Chosen	62
Figure 4-22: Ethernet Parameters Displayed on ML402 LCD Display	62
Figure 4-23: Status Dialog Box	63
Figure 4-24: Status Showing Reconnection	63
Figure 4-25: Two Windows Shown after Configuration	64

Chapter 5: VSK Diagnostics and Support Tool Kit

Figure 5-1: VSK Support Toolkit to Develop a Video Processor Pcore	65
Figure 5-2: VIO DC – Top-Level Design with Seven Independent Clock Domains	66
Figure 5-3: VIO DC Video Routing MUX	67
Figure 5-4: SPort Waveform	69
Figure 5-5: VIO DC Clock Routing MUX	73
Figure 5-6: VIO Pcore Top-Level Diagram	74
Figure 5-7: VIO Parameter Mask	75
Figure 5-8: Look Under Mask View of the vio if Block	76
Figure 5-9: VIO Bitstream Design	78
Figure 5-10: VIO Pcore Top-Level Diagram	79
Figure 5-11: DDR Design	81
Figure 5-12: RGB Camera Video Processing Pipeline	81
Figure 5-13: VSK Demo Setup	82

<i>Figure 5-14: ML402 Board - Top View</i>	83
<i>Figure 5-15: Virtex-4 ML40x Evaluation Platform Components (Back)</i>	83
<i>Figure 5-16: Configure the ML402 Board</i>	84
<i>Figure 5-17: HyperTerm RS-232 Terminal Window</i>	85

Chapter 6: VSK Tutorial

<i>Figure 6-1: Gain and Offset</i>	90
<i>Figure 6-2: Gain and Offset System Architecture</i>	90
<i>Figure 6-3: vid_go_start Simulation Results</i>	92
<i>Figure 6-4: Gain and Offset Processing Pcore</i>	92
<i>Figure 6-5: Connecting the Blocks</i>	93
<i>Figure 6-6: EDK Processor Configuration</i>	94
<i>Figure 6-7: Design Saved as vid_go.mdl</i>	95
<i>Figure 6-8: Generating the Pcore</i>	96
<i>Figure 6-9: Configure Coprocessor Panel</i>	97
<i>Figure 6-10: System Menu Showing New Imported Pcore</i>	97
<i>Figure 6-11: Pcore Wiring with vid_gain_offset Pcore Inserted into Video Pipeline</i> ...	98
<i>Figure 6-12: iMPACT Window</i>	100

Chapter 7: Compiling the VIODC FPGA Design

<i>Figure 7-1: VIODC Serial Register I/O Block</i>	102
<i>Figure 7-2: vsk_viodc_xxx.mdl Top Level</i>	103
<i>Figure 7-3: MSG Generate Block</i>	103
<i>Figure 7-4: Directory Structure Generated by Multiple Subsystem Generator</i>	104
<i>Figure 7-5: Project Navigator Source File View</i>	105

Appendix A: VSK I/O Connector Location Pictures

<i>Figure A-1: VIODC Rear View</i>	107
<i>Figure A-2: VIODC Left Side View</i>	108
<i>Figure A-3: VIODC Right Side View</i>	109
<i>Figure A-4: LVDS Camera</i>	110
<i>Figure A-5: ML402 Board</i>	111
<i>Figure A-6: ML402 Evaluation Platform</i>	112

Schedule of Tables

Chapter 1: Video Starter Kit Overview

Chapter 2: Developing Video Applications In System Generator

Chapter 3: EDK Integration

<i>Table 3-1: Pcore Directory Structure</i>	38
---	----

Chapter 4: Hardware Co-Simulation

Chapter 5: VSK Diagnostics and Support Tool Kit

<i>Table 5-1: VSK Support Toolkit Components</i>	65
<i>Table 5-2: VIODC Video Format</i>	68
<i>Table 5-3: Available IIC Devices</i>	68
<i>Table 5-4: VIODC Registers</i>	70
<i>Table 5-5: VIO_IF GPIO Format</i>	79
<i>Table 5-6: VIO Registers</i>	80
<i>Table 5-7: Keystroke Menu</i>	87
<i>Table 5-8: Available Devices</i>	87

Chapter 6: VSK Tutorial

Chapter 7: Compiling the VIODC FPGA Design

Appendix A: VSK I/O Connector Location Pictures

About This Guide

This user guide provides a description of the Video Starter Kit (VSK) contents, features, hardware, and software. The Video Starter Kit hardware consists of a ML402 FPGA development platform with a Video Input and Output Daughter Card (VIODC) and an LVDS video camera. The Video Starter Kit can be used with System Generator to develop EDK processing cores that process live video streams.

Guide Contents

This user guide contains the following chapters:

- [Chapter 1, “Video Starter Kit Overview”](#) – provides a kit overview with a brief description of the ML402 development platform, the VIODC, and the LVDS video camera.
- [Chapter 2, “Developing Video Applications In System Generator”](#) – The Video Starter Kit provides for both simulation and real-time operation for each of the components in a video system.
- [Chapter 3, “EDK Integration”](#) – details the design-flow for incorporating a MicroBlaze™ processor into MVI framework. In particular, it describes using the EDK processor block in System Generator and the automatically generated software drivers to read and write data to the System Generator design.
- [Chapter 4, “Hardware Co-Simulation”](#) – provides a description of the hardware co-simulation interfaces that make it possible to compile a System Generator diagram into an FPGA bitstream and associate this bitstream with a new run-time hardware co-simulation block.
- [Chapter 5, “VSK Diagnostics and Support Tool Kit”](#) – describes how the VSK diagnostics program serves to tie together the components of the VSK development toolkit into a program for configuring the ML402 and VIODC boards for video processing applications and for providing simple loopback and video processing functions. The VSK support toolkit consists of both hardware and software modules.
- [Chapter 6, “VSK Tutorial”](#) – illustrates the process of creating a video *processing core* or pcore which is compatible with systems constructed with the Xilinx Embedded Development Kit (EDK). EDK pcores are reusable peripherals which can be imported into any EDK project.
- [Chapter 7, “Compiling the VIODC FPGA Design”](#) – describes how to compile the System Generator `vsk_viodc_xxx.mdl` design to a bitstream (`xxx` is the version number).
- [Appendix A, “VSK I/O Connector Location Pictures”](#) – contains pictures showing connection locations on the VIODC, LVDS video camera, the ML402 board, and the ML402 Evaluation Platform.

Additional Resources

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/literature/index.htm>.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support Web Case, see the Xilinx website at:

<http://www.xilinx.com/support>.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild <i>design_name</i>
Helvetica bold	Commands that you select from a menu	File → Open
	Keyboard shortcuts	Ctrl+C
Italic font	Variables in a syntax statement for which you must supply values	ngdbuild <i>design_name</i>
	References to other manuals	See the <i>Development System Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7:0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>
Braces { }	A list of items from which you must choose one or more	lowpwr = { on off }
Vertical bar	Separates items in a list of choices	lowpwr = { on off }

Convention	Meaning or Use	Example
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	allow block <i>block_name</i> <i>loc1 loc2 ... locn</i> ;

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section “ Additional Resources ” for details. Refer to “ Title Formats ” in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the <i>Handbook</i> .
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Video Starter Kit Overview

Key Features

- Standard Video Development Platform for Xilinx FPGAs
- Real Time HD video simulation using Xilinx System Generator's *Hardware in the Loop*
- Video Starter Kit (VSK) includes:
 - ◆ Video I/O Daughter Card (VIODC) supports common video interfaces and standards
 - ◆ ML402 board with FPGA development platform (Xilinx XC4VSX35 FPGA)
 - ◆ LVDS Camera featuring Micron MTV022 automotive CMOS image sensor
 - ◆ Xilinx System Generator Software (8.2) for VSK
 - ◆ Xilinx ISE Software (v8.2) for VSK
 - ◆ Xilinx EDK Software (v8.2) for VSK
 - ◆ Application demos
 - ◆ Video cables and power supply
- VIODC features:
 - ◆ High Definition Component video input and output including 1080I, 720P, and 525P
 - ◆ Standard Definition S-video and Composite video input and output
 - ◆ Digital Video Interface (DVI) input and output up to 165 MHz
 - ◆ VGA analog input and output up to UXGA
 - ◆ SDI Serial Digital video interface input with cable equalizer and output cable driver. (The VSK is a demonstration platform only. For HD-SDI verification and compliance, Xilinx recommends using the [Cook Technologies SDV board](#)).
 - ◆ LVDS camera input
- Software development features:
 - ◆ System Generator Blockset for Mathwork's Simulink
 - ◆ High-Speed Ethernet Hardware-in-the-Loop co-simulation provides near real-time video simulation
 - ◆ High performance Multi-Port DDR memory controller
 - ◆ Automatically create MicroBlaze™ video peripherals with memory mapped I/O
 - ◆ Import MicroBlaze projects into System Generator models

VSK Hardware Overview

The Video Starter Kit hardware consists of a ML402 FPGA development platform with a VIODC and an LVDS video camera.

ML402 Development Platform

The VSK is based on the Virtex™-4 ML402 XtremeDSP Evaluation Platform. The ML402 board contains a programmable XC4VSX35 FPGA and a number of standard peripheral interfaces, such as Ethernet, RS232, and DDR memory.

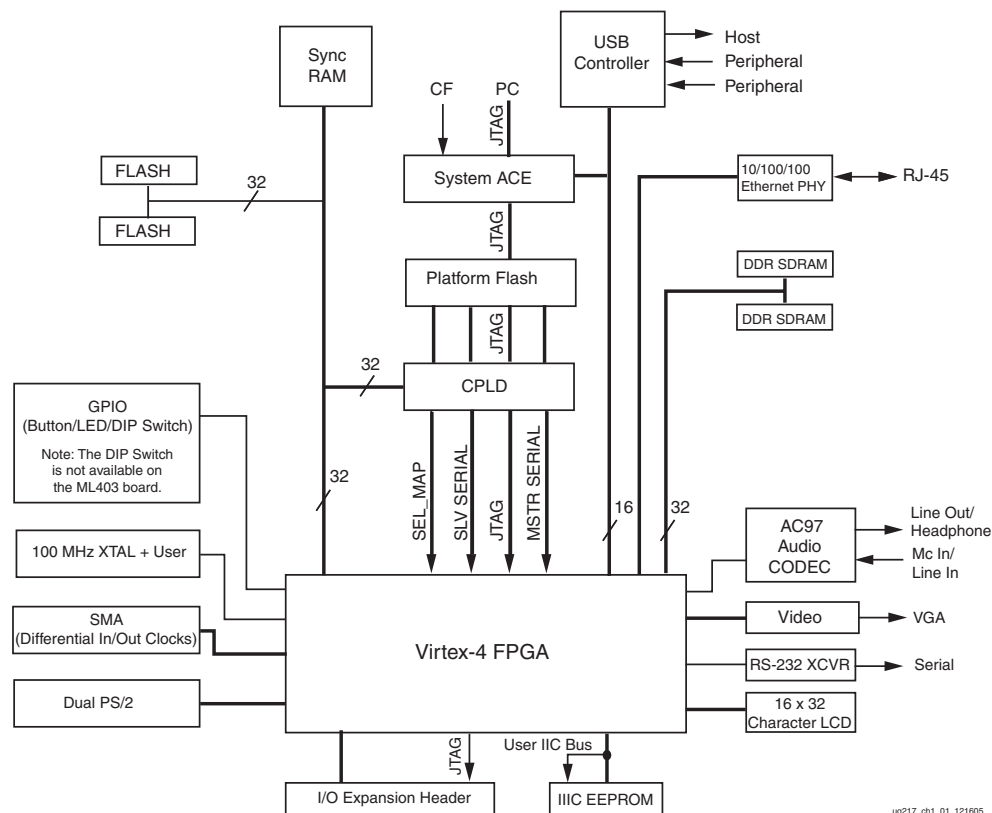


Figure 1-1: ML402 Block Diagram

XC4VSX35 FPGA

At the heart of the ML402 board is the XC4VSX35 FPGA, which contains both substantial logic resources (15,360 logic slices), dual port memory (192 x 18-Kbit block RAMs) and very high performance DSP blocks (192 DSP48 slices). In addition to high performance processing capability, the XC4VSX35 FPGA provides access to the VIODC card and the various external interfaces on the ML402 board.

Gigabit Ethernet

The 10/100/1 Gigabit Ethernet port provides a link between the VSK and a PC for high speed video rate simulation. This high-speed simulation capability is known as Hardware-in-the-Loop Co-Simulation. Simulation rates up to 600 Mb/s are achievable.

RS-232 Port

The RS-232 port provides a link to a PC terminal program, such as HyperTerminal. Used for debugging and controlling a MicroBlaze™ embedded processor. It must be connected to the PC using a NULL modem cable.

DDR Memory

A 267 MHz 32-bit wide DDR memory is used to store video frames.

System Ace Controller

The System Ace controller provides access to Compact Flash memory cards which are used to hold demos and bootable FPGA configurations.

I/O Expansion Header

The 64-signal pin expansion header is used to connect to the VIODC. For more information on the ML402 board, refer to the [ML402](#) webpage on the Xilinx website.

Video Input and Output Daughter Card

The VIODC is a standard video interface card for Xilinx development platforms. It is compatible with the ML401, ML402, ML403 boards and other future Xilinx development platforms.

The VIODC is shown in [Figure 1-2](#) with the video ports labeled. The VIODC provides access to high definition and standard definition video streams as well as computer graphics video interfaces, such as VGA over DVI and SDI interfaces. The following interfaces are supported.

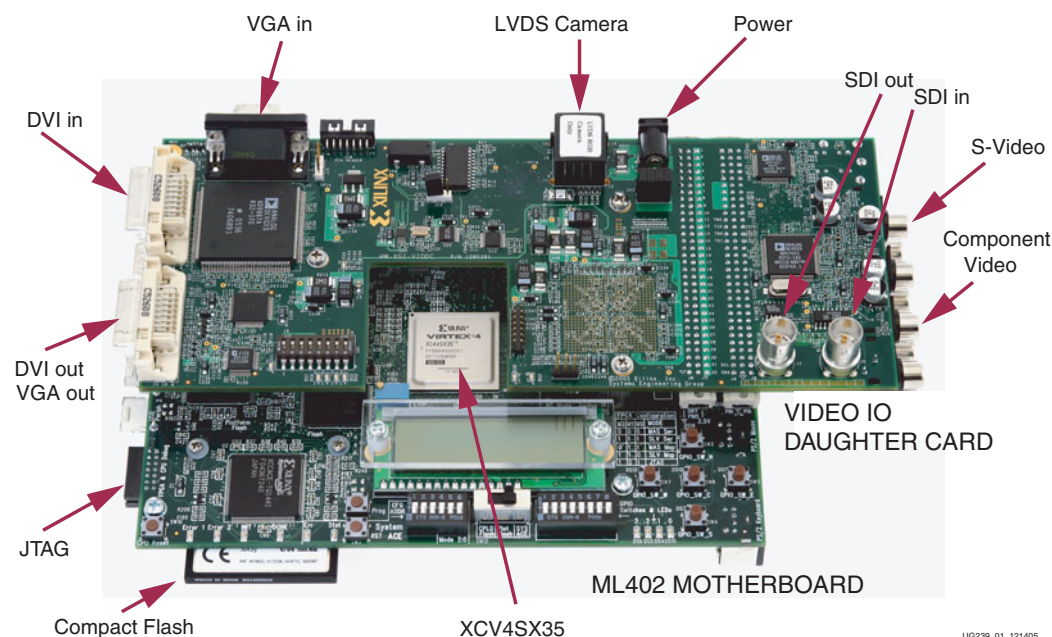


Figure 1-2: VIODC and ML402 Board with Video Interface Ports Labeled

UG239_01_121405

LVDS Camera Input

The LVDS camera input port supports the [Irvine Sensors](#) LVDS RGB Camera with a [Micron](#) MT9V022 1/3 inch CMOS image sensor. The camera provides 752 x 480 pixels at 60 Hz progressive scan. It features low noise and very high dynamic range. The interface is implemented using LVDS signaling over standard Cat-6 Ethernet cables. Note that the LVDS camera interface is not compatible with Ethernet.

Component Video I/O

The Component Video I/O uses standard RCA connectors to provide High Definition (HD) video to the VIODC. Component Video is encoded as YPbPr video channels. The Component Video input on the VIODC supports 1080I, 720P, and 525P video standards. The Component Video interface devices on the VIODC support 10-bit digital video.

DVI Digital Video I/O

The VIODC supports DVI video input and output. DVI is commonly used to interface to flat panel displays and computer graphics cards. The VIODC DVI interfaces support up to 165 MHz pixel clocks. In addition to computer graphics, DVI is also used to carry HD video and is commonly found in high-end consumer video equipment, such as plasma displays, and can be found on some DVD players. The DVI ports can also be connected to HDMI interfaces by using a simple adapter.

S-Video and Composite Video

The VIODC supports S-Video inputs and outputs. These interfaces can be configured to support NTSC, PAL, and virtually any other Standard Definition (SD) video format.

SDI Video Interface

A complete SDI video interface capable of supporting both SD and HD SDI is included with the VIODC. The SDI standard is a high-speed serial interface used to carry video over coax cable. It is generally used in a studio environment. The SDI system includes cable equalizers and genlock circuitry. (The VSK is a demonstration platform only. For HD-SDI verification and compliance, Xilinx recommends using the [Cook Technologies SDV board](#)).

XCV2P7 FPGA

The VSK also includes a Xilinx XCV2P7 FPGA, which is used to interface to the various video interfaces, as well as the ML402 main board. It features Multi-Gigabit Transceivers (MGTs), which are used to support the SDI interface. It also enables the VIODC to be used in a stand-alone fashion.

VSK Demo Application

Several demo applications are included with the VSK. One demo (Figure 1-3) shows how the VSK can be configured as a video processor. This demo application is included in the VSK_diagnostics design included in the VSK examples directory. It can be used to apply some common video filters to the video from the RGB LVDS camera or other video sources.

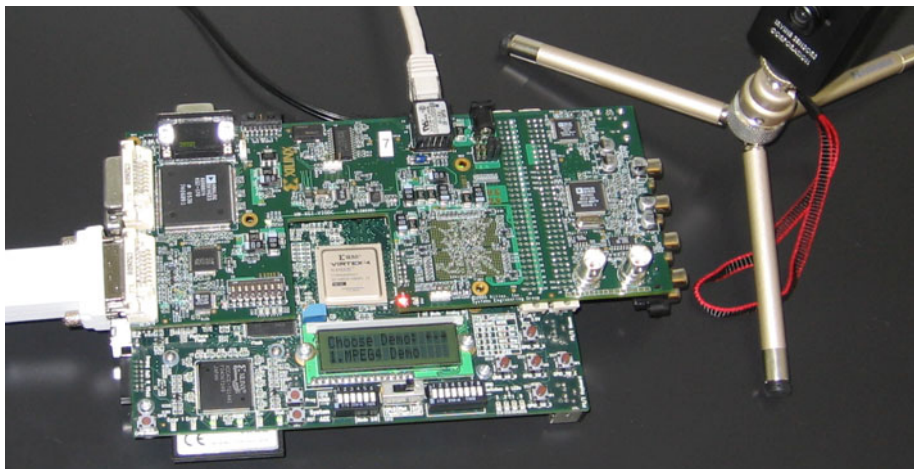


Figure 1-3: RGB Camera Demo Setup

Figure 1-4 illustrates a common video processing pipeline. The design implements a sequence of video operations including gamma correction, Bayer filtering, and color space correction. It is implemented using the System Generator blockset for MATLAB Simulink. System Generator is used to export this design as an EDK pcore, which is a standard Xilinx peripheral for embedded processors. After a pcore is created, it can be used in any Xilinx EDK project. Any EDK project can use a pcore, even if they are targeted to other development boards or FPGAs.

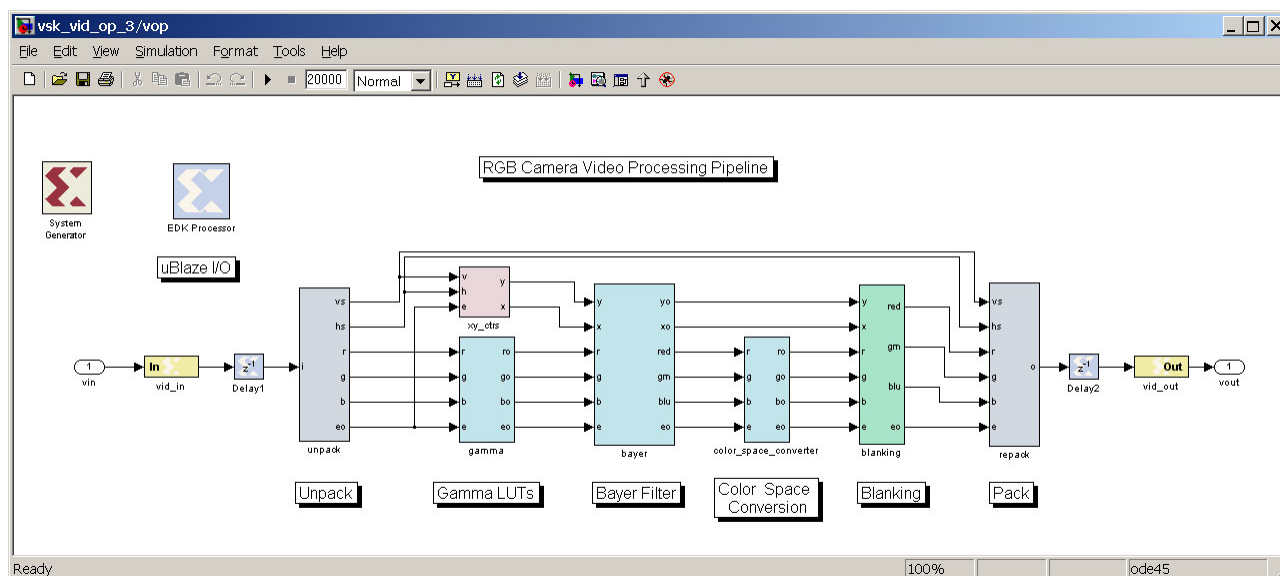


Figure 1-4: RGB Camera Video Processing Pipeline

The RGB camera processing pipeline design has a video input and a video output port. In the complete application, these video buses are connected to other pcors implementing

video processing, memory or I/O to the VIODC. The block diagram of the VSK diagnostics program is shown in [Figure 1-5](#).

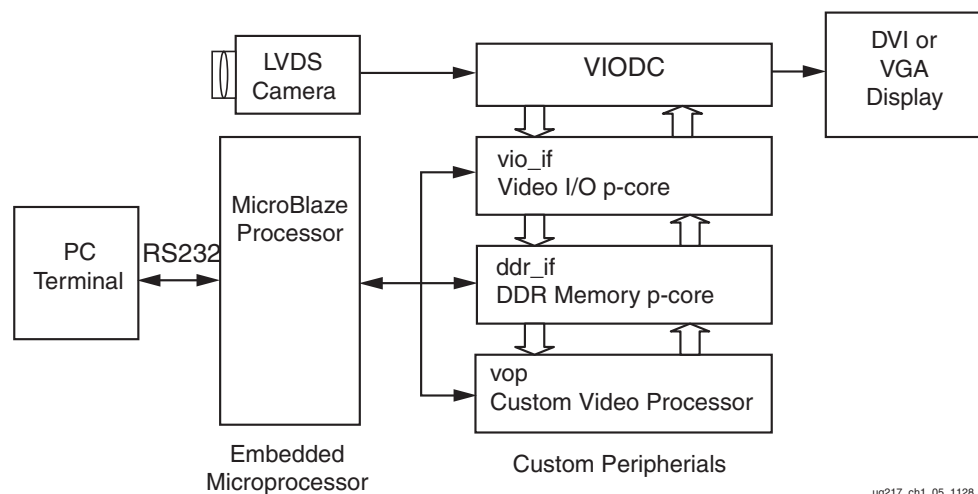


Figure 1-5: Block Diagram of VSK RGB Camera Demo Included in the VSK

For this application, the embedded MicroBlaze processor is used to configure the video processing pipeline. It communicates with memories and registers in the video pcores via System Generator shared memory primitives. The hardware logic and software drivers required by MicroBlaze to communicate with the shared memories in the pcore are automatically generated by System Generator during compilation.

The video processing demo is included in a pcore named vop for Video Op. The Sysgen design is named `vsk_vid_op_6.mdl`. This demo is part of the VSK diagnostic program and can be found in the VSK examples directory. For more information, refer to [Chapter 5, “VSK Diagnostics and Support Tool Kit.”](#)

Software and Application Updates Available Online

VSK software and applications are supported by a [VSK web page](#) and the latest software and applications versions can be found there. The software support is integrated into System Generator and will be upgraded as new System Generator versions are released. New applications for the VSK will be posted on the VSK web page as they are developed.

Software Support Package Overview

The VSK includes hardware, software, and applications. Xilinx software is used to create applications which run on the VSK and Xilinx FPGAs. Three basic software flows are supported. These are illustrated in [Figure 1-6](#), [Figure 1-7](#), and [Figure 1-8](#).

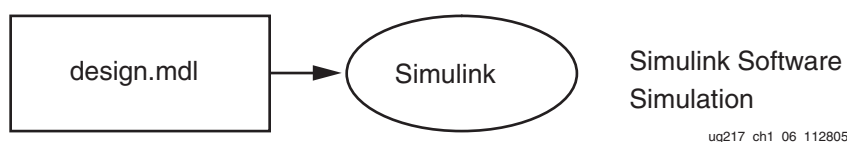


Figure 1-6: Software Simulation Flow

Software Simulation

In the first flow, called software simulation, Simulink designs that are constructed from the System Generator blocks are compiled and run in MATLAB Simulink. Figure 1-6 shows the software flow for software simulation. This flow is quick and easy to develop and offers good performance using the built-in MATLAB floating-point matrix operations. Larger systems, however, slow down significantly, and it is difficult to use this approach with live video streams. Additionally, problems occur when the design is implemented in fixed-point blocks for FPGA implementation. This can result in very low pixel rates due to poor simulation performance, often requiring hours per frame of video.

Hardware Implementation

The second software flow (Figure 1-7) compiles the user's design to hardware and runs the hardware on the VSK video development platform. This allows the video IP to be tested using live video streams.

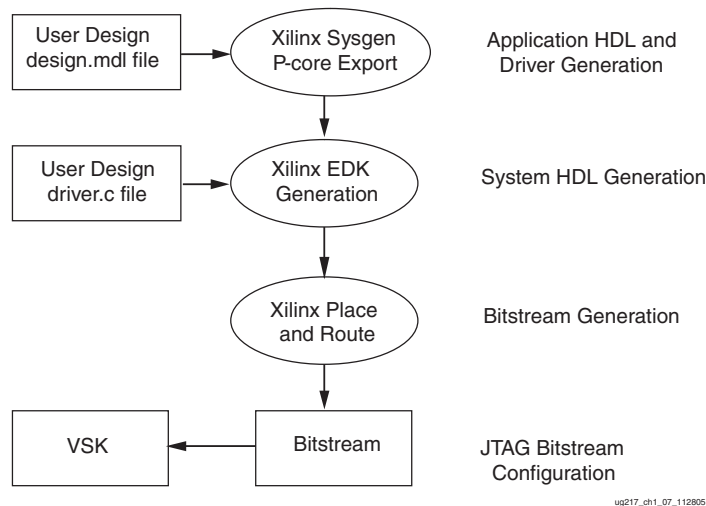


Figure 1-7: Real-Time Deployment Flow

Hardware Co-Simulation

The third type of software flow (Figure 1-8) is a hybrid of the software simulation and hardware deployment called Hardware-in-the-Loop co-simulation. In it, the bulk of the design is generated as in the real-time deployment flow. However, hardware data streams can be routed to the Simulink software simulation using the Xilinx System Generator Hardware co-sim engine.

The advantage of this mode is that small video filters which are part of a larger video processing system can be run in simulation, while the bulk of the video system is implemented in real time hardware. If buffering is employed, the software simulation can operate on stored video frames from the video stream at a reduced frame rate. Using the Ethernet Co-Simulation, near real-time video rates can be achieved. This translates to a few frames per second using 640 x 480 video.

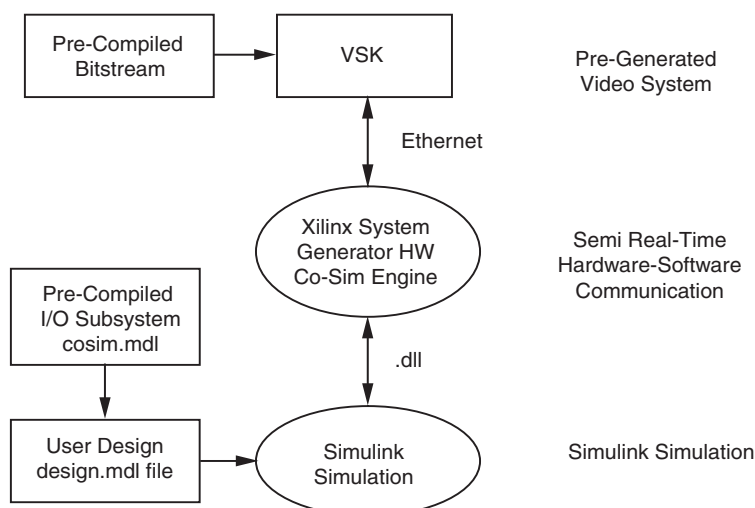


Figure 1-8: Hardware-in-the-Loop Flow

The pre-generated bitstream and co-sim subsystem can be generated from another system generator diagram or it can be an existing EDK project. The user can use the EDK import feature in System Generator to import an EDK project as a co-sim block.

VIODC HDL Support Package

While the above software flows leverage the advantages of developing video IP in System Generator/MATLAB/Simulink, users may prefer to use traditional HDL design flows. The Video Starter Kit also includes two demonstrations written in Verilog. These examples exercise all the video functions on the VIODC and are generally self-explanatory. In addition, these demos can run on a stand-alone VIODC board.

Refer to the *DVI, VGA, and Component Video Demonstration User Guide* and the *SDI Video Demonstration User Guide* for further information.

System Generator Support

System Generator includes several features that are useful for developing video applications with the Video Starter Kit. These are outlined below and additional documentation for each of these features can be found in the VSK document package. In addition, tutorials are included in the examples directory to assist in learning to use these powerful features.

DDR Memory Controller

The VSK includes a capable multi-port memory controller. The controller supports the DDR memory on the ML402 board. It can also be targeted to other boards and is fully configurable for port size and number of ports. The controller contains a simulation model and can be run in HDL co-simulation mode, or compiled to run in real time and as part of hardware co-simulation block.

Pcore Export and EDK Import

Pcore export is a new method of generation from Simulink diagrams that allows the user diagram to be imported into any EDK project as a Pcore. Conversely, EDK import allows EDK projects to be imported into System Generator diagrams. Pcore export is used to generate the three pcores in the VSK diagnostic demo from System Generator diagrams.

Multiple Subsystem Generator

The Multiple Subsystem Generator flow allows System Generator models to include multiple clock domains. This flow is used to generate the design for the VIODC FPGA, which is included in the VSK diagnostics program.

Ethernet Co-Sim

High-speed Ethernet co-sim and point-to-point Ethernet co-sim are supported by the System Generator for the VSK. To achieve near real-time video rates, reusable buffer blocks are included in the Ethernet demos that are included in the VSK.

Diagnostics

A diagnostics program called the `vsk_diagnostics` is included with the VSK. Refer to [Chapter 5, “VSK Diagnostics and Support Tool Kit”](#) for more information. The diagnostics include System Generator designs for the VIODC FPGA, and three pcores integrated into an EDK project for the ML402 FPGAs. They also include software routines to configure the video interface chips on the VIODC and to control the video processing pcore, video interface pcore, and DDR memory pcore.

Demonstrations

Several demonstration designs are included with the VSK.

MPEG Decoding Demo

The VSK diagnostics include an MPEG-4 demo, which can be run from the Compact Flash. Refer to the *Video Starter Kit Quick Start Guide* (UG239) and the *MPEG-4 Demonstration User Guide* (UG234) for more details.

VSK Diagnostics Camera Demo

The VSK diagnostics also include a camera demo, which can be run from the Compact Flash. Refer to *Video Starter Kit Quick Start Guide* (UG239) and [Chapter 5, “VSK Diagnostics and Support Tool Kit”](#) for more details.

SDI Demo

A demo featuring the SDI interface and written in Verilog is available for the VIODC. Refer to the documents *SDI Video Demonstration User Guide* in the VSK document package for further information.