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ML501 Evaluation Platform

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/30/06	1.0	Initial Xilinx release.
09/18/06	1.0.1	Minor typographical edit.
03/15/07	1.1	• Updated description for “4. Oscillator Sockets,” page 18 • Expanded Table 1-4, page 18 • Updated Appendix A, “Programming the IDT Clock Chip”
11/26/07	1.2	• Added sections on “MIG Compliance,” page 16 and “37. System Monitor,” page 34 • Added Appendix B, “References”
06/13/08	1.2.1	• Updated links in Appendix B, “References.” • Removed obsolete reference to XAPP445.
11/10/08	1.3	• Added content to “17. System ACE and CompactFlash Connector,” page 27 and “Configuration Options,” page 36. • Updated Platform Flash memory to Platform Flash PROM throughout.
08/24/09	1.4	• Updated the audio codec frequencyin “4. Oscillator Sockets.” • Updated programming instructions for the Clock Generator in “Programming the IDT Clock Chip” in Appendix A.

Table of Contents

About This Guide

The ML50*x* evaluation platforms enable designers to investigate and experiment with features of Virtex®-5 FPGAs. This user guide describes the features and operation of the ML501 Evaluation Platform.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "ML501 Evaluation Platform," provides details on the board components
- Appendix A, "Programming the IDT Clock Chip," is a tutorial that steps through programming the clock chip on the ML501 board
- Appendix B, "References"

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 FPGA Family Overview

  The features and product selection of the Virtex-5 FPGA family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 FPGA family.

- Virtex-5 FPGA User Guide

  This user guide includes chapters on:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM and FIFO memory
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - I/O Logic Resources
  - Advanced I/O Logic Resources

- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platform devices.

- Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller User Guide

  This user guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT and SXT platform devices.

- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express® Designs

  This user guide describes the integrated Endpoint blocks in the Virtex-5 LXT and SXT platform devices for PCI Express designs.

- XtremeDSP Design Considerations

  This guide describes the XtremeDSP. slice and includes reference designs for using the DSP48E.

- Virtex-5 FPGA Configuration User Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA Packaging and Pinout Specification

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx® website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the Virtex-5 *Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Documentation" for details.
Red text	Cross-reference link to a location in another document	See Figure 5 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

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Chapter 1

ML501 Evaluation Platform

Introduction

The ML501 Evaluation Platform enables designers to investigate and experiment with features of Virtex-5 LX FPGAs. This user guide describes features and operation of the ML501 Evaluation Platform.

Features

- Virtex-5 XC5VLX50-1FFG676 FPGA
- 64-bit DDR2 small outline DIMM (SODIMM), compatible with EDK supported IP and software drivers
- Programmable system clock generator chip
- One differential clock input pair and differential clock output pair with SMA connectors
- 3.3V clock oscillator socket populated with a 100-MHz oscillator
- General purpose DIP switches, LEDs, and pushbuttons
- Expansion header with 32 single-ended I/O, 16 LVDS capable differential pairs, 14 spare I/Os shared with buttons and LEDs, power, JTAG chain expansion capability, and IIC bus expansion
- Stereo AC97 audio codec with line-in, line-out, 50-mW headphone, microphone-in jacks, and SPDIF digital audio jacks
- RS-232 serial port
- 16-character x 2-line LCD display
- One 8-Kb IIC EEPROM
- DVI video connector (VGA supported with included adapter)
- PS/2 mouse and keyboard connectors
- System ACE™ CompactFlash configuration controller with Type I CompactFlash connector
- ZBT synchronous SRAM, 9 Mb on 32-bit data bus with four parity bits
- Intel P30 StrataFlash linear flash chips (32 MB)
- Serial Peripheral Interface™ (SPI) Flash (2 MB)
- 10/100/1000 tri-speed Ethernet PHY transceiver
- USB interface chip with host and peripheral ports
- Piezo audio transducer
- Rechargeable lithium battery to hold FPGA encryption keys

- Xilinx XC95144XL CPLD for glue logic
- Xilinx XCF32P Platform Flash PROM configuration storage device
- JTAG configuration port for use with Parallel Cable III, Parallel Cable IV, or Platform USB download cable
- Onboard power supplies for all necessary voltages
- Temperature and voltage monitoring chip with fan controller
- 5V @ 3A AC adapter
- Power indicator LED
- System monitor

Package Contents

- Xilinx Virtex-5 FPGA ML501 Evaluation Platform
- System ACE CompactFlash card
- Power supply
- DVI to VGA adaptor

Additional Information

For current information about the ML501 Evaluation Platform, visit www.xilinx.com/ml501

The information includes:

- Current version of this user guide in PDF format
- Example design files for demonstration of Virtex-5 FPGA features and technology
- Demonstration hardware and software configuration files for the System ACE controller, Platform Flash PROM configuration storage device, CPLD, and linear flash chips
- MicroBlaze™ EDK reference design files
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Allegro PCB format
- Gerber files for the PC board (Many free or shareware Gerber file viewers are available on the internet for viewing and printing these files.)
- Additional documentation, errata, frequently asked questions, and the latest news

For information about the Virtex-5 family of FPGA devices, including product highlights, data sheets, user guides, and application notes, see the Virtex-5 FPGA website at www.xilinx.com/virtex5. Additional information is available from the data sheets and application notes from the component manufacturers.

Block Diagram

Figure 1-1 shows a block diagram of the ML501 Evaluation Platform (board).

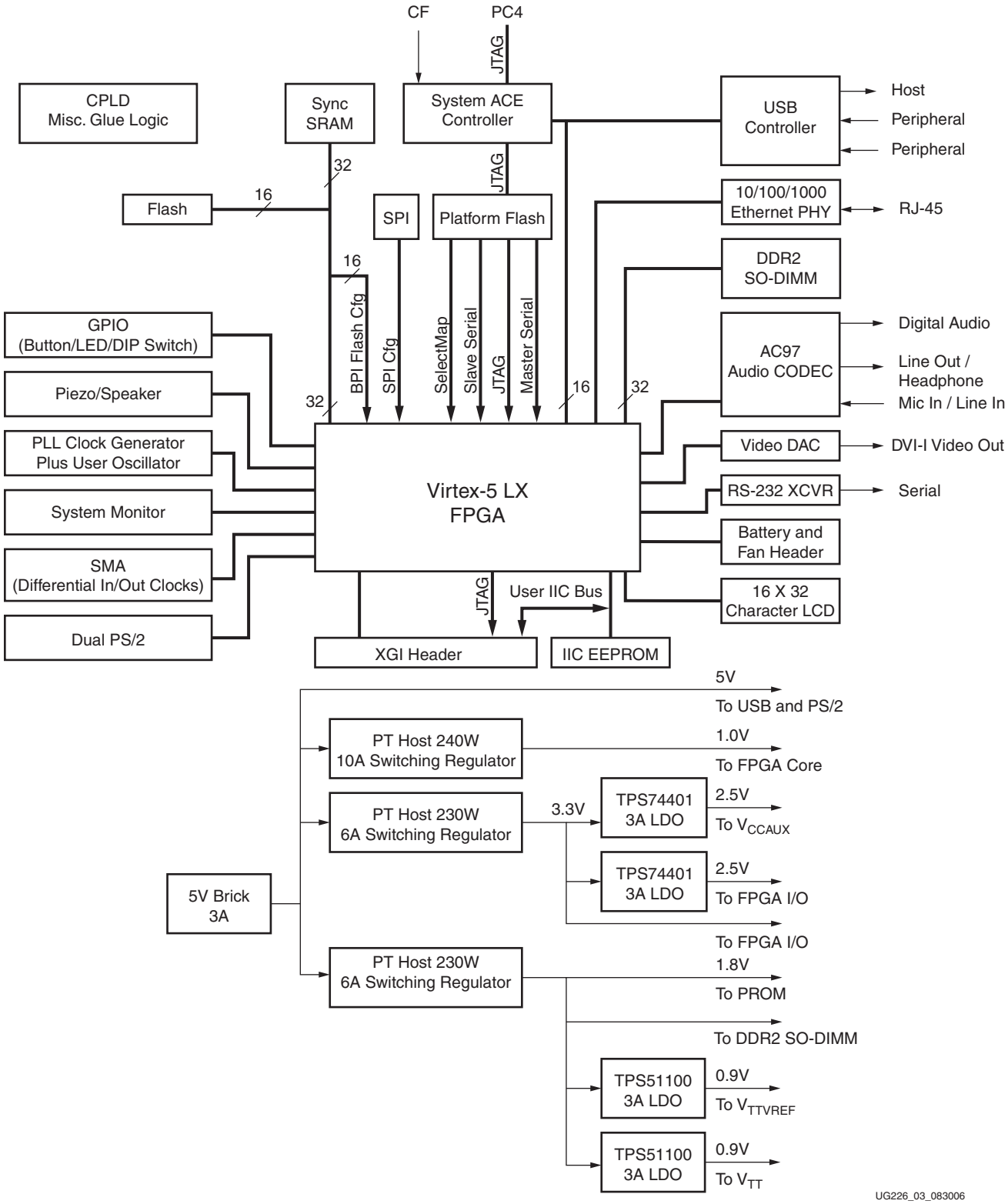

Figure 1-1: **Virtex-5 FPGA ML501 Evaluation Platform Block Diagram**

Detailed Description

The ML501 Evaluation Platform (board) is shown in Figure 1-2 (front) and Figure 1-3, page 13 (back). The numbered sections on the pages following the figures contain details on each feature.

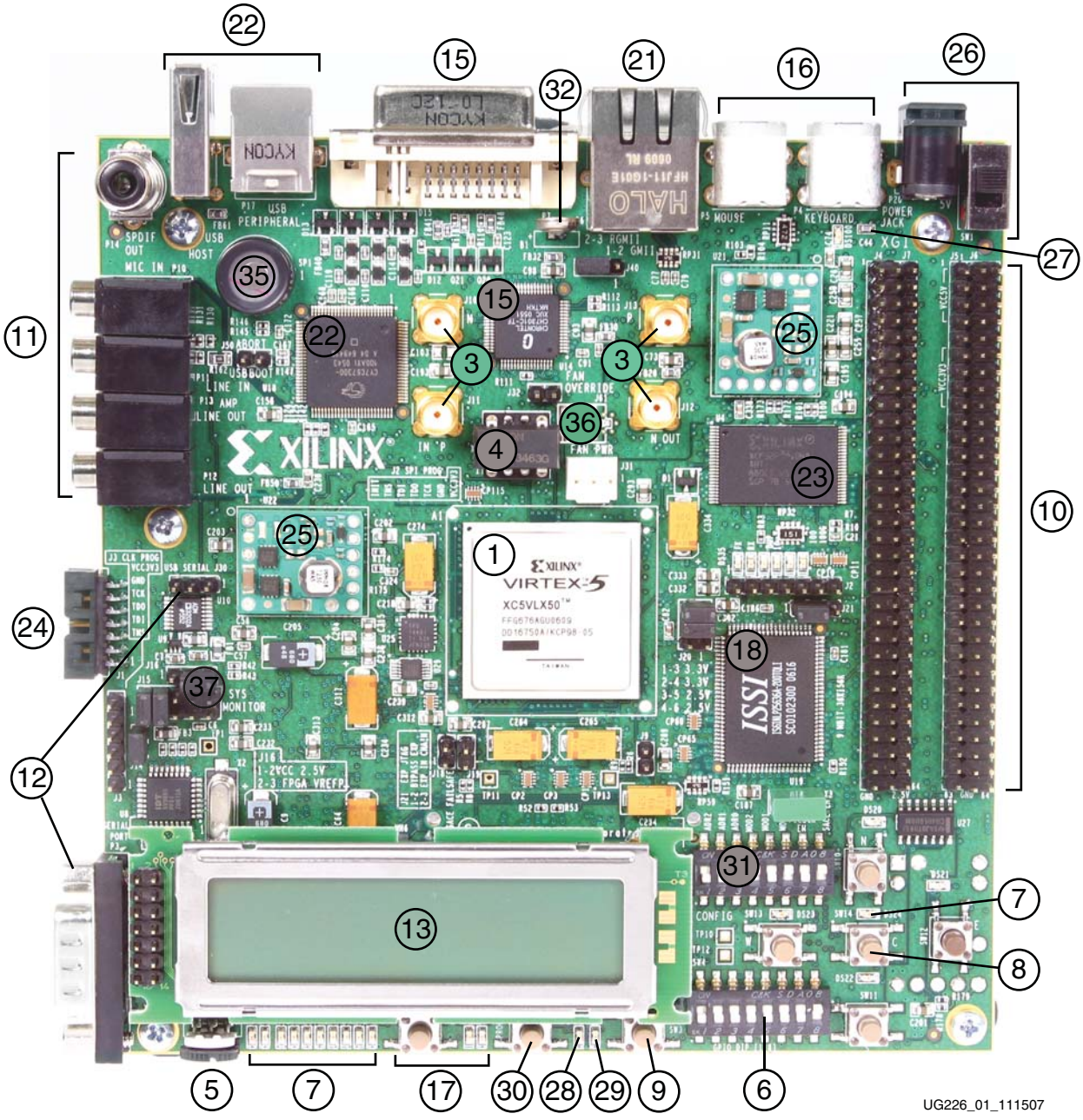

Figure 1-2: **Detailed Description of Virtex-5 FPGA ML501 Evaluation Platform Components (Front)**

Note: The label on the CompactFlash (CF) card shipped with your board might differ from the one shown.

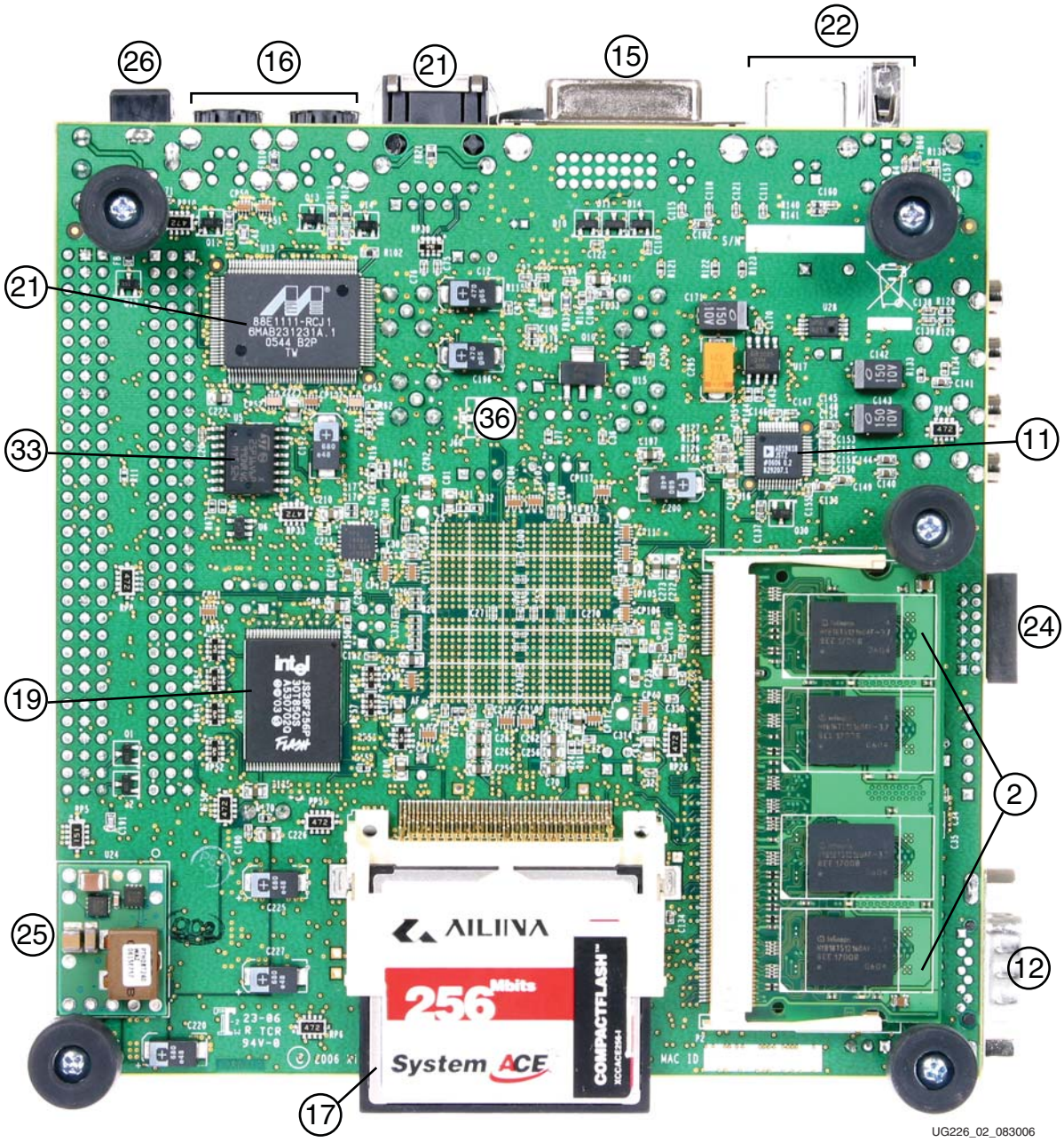

Figure 1-3: **Detailed Description of Virtex-5 FPGA ML501 Evaluation Platform Components (Back)**

1. Virtex-5 FPGA

A Xilinx Virtex-5 FPGA, XC5VLX50-1FFG676, is installed on the Evaluation Platform (the board).

Configuration

The board supports configuration in all modes: JTAG, Master Serial, Slave Serial, Master SelectMAP, Slave SelectMAP, Byte-wide Peripheral Interface (BPI) Up, BPI Down, and SPI modes. See the "Configuration Options," page 36 section for more information.

I/O Voltage Rails

The FPGA has 14 banks. The I/O voltage applied to each bank is summarized in Table 1-1.

Table 1-1: **I/O Voltage Rail of FPGA Banks**

FPGA Bank	I/O Voltage Rail
0	3.3V
1	3.3V
2	3.3V
3	2.5V
4	3.3V
11	User selectable as 2.5V or 3.3V using jumper J20
12	3.3V
13	User selectable as 2.5V or 3.3V using jumper J20
14	1.8V
15	3.3V
16	1.8V
17	3.3V
18	1.8V
21	1.8V

Digitally Controlled Impedance

Some FPGA banks can support the digitally controlled impedance (DCI) feature in Virtex-5 FPGAs. Support for DCI is summarized in Table 1-2.

Table 1-2: **DCI Capability of FPGA Bank**

FPGA Bank	DCI Capability
1	Not supported.
2	Not supported.
3	Not supported.
4	Not supported.
11	Yes, 49.9Ω resistors are installed.
12	Not supported.
13	Yes, 49.9Ω resistors are installed.
14	Yes, 49.9Ω resistors are installed.
15	Yes, 49.9Ω resistors are installed.
16	Yes, 49.9Ω resistors are installed.
17	Yes, 49.9Ω resistors are installed.
18	Not supported.
21	Yes, 49.9Ω resistors are installed.

2. DDR2 SODIMM

The ML501 platform is shipped with a single-rank unregistered 256 MB SODIMM. The DDR2 SODIMM used is generally a Micron MT4HTF3264HY-53E or similar module. Serial Presence Detect (SPD) using an IIC interface to the DDR DIMM is also supported with the FPGA.

Note: The board is only tested for DDR2 SDRAM operation at a 400 MHz data rate. Faster data rates might be possible but are not tested.

MIG Compliance

The ML50*x* DDR2 interface is MIG pinout compliant. The MIG DDR2 routing guidelines outlined in the *Xilinx Memory Interface Generator (MIG) User Guide* [Ref 13] have been achieved.

The board's DDR2 SODIMM memory interface is designed to the requirements defined by the *MIG User Guide* using the MIG tool. The MIG documentation requires that designers follow the MIG pinout and layout guidelines. The MIG tool generates and ensures that the proper FPGA I/O pin selections are made in support of the board's DDR2 interface. The initial pin selection for the board was modified and then re-verified to meet the MIG pinout requirements. To ensure a robust interface, the ML50*x* DDR2 layout incorporates matched trace lengths for data signals to the corresponding data strobe signal as defined in the MIG user guide. See Appendix B, "References" for links to additional information about MIG and Virtex-5 FPGAs in general.

DDR2 Memory Expansion

The DDR2 interface support user installation of SODIMM modules with more memory since higher order address and chip select signals are also routed from the SODIMM to the FPGA.

DDR2 Clock Signal

Two matched length pairs of DDR2 clock signals are broadcast from the FPGA to the SODIMM. The FPGA design is responsible for driving both clock pairs with low skew. The delay on the clock trace is designed to match the delay of the other DDR2 control signals.

DDR2 Signaling

All DDR2 SDRAM control signals are terminated through 47Ω resistors to a 0.9V VTT reference voltage. The FPGA DDR2 interface supports SSTL18 signaling and all DDR2 signals are controlled impedance. The DDR2 data, mask, and strobe signals are matched length within byte groups. The ODT functionality of the SODIMM should be utilized.

3. Differential Clock Input And Output With SMA Connectors

High-precision clock signals can be input to the FPGA using differential clock signals brought in through 50Ω SMA connectors. This allows an external function generator or other clock source to drive the differential clock inputs that directly feed the global clock input pins of the FPGA. The FPGA can be configured to present a 100Ω termination impedance.

A differential clock output from the FPGA is driven out through a second pair of SMA connectors. This allows the FPGA to drive a precision clock to an external device such as a piece of test equipment. Table 1-3 summarizes the differential SMA clock pin connections.

Table 1-3: **Differential SMA Clock Connections**

Label	Clock Name	FPGA Pin
J10	SMA_DIFF_CLK_IN_N	F10
J11	SMA_DIFF_CLK_IN_P	F9
J12	SMA_DIFF_CLK_OUT_N	F19
J13	SMA_DIFF_CLK_OUT_P	E18

4. Oscillator Sockets

The board has one crystal oscillator socket (X1) wired for standard LVTTL-type oscillators. It connects to the FPGA clock pin as shown in Table 1-4. The X1 socket is populated with a 100-MHz oscillator and is powered by the 3.3V supply.

The board also provides an IDT5V9885 (U8) EEPROM programmable clock generator device. This device is used to generate a variety of clocks to the board peripherals and FPGA. The programmable clock generator provides the following factory default single-ended outputs:

- 25 MHz to the Ethernet PHY (U13)
- 14.318 MHz to the audio codec (U16)
- 27 MHz to the USB controller (U18)
- 33 MHz to the Xilinx System ACE CF (U2)
- 33 MHz, 27 MHz, and a differential 200 MHz clock to the Xilinx FPGA

If users change the factory default configuration of the clock generator chip, the related reference design material might not work as designed. Instructions for returning the IDT5V9885 to the factory default configuration are provided in Appendix A, "Programming the IDT Clock Chip."

Table 1-4: **Oscillator Socket Connection**

Label	Clock Name	FPGA Pin	Description
X1	USER_CLK	AD8	100 MHz single-ended
U8	CLK_33MHZ_FPGA	AB12	33 MHz single-ended
U8	CLK_27MHZ_FPGA	AD13	27 MHz single-ended
U8	CLK_DIFF_FPGA_P	E16	200 MHz differential pair (pos)
U8	CLK_DIFF_FPGA_N	E17	200 MHz differential pair (neg)

5. LCD Brightness and Contrast Adjustment

Turning potentiometer R87 adjusts the image contrast of the character LCD. The potentiometer should be turned with a screwdriver.

6. DIP Switches (Active-High)

Eight general-purpose (active-High) DIP switches are connected to the user I/O pins of the FPGA. Table 1-5 summarizes these connections.

Table 1-5: **DIP Switch Connections (SW4)**

SW4	FPGA Pin
GPIO_DIP_SW1	U4
GPIO_DIP_SW2	V3
GPIO_DIP_SW3	T4
GPIO_DIP_SW4	T5
GPIO_DIP_SW5	U6

Table 1-5: **DIP Switch Connections (SW4) *(Continued)***

SW4	FPGA Pin
GPIO_DIP_SW6	U5
GPIO_DIP_SW7	U7
GPIO_DIP_SW8	T7

7. User and Error LEDs (Active-High)

There are a total of 15 active-High LEDs directly controllable by the FPGA:

- Eight green LEDs are general purpose LEDs arranged in a row
- Five green LEDs are positioned next to the North-East-South-West-Center-oriented pushbuttons (only the *center* one is cited in Figure 1-2, page 12)
- Two red LEDs are intended to be used for signaling error conditions, such as bus errors, but can be used for any other purpose

Some LEDs are buffered through the CPLD to allow the LED signals to be used as higher-performance I/O by way of the XGI expansion connector. Table 1-6 summarizes the LED definitions and connections.

Table 1-6: **User and Error LED Connections**

Reference Designator	Label/Definition	Color	FPGA Pin	Buffered
DS20	LED North	Green	Y8	Yes
DS21	LED East	Green	Y18	Yes
DS22	LED South	Green	AA8	Yes
DS23	LED West	Green	AA18	Yes
DS24	LED Center	Green	T22	Yes
DS17	GPIO LED 0	Green	E13	Yes
DS16	GPIO LED 1	Green	D14	Yes
DS15	GPIO LED 2	Green	E12	Yes
DS14	GPIO LED 3	Green	F12	Yes
DS13	GPIO LED 4	Green	D15	No
DS12	GPIO LED 5	Green	E15	No
DS11	GPIO LED 6	Green	E10	No
DS10	GPIO LED 7	Green	E11	No
D56	Error 1	Red	N4	No
D55	Error 2	Red	P5	No

8. User Pushbuttons (Active-High)

Five active-High user pushbuttons are available for general purpose usage and are arranged in a North-East-South-West-Center orientation (only the *center* one is cited in Figure 1-2, page 12). Table 1-7 summarizes the user pushbutton connections.

Table 1-7: **User Pushbutton Connections**

Reference Designator	Label/Definition	FPGA Pin
SW10	N (GPIO North)	A22
SW12	E (GPIO East)	A23
SW11	S (GPIO South)	B22
SW13	W (GPIO West)	C21
SW14	C (GPIO Center)	B21

9. CPU Reset Button (Active-Low)

The CPU reset button is an active-Low pushbutton and is used as a system or user reset button. This pushbutton switch is wired only to an FPGA I/O pin so it can also be used as a general-purpose pushbutton switch (see Table 1-8).

Table 1-8: **CPU Reset Connections**

Reference Designator	Label/Definition	FPGA Pin
SW3	CPU RESET	T23

10. XGI Expansion Headers

The board contains expansion headers for easy expansion or adaptation of the board for other applications. The expansion connectors use standard 0.1-inch headers. The expansion connectors contain connections to single-ended and differential FPGA I/Os, ground, 2.5V/3.3V/5V power, JTAG chain, and the IIC bus. All signals on connectors J4 and J6 have matched length traces that are matched to each other.

Differential Expansion I/O Connectors

Header J4 contains 16 pairs of differential signal connections to the FPGA I/Os. This permits the signals on this connector to carry high-speed differential signals, such as LVDS data. All differential signals are routed with 100Ω differential trace impedance. Matched length traces are used across all differential signals on J4. Consequently, these signals connect to the FPGA I/O, and they can be used as independent single-ended nets. The V_{CCIO} of these signals can be set to 2.5V or 3.3V by setting jumper J20. Table 1-9, page 21 summarizes the differential connections on this expansion I/O connector.

Table 1-9: **Expansion I/O Differential Connections (J4)**

J4 Differential Pin Pair		Schematic Net Name		FPGA Pin	
Pos	**Neg**	**Pos**	**Neg**	**Pos**	**Neg**
4	2	HDR2_4	HDR2_2	F24	F25
8	6	HDR2_8	HDR2_6	E25	E26
12	10	HDR2_12	HDR2_10	G21	G22
16	14	HDR2_16	HDR2_14	P19	N19
20	18	HDR2_20	HDR2_18	J25	J26
24	22	HDR2_24	HDR2_22	R22	R23
28	26	HDR2_28	HDR2_26	N22	N21
32	30	HDR2_32	HDR2_30	V26	U26
36	34	HDR2_36	HDR2_34	K23	K22
40	38	HDR2_40	HDR2_38	G26	H26
44	42	HDR2_44	HDR2_42	L20	L19
48	46	HDR2_48	HDR2_46	P23	N23
52	50	HDR2_52	HDR2_50	G24	G25
56	54	HDR2_56	HDR2_54	M20	M19
60	58	HDR2_60	HDR2_58	H24	J24
64	62	HDR2_64	HDR2_62	P21	P20

Single-Ended Expansion I/O Connectors

Header J6 contains 32 single-ended signal connections to the FPGA I/Os. This permits the signals on this connector to carry high-speed, single-ended data. All single-ended signals on connector J6 are matched length traces. The V_{CCIO} of these signals can be set to 2.5V or 3.3V by setting jumper J20. Table 1-10 summarizes the single-ended connections on this expansion I/O connector.

Table 1-10: **Expansion I/O Single-Ended Connections (J6)**

J6 Pin	Schematic Net Name	FPGA Pin
2	HDR1_2	J20
4	HDR1_4	J23
6	HDR1_6	J21
8	HDR1_8	H23
10	HDR1_10	M22
12	HDR1_12	K20
14	HDR1_14	K21
16	HDR1_16	M21
18	HDR1_18	L25
20	HDR1_20	L24
22	HDR1_22	K26
24	HDR1_24	K25
26	HDR1_26	M26
28	HDR1_28	M25
30	HDR1_30	N24
32	HDR1_32	M24
34	HDR1_34	AB25
36	HDR1_36	N26
38	HDR1_38	P25
40	HDR1_40	P24
42	HDR1_42	T24
44	HDR1_44	T25
46	HDR1_46	U24
48	HDR1_48	U25
50	HDR1_50	W25
52	HDR1_52	W26
54	HDR1_54	Y25

Table 1-10: **Expansion I/O Single-Ended Connections (J6) *(Continued)***

J6 Pin	Schematic Net Name	FPGA Pin
56	HDR1_56	Y26
58	HDR1_58	P26
60	HDR1_60	AA25
62	HDR1_62	AC26
64	HDR1_64	AB26

Other Expansion I/O Connectors

In addition to the high-speed I/O paths, additional I/O signals and power connections are available to support expansion cards plugged into the ML501 board. Fourteen I/O pins from the general-purpose pushbutton switches and LEDs on the board are connected to expansion connector J5. This permits additional I/Os to connect to the expansion connector if the pushbutton switches and LEDs are not used. The connection also allows the expansion card to utilize the pushbutton switches and LEDs on the board.

The expansion connector also allows the board's JTAG chain to be extended onto the expansion card by setting jumper J21 accordingly.

The IIC bus on the board is also extended onto the expansion connector to allow additional IIC devices to be bused together. If the expansion IIC bus is to be utilized, the user must have the IIC pull-up resistors present on the expansion card. Bidirectional level shifting transistors allow the expansion card to utilize 2.5V to 5V signaling on the IIC bus.

Power supply connections to the expansion connectors provide ground, 2.5V, 3.3V, and 5V power pins. If the expansion card draws significant power from the ML501 board, ensure that the total power draw can be supplied by the board.

The ML501 expansion connector is backward compatible with the expansion connectors on the ML40*x*, ML32*x*, and ML42*x* boards, thereby allowing their daughter cards to be used with the ML501 Evaluation Platform. Table 1-11, page 24 summarizes the additional expansion I/O connections.

Table 1-11: **Additional Expansion I/O Connections (J5)**

J5 Pin	Label	FPGA Pin	Description
1	VCC5	–	5V Power Supply
2	VCC5	–	5V Power Supply
3	VCC5	–	5V Power Supply
4	VCC5	–	5V Power Supply
5	NC	–	Not Connected
6	VCC3V3	–	3.3V Power Supply
7	VCC3V3	–	3.3V Power Supply
8	VCC3V3	–	3.3V Power Supply
9	VCC3V3	–	3.3V Power Supply
10	NC	–	Not Connected
11	FPGA_EXP_TMS	–	Expansion TMS
12	FPGA_EXP_TCK	–	Expansion TCK
13	FPGA_EXP_TDO	–	Expansion TDO
14	FPGA_EXP_TDI	–	Expansion TDI
15	GPIO_LED_N	Y8	LED North
16	SW3 (N)	A22	GPIO Switch North
17	GPIO_LED_C	T22	LED Center
18	SW14 (C)	B21	GPIO Switch Center
19	GPIO_LED_W	AA18	LED West
20	SW13 (W)	C21	GPIO Switch West
21	GPIO_LED_S	AA8	LED South
22	SW11 (S)	B22	GPIO Switch South
23	GPIO_LED_E	Y18	LED East
24	SW12 (E)	A23	GPIO Switch East
25	GPIOLED 0	E13	GPIO LED 0
26	GPIOLED 1	D14	GPIO LED 1
27	GPIOLED 2	E12	GPIO LED 2
28	GPIOLED 3	F12	GPIO LED 3
29	NC	-	Not Connected
30	NC	-	Not Connected
31	IIC_SCL_EXP	R20	Expansion IIC SCL
32	IIC_SDA_EXP	T20	Expansion IIC SDA

11. Stereo AC97 Audio Codec

The ML501 board has an AC97 audio codec (U16) to permit audio processing. The Analog Devices AD1981 Audio Codec supports stereo 16-bit audio with up to 48-kHz sampling. The sampling rate for record and playback can be different.

Note: The reset for the AC97 codec is shared with the reset signal for the flash memory chips and is designed to be asserted at power-on or at system reset.

Separate audio jacks are provided for Microphone, Line In, Line Out, and Headphone. All jacks are stereo except for Microphone. The Headphone jack is driven by the audio codec's internal 50-mW amplifier. The SPDIF jack supplies digital audio output from the codec. Table 1-12 summarizes the audio jacks.

Table 1-12: **ML501 Audio Jacks**

Reference Designator	Function
P10	Microphone - In
P11	Analog Line - In
P12	Analog Line - Out
P13	Headphone - Out
P14	SPDIF - Out

12. RS-232 Serial Port

The ML501 board contains one male DB-9 RS-232 serial port, allowing the FPGA to communicate serial data with another device. The serial port is wired as a host (DCE) device. Therefore, a null modem cable is normally required to connect the board to the serial port on a computer. The serial port is designed to operate up to 115200 Bd. An interface chip is used to shift the voltage level between FPGA and RS-232 signals.

Note: The FPGA is connected only to the TX and RX data pins on the serial port. Therefore, other RS-232 signals, including hardware flow-control signals, are not used. Flow control should be disabled when communicating with a computer.

A secondary serial interface is available by using header J30 to support debug of the USB controller chip. Header J30 brings out RS-232 voltage level signals for ground, TX data, and RX data.

13. 16-Character x 2-Line LCD

The ML501 board has a 16-character x 2-line LCD (Tianma TM162VBA6) on the board to display text information. Potentiometer R87 adjusts the contrast of the LCD. The data interface to the LCD is connected to the FPGA to support 4-bit mode only. The CPLD is used to shift the voltage level between the FPGA and the LCD. The LCD module has a connector that allows the LCD to be removed from the board to access to the components below it.

Caution! Care should be taken not to scratch or damage the surface of the LCD window.