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Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

DS202 (v5.3) May 5, 2010 **Product Specification**

Virtex-5 FPGA Electrical Characteristics

Virtex®-5 FPGAs are available in -3, -2, -1 speed grades, with -3 having the highest performance. Virtex-5 FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-5 FPGA data sheet, part of an overall set of documentation on the Virtex-5 family of FPGAs, is available on the Xilinx website:

- Virtex-5 Family Overview
- Virtex-5 FPGA User Guide
- Virtex-5 FPGA Configuration Guide
- Virtex-5 FPGA XtremeDSP™ Design Considerations
- Virtex-5 FPGA Packaging and Pinout Specification
- Embedded Processor Block in Virtex-5 FPGAs Reference Guide
- Virtex-5 FPGA RocketIO™ GTP Transceiver User Guide
- Virtex-5 FPGA RocketIO GTX Transceiver User Guide
- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide
- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express® Designs
- Virtex-5 FPGA System Monitor User Guide
- Virtex-5 FPGA PCB Designer's Guide

All specifications are subject to change without notice.

Virtex-5 FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.05	V
V_{REF}	Input reference voltage	–0.5 to 3.75	V
V_{IN}(3)	3.3V I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.75 to 4.05	V
	3.3V I/O input voltage relative to GND (restricted to maximum of 100 user I/Os)(5)	–0.95 to 4.4 (Commercial Temperature)	V
		–0.85 to 4.3 (Industrial Temperature)	
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
I_{IN}	Current applied to an I/O pin, powered or unpowered	±100	mA
	Total current applied to all I/O pins, powered or unpowered	±100	mA
V_{TS}	Voltage applied to 3-state 3.3V output(4) (user and dedicated I/Os)	–0.75 to 4.05	V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(2)	+220	°C
T_J	Maximum junction temperature(2)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines, refer to UG112: *Device Package User Guide*. For thermal considerations, refer to UG195: *Virtex-5 FPGA Packaging and Pinout Specification* on the Xilinx website.
3. 3.3V I/O absolute maximum limit applied to DC and AC signals.
4. For 3.3V I/O operation, refer to UG190: *Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines.*
5. For more flexibility in specific designs, a maximum of 100 user I/Os can be stressed beyond the normal specification for no more than 20% of a data period.

Table 2: **Recommended Operating Conditions**

Symbol	Description	Temperature Range	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	0.95	1.05	V
	Internal supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	0.95	1.05	V
V_{CCAUX}(1)	Auxiliary supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	2.375	2.625	V
V_{CCO}(2,4,5)	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	1.14	3.45	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.14	3.45	V
V_{IN}	3.3V supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	GND – 0.20	3.45	V
	3.3V supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	GND – 0.20	3.45	V
	2.5V and below supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	GND – 0.20	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(6)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode	Commercial		10	mA
		Industrial		10	mA
V_{BATT}(3)	Battery voltage relative to GND, T_J = 0°C to +85°C	Commercial	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:

1. Recommended maximum voltage drop for V_{CCAUX} is 10 mV/ms.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
6. A total of 100 mA per bank should not be exceeded.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Data Rate	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)		0.75			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)		2.0			V
I_{REF}	V_{REF} leakage current per pin				10	µA
I_L	Input or output leakage current per pin (sample-tested)				10	µA
C_{IN}	Input capacitance (sample-tested)				8	pF
I_{RPU}(1)	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V		20		150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V		10		90	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V		5		45	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V		3		30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V		2		15	µA
I_{RPD}(1)	Pad pull-down (when selected) @ V_{IN} = 2.5V		5		110	µA
I_{BATT}(2)	Battery supply current				150	nA
n	Temperature diode ideality factor			1.0002		n
r	Series resistance			5.0		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.

Important Note

Typical values for quiescent supply current are now specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Data sheets for older products (e.g., Virtex-4 devices) still specify typical quiescent supply current at T_j = 25°C. Quiescent supply current is specified by speed grade for Virtex-5 devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade			Units
			-3 (C)	-2 (C & I)	-1 (C & I)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC5VLX20T	N/A	406	253	mA
		XC5VLX30	480	480	300	mA
		XC5VLX30T	507	507	317	mA
		XC5VLX50	651	651	449	mA
		XC5VLX50T	689	689	475	mA
		XC5VLX85	1072	1072	833	mA
		XC5VLX85T	1115	1115	866	mA
		XC5VLX110	1391	1391	1109	mA
		XC5VLX110T	1448	1448	1154	mA
		XC5VLX155	2615	2615	2141	mA
		XC5VLX155T	2674	2674	2188	mA
		XC5VLX220	N/A	2783	2278	mA
		XC5VLX220T	N/A	2844	2328	mA
		XC5VLX330	N/A	4193	3432	mA
		XC5VLX330T	N/A	4267	3492	mA
		XC5VSX35T	720	720	554	mA
		XC5VSX50T	1092	1092	840	mA
		XC5VSX95T	N/A	1924	1475	mA
		XC5VSX240T	N/A	4137	3168	mA
		XC5VTX150T	N/A	2067	2067	mA
		XC5VTX240T	N/A	2881	2881	mA
		XC5VFX30T	1024	1024	1024	mA
		XC5VFX70T	1658	1658	1658	mA
		XC5VFX100T	2875	2875	2875	mA
		XC5VFX130T	3041	3041	3041	mA
		XC5VFX200T	N/A	3755	3755	mA

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade			Units
			-3 (C)	-2 (C & I)	-1 (C & I)	
I_{CCOQ}	Quiescent V_{CCO} supply current	XC5VLX20T	N/A	2	2	mA
		XC5VLX30	1.5	1.5	1.5	mA
		XC5VLX30T	1.5	1.5	1.5	mA
		XC5VLX50	2	2	2	mA
		XC5VLX50T	2	2	2	mA
		XC5VLX85	3	3	3	mA
		XC5VLX85T	3	3	3	mA
		XC5VLX110	4	4	4	mA
		XC5VLX110T	4	4	4	mA
		XC5VLX155	8	8	8	mA
		XC5VLX155T	8	8	8	mA
		XC5VLX220	N/A	8	8	mA
		XC5VLX220T	N/A	8	8	mA
		XC5VLX330	N/A	12	12	mA
		XC5VLX330T	N/A	12	12	mA
		XC5VSX35T	1.5	1.5	1.5	mA
		XC5VSX50T	2	2	2	mA
		XC5VSX95T	N/A	4	4	mA
		XC5VSX240T	N/A	12	12	mA
		XC5VTX150T	N/A	7	7	mA
		XC5VTX240T	N/A	7	7	mA
		XC5VFX30T	4	4	4	mA
		XC5VFX70T	6	6	6	mA
		XC5VFX100T	7	7	7	mA
		XC5VFX130T	8	8	8	mA
		XC5VFX200T	N/A	10	10	mA

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade			Units
			-3 (C)	-2 (C & I)	-1 (C & I)	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC5VLX20T	N/A	32	32	mA
		XC5VLX30	38	38	38	mA
		XC5VLX30T	43	43	43	mA
		XC5VLX50	57	57	57	mA
		XC5VLX50T	62	62	62	mA
		XC5VLX85	93	93	93	mA
		XC5VLX85T	98	98	98	mA
		XC5VLX110	125	125	125	mA
		XC5VLX110T	130	130	130	mA
		XC5VLX155	172	172	172	mA
		XC5VLX155T	177	177	177	mA
		XC5VLX220	N/A	229	229	mA
		XC5VLX220T	N/A	236	236	mA
		XC5VLX330	N/A	345	345	mA
		XC5VLX330T	N/A	353	353	mA
		XC5VSX35T	49	49	49	mA
		XC5VSX50T	74	74	74	mA
		XC5VSX95T	N/A	131	131	mA
		XC5VSX240T	N/A	300	300	mA
		XC5VTX150T	N/A	180	180	mA
		XC5VTX240T	N/A	300	300	mA
		XC5VFX30T	60	60	60	mA
		XC5VFX70T	110	110	110	mA
		XC5VFX100T	150	150	150	mA
		XC5VFX130T	180	180	180	mA
		XC5VFX200T	N/A	250	250	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (Tj). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx® FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The power supplies can be turned on in any sequence, though the specifications shown in Table 5 are for the recommended power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. The I/O will remain 3-stated through power-on if the recommended power-on sequence is followed. Xilinx does not specify the current or I/O behavior for other power-on sequences.

Table 5 shows the minimum current required by Virtex-5 devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-5 Devices**

Device	$I_{CCINTMIN}$ Typ(1)	$I_{CCAUXMIN}$ Typ(1)	I_{CCOMIN} Typ(1)	Units
XC5VLX20T	172	54	50	mA
XC5VLX30	235	76	50	mA
XC5VLX30T	246	86	50	mA
XC5VLX50	320	114	50	mA
XC5VLX50T	336	124	50	mA
XC5VLX85	492	186	100	mA
XC5VLX85T	515	196	100	mA
XC5VLX110	623	250	100	mA
XC5VLX110T	651	260	100	mA
XC5VLX155	695	351	100	mA
XC5VLX155T	728	368	100	mA
XC5VLX220	1023	458	150	mA
XC5VLX220T	1056	472	150	mA
XC5VLX330	1470	690	150	mA
XC5VLX330T	1509	706	150	mA
XC5VSX35T	307	98	50	mA
XC5VSX50T	472	148	50	mA
XC5VSX95T	804	262	100	mA
XC5VSX240T	1632	662	150	mA
XC5VTX150T	969	386	150	mA
XC5VTX240T	1245	572	150	mA
XC5VFX30T	358	116	50	mA
XC5VFX70T	695	232	100	mA
XC5VFX100T	749	298	100	mA
XC5VFX130T	1111	392	150	mA
XC5VFX200T	1222	534	150	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. The maximum startup current can be obtained using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools and adding the quiescent plus dynamic current consumption.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.3	0.8	2.0	3.45	0.4	2.4	Note(3)	Note(3)
LVCMOS33, LVDCI33	–0.3	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(6)	Note(6)
PCI33_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note(5)	Note(5)
PCI66_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note(5)	Note(5)
PCI-X(5)	–0.2	35% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note(5)	Note(5)
GTLP	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	–	0.6	N/A	36	N/A
GTL	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	–	0.4	N/A	32	N/A
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
HSTL IV(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	48	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33_3, PCI66_3, and PCI-X, refer to **UG190**: *Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines*.
6. Supported drive strengths of 2, 4, 6, or 8 mA.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15		15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15		15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15		15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15		15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825			V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals		–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	820	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see UG190: *Virtex-5 FPGA User Guide, Chapter 6, SelectIO Resources*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6		2.2	V
V_{IDIFF}	Differential Input Voltage(1,2)	0.100		1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

PowerPC 440 Switching Characteristics

Consult the *Embedded Processor Block in Virtex-5 FPGAs Reference Guide* for further information.

Table 12: **Processor Block Switching Characteristics**

Clock Name	Description	Speed Grade			Units
		-3	-2	-1	
CPMC440CLK	CPU clock	550	475	400	MHz
CPMINTERCONNECTCLK	Xbar clock	366.6	316.6	266.6	MHz
CPMPPCS0PLBCLK	Slave 0 PLB clock(1)	183.3	158.3	133.3	MHz
CPMPPCS1PLBCLK	Slave 1 PLB clock(1)	183.3	158.3	133.3	MHz
CPMPPCMPLBCLK	Master PLB clock(1)	183.3	158.3	133.3	MHz
CPMMCCLK	Memory interface clock(1)(2)	366.6	316.6	266.6	MHz
CPMFCMCLK	FCM clock(1)	275	237.5	200	MHz
CPMDCRCLK	FPGA logic DCR clock(1)	183.3	158.3	133.3	MHz
CPMDMA0LLCLK	DMA0 LL clock(1)	250	250	200	MHz
CPMDMA1LLCLK	DMA1 LL clock(1)	250	250	200	MHz
CPMDMA2LLCLK	DMA2 LL clock(1)	250	250	200	MHz
CPMDMA3LLCLK	DMA3 LL clock(1)	250	250	200	MHz
JTGC440TCK	JTAG clock	50	50	50	MHz
CPMC440TIMERCLOCK	Timer clock	275	237.5	200	MHz

Notes:

1. Typical bus frequencies are provided for reference only, actual frequencies are user-design dependent.
2. Refer to DS567 for maximum clock speed of designs using the DDR2 Memory Controller for PowerPC® 440 Processors.

Table 13: **Processor Block MIB Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMMCCLK	1.146	1.247	1.463	ps
$T_{CK\_ADDRESS}$		CPMMCCLK	1.017	1.136	1.38	ps
T_{CK_DATA}		CPMMCCLK	1.076	1.172	1.38	ps
$T_{CONTROL\_CK}$		CPMMCCLK	0.736	0.844	0.941	ps
T_{DATA_CK}		CPMMCCLK	0.834	0.95	1.058	ps

Table 14: **Processor Block PLBM Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMPPCMPLBCLK	0.971	1.095	1.354	ps
$T_{CK\_ADDRESS}$		CPMPPCMPLBCLK	1.215	1.372	1.673	ps
T_{CK_DATA}		CPMPPCMPLBCLK	1.115	1.257	1.535	ps
$T_{CONTROL\_CK}$		CPMPPCMPLBCLK	1.7	1.79	1.86	ps
T_{DATA_CK}		CPMPPCMPLBCLK	0.774	0.914	1.059	ps

Table 15: **Processor Block PLBS0 Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMPPCS0PLBCLK	1.063	1.196	1.462	ps
T_{CK_DATA}		CPMPPCS0PLBCLK	1.052	1.189	1.461	ps
$T_{CONTROL\_CK}$		CPMPPCS0PLBCLK	1.307	1.545	1.836	ps
$T_{ADDRESS\_CK}$		CPMPPCS0PLBCLK	1.253	1.492	1.787	ps
T_{DATA_CK}		CPMPPCS0PLBCLK	0.825	0.971	1.124	ps

Table 16: **Processor Block PLBS1 Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMPPCS1PLBCLK	1.083	1.234	1.525	ps
T_{CK_DATA}		CPMPPCS1PLBCLK	1.146	1.298	1.615	ps
$T_{CONTROL\_CK}$		CPMPPCS1PLBCLK	1.335	1.596	1.921	ps
$T_{ADDRESS\_CK}$		CPMPPCS1PLBCLK	1.328	1.568	1.864	ps
T_{DATA_CK}		CPMPPCS1PLBCLK	0.821	0.969	1.127	ps

Table 17: **Processor Block DMA0 Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMDMA0LLCLK	1.256	1.42	1.665	ps
T_{CK_DATA}		CPMDMA0LLCLK	1.312	1.472	1.712	ps
$T_{CONTROL\_CK}$		CPMDMA0LLCLK	0.453	0.558	0.716	ps
T_{DATA_CK}		CPMDMA0LLCLK	–0.105	–0.105	–0.104	ps

Table 18: **Processor Block DMA1 Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMDMA1LLCLK	1.127	1.266	1.474	ps
T_{CK_DATA}		CPMDMA1LLCLK	1.266	1.418	1.645	ps
$T_{CONTROL\_CK}$		CPMDMA1LLCLK	0.447	0.555	0.717	ps
T_{DATA_CK}		CPMDMA1LLCLK	–0.014	0.01	0.046	ps

Table 19: **Processor Block DMA2 Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMDMA2LLCLK	1.101	1.235	1.437	ps
T_{CK_DATA}		CPMDMA2LLCLK	1.127	1.262	1.463	ps
$T_{CONTROL\_CK}$		CPMDMA2LLCLK	0.771	0.924	1.155	ps
T_{DATA_CK}		CPMDMA2LLCLK	0.135	0.142	0.168	ps

Table 20: **Processor Block DMA3 Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMDMA3LLCLK	1.094	1.242	1.462	ps
T_{CK_DATA}		CPMDMA3LLCLK	1.056	1.184	1.376	ps
$T_{CONTROL\_CK}$		CPMDMA3LLCLK	0.636	0.767	0.965	ps
T_{DATA_CK}		CPMDMA3LLCLK	0.087	0.119	0.116	ps

Table 21: **Processor Block DCR Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMDCRCLK				
$T_{CK\_ADDRESS}$		CPMDCRCLK				
T_{CK_DATA}		CPMDCRCLK				
$T_{CONTROL\_CK}$		CPMDCRCLK				
$T_{ADDRESS\_CK}$		CPMDCRCLK				
T_{DATA_CK}		CPMDCRCLK				

Table 22: **Processor Block FCM Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CPMFCMCLK	0.967	1.084	1.324	ps
T_{CK_DATA}		CPMFCMCLK	1.041	1.158	1.4	ps
$T_{CK\_INSTRUCTION}$		CPMFCMCLK	0.701	0.818	1.06	ps
$T_{CONTROL\_CK}$		CPMFCMCLK	1.057	1.218	1.395	ps
T_{DATA_CK}		CPMFCMCLK	0.608	0.698	0.768	ps
T_{RESULT_CK}		CPMFCMCLK	0.608	0.698	0.768	ps

Table 23: **Processor Block MISC Switching Characteristics**

Clock Name	Description	Reference Clock	Speed Grade			Units
			-3	-2	-1	
Clock-to-out and setup relative to clock						
$T_{CK\_CONTROL}$		CLK1				
$T_{CK\_ADDRESS}$		CLK2				
T_{CK_DATA}		CLK3				
$T_{CONTROL\_CK}$		CLK4				
$T_{ADDRESS\_CK}$		CLK5				
T_{DATA_CK}		CLK6				

GTP_DUAL Tile Specifications

GTP_DUAL Tile DC Characteristics

Table 24: **Absolute Maximum Ratings for GTP_DUAL Tiles**

Symbol	Description		Units
MGTAVCCPLL	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	–0.5 to 1.32	V
MGTAVTTTX	Analog supply voltage for the GTP_DUAL transmitters relative to GND	–0.5 to 1.32	V
MGTAVTTRX	Analog supply voltage for the GTP_DUAL receivers relative to GND	–0.5 to 1.32	V
MGTAVCC	Analog supply voltage for the GTP_DUAL common circuits relative to GND	–0.5 to 1.1	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	–0.5 to 1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 25: **Recommended Operating Conditions for GTP_DUAL Tiles(1)(2)**

Symbol	Description	Min	Max	Units
MGTAVCCPLL(1)	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	1.14	1.26	V
MGTAVTTTX(1)	Analog supply voltage for the GTP_DUAL transmitters relative to GND	1.14	1.26	V
MGTAVTTRX(1)	Analog supply voltage for the GTP_DUAL receivers relative to GND	1.14	1.26	V
MGTAVCC(1)	Analog supply voltage for the GTP_DUAL common circuits relative to GND	0.95	1.05	V
MGTAVTTRXC(1)	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	1.14	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_J = –40°C to +100°C.

Table 26: **DC Characteristics Over Recommended Operating Conditions for GTP_DUAL Tiles(1)**

Symbol	Description	Min	Typ	Max	Units
$I_{MGTAVTTTX}$	GTP_DUAL tile transmitter termination supply current(2)		71	90	mA
$I_{MGTAVCCPLL}$	GTP_DUAL tile shared PLL supply current		36	60	mA
$I_{MGTAVTTRXC}$	GTP_DUAL tile resistor termination calibration supply current		0.1	0.5	mA
$I_{MGTAVTTRX}$	GTP_DUAL tile receiver termination supply current(3)		0.1	0.5	mA
$I_{MGTAVCC}$	GTP_DUAL tile internal analog supply current		56	110	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	49.9 ± 1% tolerance			Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.2 Gb/s line rate.
2. ICC numbers are given per GTP_DUAL tile with both GTP transceivers operating with default settings.
3. AC coupled TX/RX link.

Table 27: **GTP_DUAL Tile Quiescent Supply Current**

Symbol	Description	Typ(1)	Max	Units
$I_{AVTTTXQ}$	Quiescent MGTAVTTTX (transmitter termination) supply current	8.5	18	mA
$I_{AVCCPLLQ}$	Quiescent MGTAVCCPLL (PLL) supply current	8	18	mA
$I_{AVTTRXQ}$	Quiescent MGTAVTTRX (receiver termination) supply current. Includes MGTAVTTRXCQ.	0.1	0.8	mA
I_{AVCCQ}	Quiescent MGTAVCC (analog) supply current	2.5	11	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTP_DUAL tile quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP_DUAL tiles in the target LXT or SXT device.

GTP_DUAL Tile DC Input and Output Levels

Table 28 summarizes the DC output specifications of the GTP_DUAL tiles in Virtex-5 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* for further details.

Table 28: **GTP_DUAL Tile DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 3.2 Gb/s	150		2000	mV
		External AC coupled > 3.2 Gb/s	180		2000	mV
V_{IN}	Absolute input voltage	DC coupled	–400		MGTAVTTRX + 400 up to 1320	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V		800		mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			1400	mV
V_{SEOUT}	Single-ended output voltage swing(1)	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			700	mV
V_{CMOUT}	Common mode output voltage	Equation based MGTAVTTTX = 1.2V	1200 – Amplitude/2			mV
R_{IN}	Differential input resistance		90	100	120	Ω
R_{OUT}	Differential output resistance		90	100	120	Ω
T_{OSKEW}	Transmitter output skew				15	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

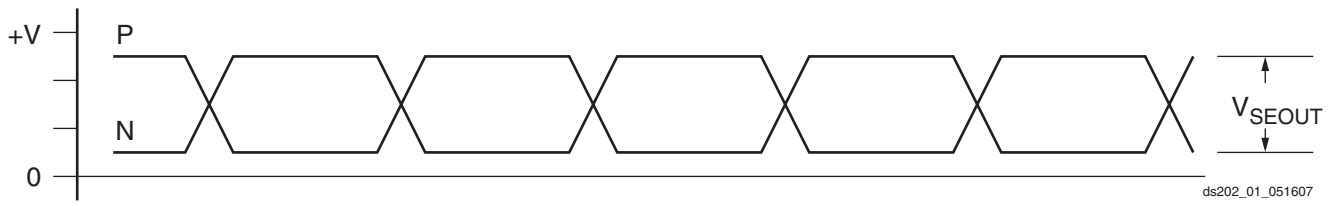

Figure 1: **Single-Ended Output Voltage Swing**

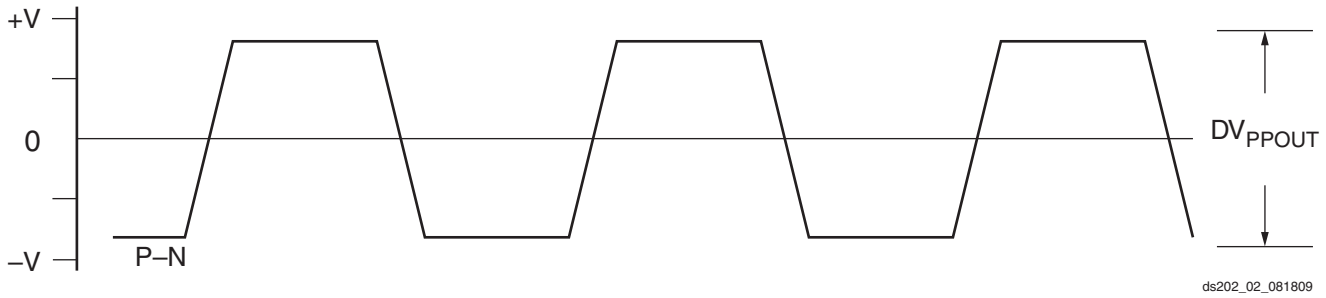

Figure 2: **Peak-to-Peak Differential Output Voltage**

Table 29 summarizes the DC specifications of the clock input of the GTP_DUAL tile. Figure 3 shows the single-ended input voltage swing. Figure 4 shows the peak-to-peak differential clock input voltage swing. Consult UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* for further details.

Table 29: **GTP_DUAL Tile Clock DC Input Specifications(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		200	800	2000	mV
V_{ISE}	Single-ended input voltage		100	400	1000	mV
R_{IN}	Differential input resistance		80	105	130	Ω
C_{EXT}	Required external AC coupling capacitor		75	100	200	nF

Notes:

1. V_{MIN} = 0V and V_{MAX} = 1200mV

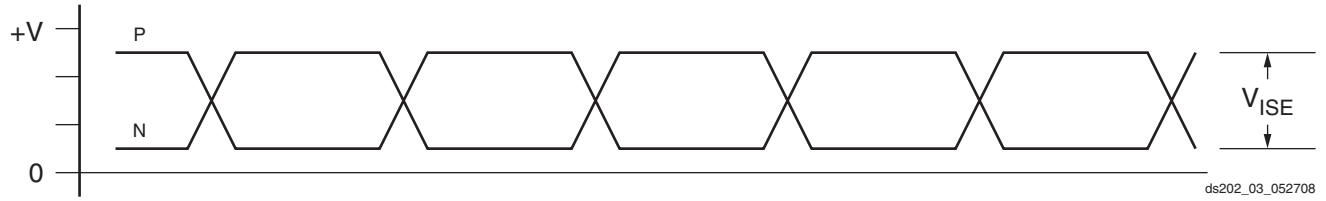

Figure 3: **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

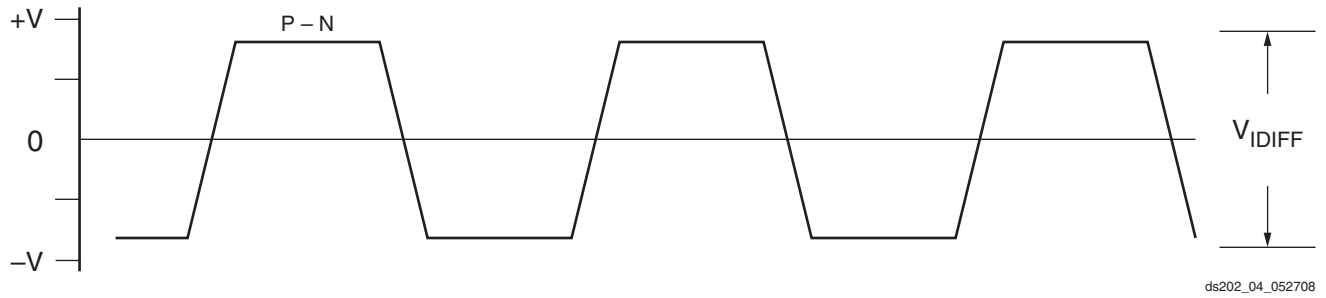

Figure 4: **Differential Clock Input Voltage Swing Peak-to-Peak**

GTP_DUAL Tile Switching Characteristics

Consult UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* for further information.

Table 30: **GTP_DUAL Tile Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.75	3.75	3.2	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.0	2.0	2.0	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.0	1.0	1.0	GHz

Table 31: **Dynamic Reconfiguration Port (DRP) in the GTP_DUAL Tile Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTPDRPCLK}$	GTP DCLK (DRP clock) maximum frequency	200	175	150	MHz

Table 32: **GTP_DUAL Tile Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range(1)	CLK	60		350	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200	400	ps
T_{FCLK}	Reference clock fall time	80% – 20%		200	400	ps
T_{DCREF}	Reference clock duty cycle(2)	CLK	40	50	60	%
T_{GJTT}	Reference clock total jitter, peak-peak(3)	CLK			40	ps
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock			1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock			200	µs

Notes:

1. The clock from the GTP_DUAL differential clock pin pair can be used for all serial bit rates. GREFCLK can be used for serial bit rates up to 1 Gb/s.
2. For reference clock rates above 325 MHz, a duty cycle of 45% to 55% must be maintained.
3. Measured at the package pin. GTP_DUAL jitter characteristics measured using a clock with specification T_{GJTT}.

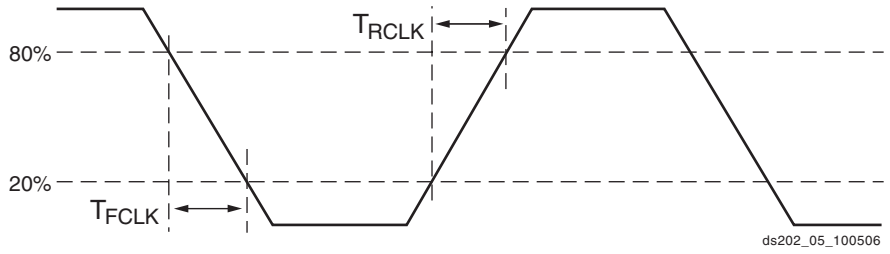

Figure 5: **Reference Clock Timing Parameters**

Table 33: **GTP_DUAL Tile User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency		375	375	320	MHz
F_{RXREC}	RXRECCLK maximum frequency		375	375	320	MHz
T_{RX}	RXUSRCLK maximum frequency		375	375	320	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	RXDATAWIDTH = 0	350	350	320	MHz
		RXDATAWIDTH = 1	187.5	187.5	160	MHz
T_{TX}	TXUSRCLK maximum frequency		375	375	320	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	TXDATAWIDTH = 0	350	350	320	MHz
		TXDATAWIDTH = 1	187.5	187.5	160	MHz

Notes:

1. Clocking must be implemented as described in UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*

Table 34: **GTP_DUAL Tile Transmitter Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.1		F_{GTPMAX}	Gb/s
T_{RTX}	TX Rise time			140		ps
T_{FTX}	TX Fall time			120		ps
T_{LLSKEW}	TX lane-to-lane skew(1)				855	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude				20	mV
$T_{TXOOBTRANS}$	Electrical idle transition time				40	ns
$T_{J3.75}$	Total Jitter(2)	3.75 Gb/s			0.35	UI
$D_{J3.75}$	Deterministic Jitter(2)				0.19	UI
$T_{J3.2}$	Total Jitter(2)	3.20 Gb/s			0.35	UI
$D_{J3.2}$	Deterministic Jitter(2)				0.19	UI
$T_{J2.5}$	Total Jitter(2)	2.50 Gb/s			0.30	UI
$D_{J2.5}$	Deterministic Jitter(2)				0.14	UI
$T_{J2.0}$	Total Jitter(2)	2.00 Gb/s			0.30	UI
$D_{J2.0}$	Deterministic Jitter(2)				0.14	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s			0.20	UI
$D_{J1.25}$	Deterministic Jitter(2)				0.10	UI
$T_{J1.00}$	Total Jitter(2)	1.00 Gb/s			0.20	UI
$D_{J1.00}$	Deterministic Jitter(2)				0.10	UI
T_{J500}	Total Jitter(2)	500 Mb/s			0.10	UI
D_{J500}	Deterministic Jitter(2)				0.04	UI
T_{J100}	Total Jitter(2)	100 Mb/s			0.02	UI
D_{J100}	Deterministic Jitter(2)				0.01	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP_DUAL sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1.
3. All jitter values are based on a Bit-Error Ratio of $1e^{-12}$.

Table 35: **GTP_DUAL Tile Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTPRX}	Serial data rate	RX oversampler not enabled	0.5		F_{GTPMAX}	Gb/s
		RX oversampler enabled	0.1		0.5	Gb/s
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak	OOBDETECT_THRESHOLD = 100	60	105	165	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000		0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed			150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance(2)	CDR 2nd-order loop disabled with PLL_RXDIVSEL_OUT = 1(3)	–200		200	ppm
		CDR 2nd-order loop disabled with PLL_RXDIVSEL_OUT = 2(3)	–200		200	ppm
		CDR 2nd-order loop disabled with PLL_RXDIVSEL_OUT = 4(3)	–100		100	ppm
		CDR 2nd-order loop enabled	–1000		1000	ppm
SJ Jitter Tolerance(4)						
$JT\_SJ_{3.75}$	Sinusoidal Jitter(5)	3.75 Gb/s	0.30			UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(5)	3.20 Gb/s	0.40			UI
$JT\_SJ_{2.50}$	Sinusoidal Jitter(5)	2.50 Gb/s	0.40			UI
$JT\_SJ_{2.00}$	Sinusoidal Jitter(5)	2.00 Gb/s	0.40			UI
$JT\_SJ_{1.00}$	Sinusoidal Jitter(5)	1.00 Gb/s	0.30			UI
JT_SJ_{500}	Sinusoidal Jitter(5)	500 Mb/s	0.30			UI
JT_SJ_{500}	Sinusoidal Jitter(5)	500 Mb/s OS	0.30			UI
JT_SJ_{100}	Sinusoidal Jitter(5)	100 Mb/s OS	0.30			UI
SJ Jitter Tolerance with Stressed Eye(4)						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(6)	3.20 Gb/s	0.87			UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(6)	3.20 Gb/s	0.30			UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1 only.
2. Indicates the maximum offset between the receiver reference clock and the serial data. For example, a reference clock with ±100 ppm resolution results in a maximum offset of 200 ppm between the reference clock and the serial data.
3. CDR 1st-order step size set to 2.
4. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
5. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
6. Stimulus signal includes 0.4UI of DJ and 0.17UI of RJ. RX equalizer is enabled.

GTX_DUAL Tile Specifications

GTX_DUAL Tile DC Characteristics

Table 36: **Absolute Maximum Ratings for GTX_DUAL Tiles**

Symbol	Description		Units
MGTAVCCPLL	Analog supply voltage for the GTX_DUAL shared PLL relative to GND	–0.5 to 1.1	V
MGTAVTTTX	Analog supply voltage for the GTX_DUAL transmitters relative to GND	–0.5 to 1.32	V
MGTAVTTRX	Analog supply voltage for the GTX_DUAL receivers relative to GND	–0.5 to 1.32	V
MGTAVCC	Analog supply voltage for the GTX_DUAL common circuits relative to GND	–0.5 to 1.1	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column	–0.5 to 1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 37: **Recommended Operating Conditions for GTX_DUAL Tiles(1)(2)**

Symbol	Description	Min	Max	Units
MGTAVCCPLL(1)	Analog supply voltage for the GTX_DUAL shared PLL relative to GND	0.95	1.05	V
MGTAVTTTX(1)	Analog supply voltage for the GTX_DUAL transmitters relative to GND	1.14	1.26	V
MGTAVTTRX(1)	Analog supply voltage for the GTX_DUAL receivers relative to GND	1.14	1.26	V
MGTAVCC(1)	Analog supply voltage for the GTX_DUAL common circuits relative to GND	0.95	1.05	V
MGTAVTTRXC(1)	Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column	1.14	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_J = –40°C to +100°C.

Table 38: **DC Characteristics Over Recommended Operating Conditions for GTX_DUAL Tiles(1)**

Symbol	Description	Min	Typ	Max	Units
$I_{MGTAVTTTX}$	GTX_DUAL tile transmitter termination supply current(2)		43.3	86.3	mA
$I_{MGTAVCCPLL}$	GTX_DUAL tile shared PLL supply current		38.0	99.4	mA
$I_{MGTAVTTRXC}$	GTX_DUAL tile resistor termination calibration supply current		0.1	0.5	mA
$I_{MGTAVTTRX}$	GTX_DUAL tile receiver termination supply current(3)		40.3	56.5	mA
$I_{MGTAVCC}$	GTX_DUAL tile internal analog supply current		80.5	179.5	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	59.0 ± 1% tolerance			Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.2 Gb/s line rate.
2. I_{CC} numbers are given per GTX_DUAL tile with both GTX transceivers operating with default settings.
3. AC coupled TX/RX link.
4. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 39: **GTX_DUAL Tile Quiescent Supply Current**

Symbol	Description	Typ(1)	Max	Units
$I_{AVTTTXQ}$	Quiescent MGTAVTTTX (transmitter termination) supply current	8.2	21.6	mA
$I_{AVCCPLLQ}$	Quiescent MGTAVCCPLL (PLL) supply current	0.8	4.8	mA
$I_{AVTTRXQ}$	Quiescent MGTAVTTRX (receiver termination) supply current. Includes MGTAVTTRXCQ.	1.2	12.0	mA
I_{AVCCQ}	Quiescent MGTAVCC (analog) supply current	9.0	50.4	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTX_DUAL tile quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX_DUAL tiles in the target TXT or FXT device.

GTX_DUAL Tile DC Input and Output Levels

Table 40 summarizes the DC output specifications of the GTX_DUAL tiles in Virtex-5 FPGAs. Figure 6 shows the single-ended output voltage swing. Figure 7 shows the peak-to-peak differential output voltage.

Consult UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 40: **GTX_DUAL Tile DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125		1800	mV
		External AC coupled > 4.25 Gb/s	125		1800	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400		MGTAVTTRX +400 up to 1320	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V		800		mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	TXBUFDIFFCTRL = 111			1400	mV
V_{SEOUT}	Single-ended output voltage swing(1)	TXBUFDIFFCTRL = 111			700	mV
V_{CMOUT}	Common mode output voltage	Equation based MGTAVTTTX = 1.2V	1200 – DV_{PPOUT}/2			mV
R_{IN}	Differential input resistance		85	100	120	Ω
R_{OUT}	Differential output resistance		85	100	120	Ω
T_{OSKEW}	Transmitter output skew			2	8	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

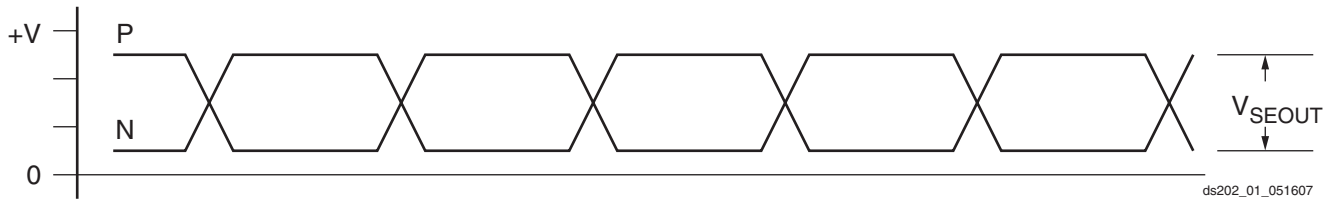

Figure 6: **Single-Ended Output Voltage Swing**

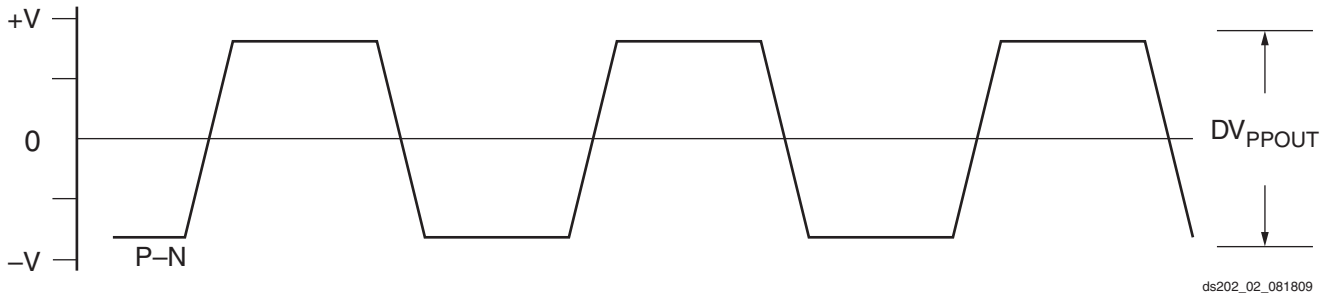

Figure 7: **Peak-to-Peak Differential Output Voltage**

Table 41 summarizes the DC specifications of the clock input of the GTX_DUAL tile. Figure 8 shows the single-ended input voltage swing. Figure 9 shows the peak-to-peak differential clock input voltage swing. Consult UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 41: **GTX_DUAL Tile Clock DC Input Level Specification(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
V_{ISE}	Single-ended input voltage		105	400	1000	mV
R_{IN}	Differential input resistance		90	105	130	Ω
C_{EXT}	Required external AC coupling capacitor			100		nF

Notes:

1. V_{MIN} = 0V and V_{MAX} = 1200mV

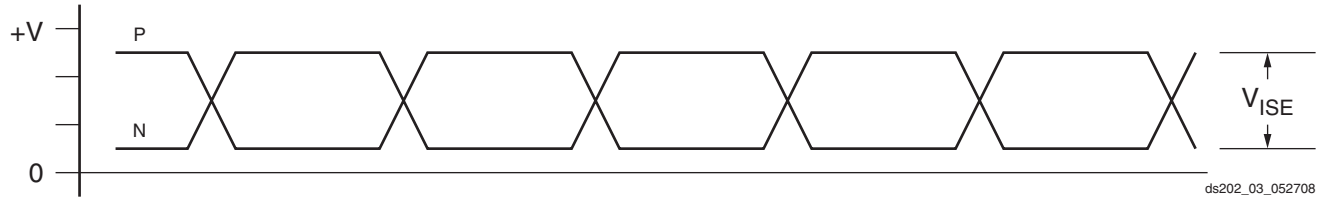

Figure 8: **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

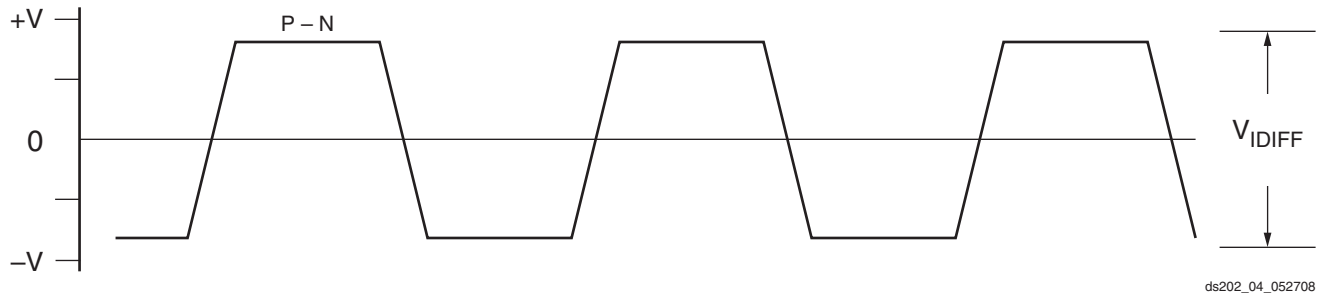

Figure 9: **Differential Clock Input Voltage Swing Peak-to-Peak**

GTX_DUAL Tile Switching Characteristics

Consult UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further information.

Table 42: **GTX_DUAL Tile Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.5	6.5	4.25	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.25	3.25	3.25	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.48	1.48	1.48	GHz

Table 43: **Dynamic Reconfiguration Port (DRP) in the GTX_DUAL Tile Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTXDRPCLK}$	GTX DCLK (DRP clock) maximum frequency	200	175	150	MHz

Table 44: **GTX_DUAL Tile Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range(1)	CLK	60		650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200		ps
T_{FCLK}	Reference clock fall time	80% – 20%		200		ps
T_{DCREF}	Reference clock duty cycle	CLK	40	50	60	%
T_{GJTT}	Reference clock total jitter (2, 3)	At 100 KHz		–145		dBc/Hz
		At 1 MHz		–150		dBc/Hz
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock		0.25	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock			200	µs

Notes:

1. GREFCLK can be used for serial bit rates up to 1 Gb/s; however, Jitter Specifications are not guaranteed when using GREFCLK.
2. GTX_DUAL jitter characteristics measured using a clock with specification T_{GJTT}. A reference clock with higher phase noise can be used with link margin trade off.
3. The selection of the reference clock is application dependent. This parameter describes the quality of the reference clock used during transceiver jitter characterization - see Table 46 and Table 47.

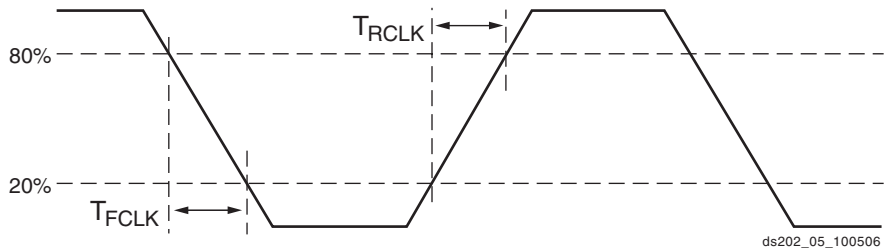

Figure 10: **Reference Clock Timing Parameters**

Table 45: **GTX_DUAL Tile User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Device	Speed Grade			Units
				-3	-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit datapath	FXT	325	325	212.5	MHz
			TXT	-	325	212.5	MHz
		Internal 16-bit datapath	FXT	406.25	406.25	265.625	MHz
			TXT	-	406.25	265.625	MHz
F_{RXREC}	RXRECCLK maximum frequency		FXT	406.25	406.25	265.625	MHz
			TXT	-	406.25	265.625	MHz
T_{RX}	RXUSRCLK maximum frequency		FXT	406.25	406.25	265.625	MHz
			TXT	-	406.25	265.625	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	FXT	375	312.5	235.625	MHz
		2 byte interface		406.25	390.625	265.625	MHz
		4 byte interface		203.125	203.125	132.813	MHz
		1 byte interface	TXT	-	312.5	235.625	MHz
		2 byte interface		-	265.625	265.625	MHz
		4 byte interface		-	203.125	132.813	MHz
T_{TX}	TXUSRCLK maximum frequency		FXT	406.25	406.25	265.625	MHz
			TXT	-	406.25	265.625	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	FXT	375	312.5	235.625	MHz
		2 byte interface		406.25	390.625	265.625	MHz
		4 byte interface		203.125	203.125	132.813	MHz
		1 byte interface	TXT	-	312.5	235.625	MHz
		2 byte interface		-	265.625	265.625	MHz
		4 byte interface		-	203.125	132.813	MHz

Notes:

1. Clocking must be implemented as described in UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.

Table 46: **GTX_DUAL Tile Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.15		F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%		120		ps
T_{FTX}	TX Fall time	80%–20%		120		ps
T_{LLSKEW}	TX lane-to-lane skew(1)				350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude				15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time				75	ns
$T_{J6.5}$	Total Jitter(2)	6.5 Gb/s			0.33	UI
$D_{J6.5}$	Deterministic Jitter(2)				0.17	UI
$T_{J5.0}$	Total Jitter(2)	5.0 Gb/s			0.33	UI
$D_{J5.0}$	Deterministic Jitter(2)				0.15	UI
$T_{J4.25}$	Total Jitter(2)	4.25 Gb/s			0.33	UI
$D_{J4.25}$	Deterministic Jitter(2)				0.14	UI

Table 46: **GTX_DUAL Tile Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.75}$	Total Jitter(2)	3.75 Gb/s			0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)				0.16	UI
$T_{J3.2}$	Total Jitter(2)	3.2 Gb/s			0.20	UI
$D_{J3.2}$	Deterministic Jitter(2)				0.10	UI
$T_{J3.2L}$	Total Jitter(2)	3.2 Gb/s(3)			0.36	UI
$D_{J3.2L}$	Deterministic Jitter(2)				0.16	UI
$T_{J2.5}$	Total Jitter(2)	2.5 Gb/s			0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)				0.08	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s			0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)				0.06	UI
T_{J750}	Total Jitter(2)(4)	750 Mb/s			0.10	UI
D_{J750}	Deterministic Jitter(2)(4)				0.03	UI
T_{J150}	Total Jitter(2)(4)	150 Mb/s			0.02	UI
D_{J150}	Deterministic Jitter(2)(4)				0.01	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTX_DUAL sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.
3. PLL frequency at 1.6 GHz and OUTDIV = 1.
4. GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.

Table 47: **GTX_DUAL Tile Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.75		F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.15		0.75	Gb/s
$T_{RXELECIDLE}$	TIme for RXELECIDLE to respond to loss or restoration of data	OOBDETECT_THRESHOLD = 110			75	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak	OOBDETECT_THRESHOLD = 110	55		135	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000		0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed			512	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance(2)	CDR 2nd-order loop disabled	–200		200	ppm
		CDR 2nd-order loop enabled	–2000		2000	ppm
SJ Jitter Tolerance(3)						
$JT\_SJ_{6.5}$	Sinusoidal Jitter(4)	6.5 Gb/s	0.44			UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(4)	5.0 Gb/s	0.44			UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(4)	4.25 Gb/s	0.44			UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(4)	3.75 Gb/s	0.44			UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(4)	3.2 Gb/s	0.45			UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter(4)	3.2 Gb/s(5)	0.45			UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(4)	2.5 Gb/s	0.50			UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(4)	1.25 Gb/s	0.50			UI

Table 47: **GTX_DUAL Tile Receiver Switching Characteristics *(Cont'd)***

Symbol	Description		Min	Typ	Max	Units
JT_SJ_{750}	Sinusoidal Jitter(4)(6)	750 Mb/s	0.57			UI
JT_SJ_{150}	Sinusoidal Jitter(4)(6)	150 Mb/s	0.57			UI
SJ Jitter Tolerance with Stressed Eye(3)						
$JT\_TJSE_{4.25}$	Total Jitter with Stressed Eye(7)	4.25 Gb/s	0.69			UI
$JT\_SJSE_{4.25}$	Sinusoidal Jitter with Stressed Eye(7)	4.25 Gb/s	0.1			UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. Indicates the maximum offset between the receiver reference clock and the serial data. For example, a reference clock with ±100 ppm resolution results in a maximum offset of 200 ppm between the reference clock and the serial data.
3. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
4. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
5. PLL frequency at 1.6 GHz and OUTDIV = 1.
6. GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.
7. Composite jitter with RX equalizer enabled. DFE disabled.

CRC Block Switching Characteristics

Table 48: **CRC Block Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{CRC}	CRCCLK maximum frequency	325	325	270	MHz

Ethernet MAC Switching Characteristics

Consult UG194: *Virtex-5 FPGA Tri-mode Ethernet Media Access Controller User Guide* for further information.

Table 49: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	1.25	1.25	1.25	MHz
		100 Mb/s – 8-bit width	12.5	12.5	12.5	MHz
		1000 Mb/s – 8-bit width	125	125	125	MHz
		2000 Mb/s – 16-bit width	125	125	125	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	MHz

Endpoint Block for PCI Express Designs Switching Characteristics

Consult UG197: *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide* for further information.

Table 50: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{PCIECORE}$	Core clock maximum frequency	250	250	250	MHz
$F_{PCIEUSER}$	User clock maximum frequency	250	250	250	MHz